Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details

Product Status	Active
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (84kB)
On-Chip RAM	54kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dspb56374ae

• Hardware Watchdog Timer

2.4 Packages

80-pin and 52-pin plastic LQFP packages.

3 Documentation

Table 2 lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 2. DSP56374 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56374 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56374UM/D
DSP56374 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56374
DSP56374 Product Brief	Brief description of the chip	DSP56374PB/D

4 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 3.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 3. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals[1]	Detailed Description
Power (V_{DD})		11	Table 15
Ground (GND)		9	Table 5
Scan Pins		1	Table 6
Clock and PLL		3	Table 7
Interrupt and mode control	Port H[2]	5	Table 8
SHI	Port H[2]	5	Table 9
ESAI	Port C[4]	12	Table 10
ESAI_1	Port E[5]	12	Table 11

Table 9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		I^2C Serial Clock—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through an external pull-up resistor according to the I^2C specifications. This signal is tri-stated during hardware, software, and individual reset. This pin has an internal pull up resistor. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is de-asserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		I^2C Data and Acknowledge—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR	Input or output	GPIO disconnected	Frame Sync for Receiver—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected		Port C1—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
FST	Input or output	GPIO disconnected	Frame Sync for Transmitter—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		Port C4—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

DSP56374 Data Sheet, Rev. 4.2

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.8   Enhanced Serial Audio Interface_1

Table 11. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		Port E2—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT_1	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		Port E5—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5_1	Output	GPIO disconnected	Serial Data Output 5_1—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		Serial Data Input 0_1—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		Port E6—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SDO4_1	Output	GPIO disconnected	Serial Data Output 4_1—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		Serial Data Input 1_1—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		Port E7—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		Port E8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.9   Dedicated GPIO-Port G

Table 12. Dedicated GPIO-Port G Signals

Signal Name	Type	State During Reset	Signal Description
PG0	Input, output, or disconnected	GPIO disconnected	Port G0—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG1	Input, output, or disconnected	GPIO disconnected	Port G1—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG2	Input, output, or disconnected	GPIO disconnected	Port G2—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG3	Input, output, or disconnected	GPIO disconnected	Port G3—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG4	Input, output, or disconnected	GPIO disconnected	Port G4—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG5	Input, output, or disconnected	GPIO disconnected	Port G5—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG6	Input, output, or disconnected	GPIO disconnected	Port G6—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG7	Input, output, or disconnected	GPIO disconnected	Port G7—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG8	Input, output, or disconnected	GPIO disconnected	Port G8—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

DSP56374 Data Sheet, Rev. 4.2

Table 12. Dedicated GPIO-Port G Signals (continued)

Signal Name	Type	State During Reset	Signal Description
PG9	Input, output, or disconnected	GPIO disconnected	Port G9—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG10	Input, output, or disconnected	GPIO disconnected	Port G10—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG11	Input, output, or disconnected	GPIO disconnected	Port G11—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG12	Input, output, or disconnected	GPIO disconnected	Port G12—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG13	Input, output, or disconnected	GPIO disconnected	Port G13—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG14	Input, output, or disconnected	GPIO disconnected	Port G14—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

DSP56374 Data Sheet, Rev. 4.2

4.10 Timer

Table 13. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	Timer 0 Schmitt-Trigger Input/Output—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input. Internal Pull down resistor. This input is 5 V tolerant
TIO1	Input or Output	Watchdog Timer Output	Timer 1 Schmitt-Trigger Input/Output—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input.
WDT	Output		WDT—When this pin is configured as a hardware watchdog timer pin, this signal is asserted low when the hardware watchdog timer counts down to zero. Internal Pull down resistor. This input is 5 V tolerant
TIO2	Input or Output	PLOCK Output	Timer 2 Schmitt-Trigger Input/Output—When timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer control/status register (TCSR2). If TIO2 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input .

Table 13. Timer Signal (continued)

Signal Name	Type	State during Reset	Signal Description
PLOCK	Output		PLOCK—When this pin is configured as a PLL lock pin, this signal is asserted high when the on-chip PLL enabled and locked and de-asserted when the PLL enabled and unlocked. This pin is also asserted high when the PLL is disabled. Internal Pull down resistor. This input is 5 V tolerant

4.11 JTAG/OnCE Interface

Table 14. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	Test Clock—TCK is a test clock input signal used to synchronize the JTAG test logic. Internal Pull up resistor. This input is 5 V tolerant.
TDI	Input	Input	Test Data Input—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	Test Data Output—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	Test Mode Select—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.

5 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 4.7 kΩ.

8 DC Electrical Characteristics

Table 17. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (Core_VDD) • PLL (PLLD_VDD)	V_{DD}	1.2	1.25	1.3	V
Supply voltages • I/O (IO_VDD) • PLL (PLLP_VDD) • PLL (PLLA_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Input high voltage • All pins	V_{IH}	2.0	—	V_{IO_VDD}+2V	V
Note: All 3.3-V supplies must rise prior to the rise of the 1.25-V supplies to avoid a high current condition and possible system damage.					
Input low voltage • All pins	V_{IL}	–0.3	—	0.8	V
Input leakage current	I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)	C_{IN}		4.7		pF
High impedance (off-state) input current (@ 3.46V)	I_{TSI}	–10	—	84	µA
Output high voltage • I_{OH} = -5 mA • XTAL Pin I_{OH} = -10mA	V_{OH}	2.4	—	—	V
Output low voltage • I_{OL} = 5 mA • XTAL Pin I_{OL} = 10 mA	V_{OL}	—	—	0.4	V
Internal supply current[1] (core only) at internal clock of 150 MHz • In Normal mode • In Wait mode • In Stop mode[2]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 65 16 1.2	 100 — —	 mA mA mA
Input capacitance	C_{IN}	—	—	10	pF

Note:

[1] The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.25V, V_{DD_IO} = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.30V, V_{IO_VDD}) = 3.46V at T_J = 115°C.

[2] In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

Table 19. Clock Operation (continued)

No.	Characteristics	Symbol	Min	Max	Units
Note:					

Note:

[1] Measured at 50% of the input transition.

[2] The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

[3] A valid clock signal must be applied to the EXTAL pin within 3 ms of the DSP56374 being powered up.

Table 20. Reset, Stop, Mode Select, and Interrupt Timing (continued)

No.	Characteristics	Expression	Min	Max	Unit
21	Interrupt Requests Rate[1]				
	• ESAI, ESAI_1, SHI, Timer	$12 \times T_C$	—	80.0	ns
	• DMA	$8 \times T_C$	—	53.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$8 \times T_C$	—	53.0	ns
	• $\overline{IRQ}$ (level trigger)	$12 \times T_C$	—	80.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, SHI	$6 \times T_C$	—	40.0	ns
	• Data write to ESAI, ESAI_1, SHI	$7 \times T_C$	—	46.7	ns
	• Timer	$2 \times T_C$	—	13.4	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3 \times T_C$	—	20.0	ns

Note:

[1] When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

[2] For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.

For PLL enable, (if bet 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.

[3] Periodically sampled and not 100% tested.

[4] $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
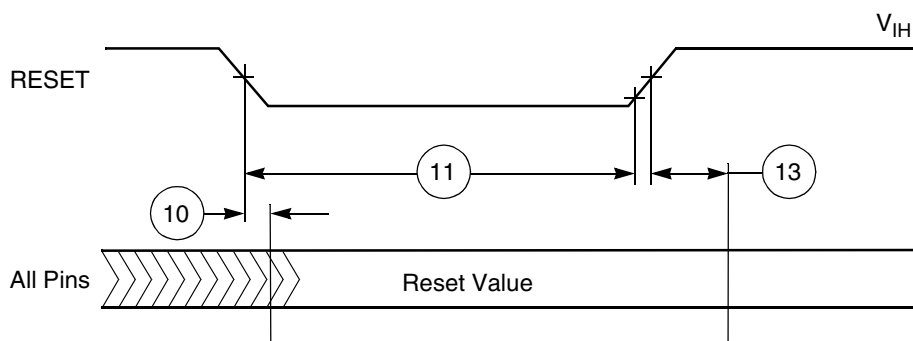
Figure 3. Reset Timing
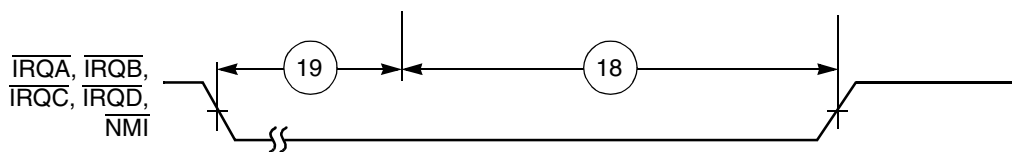
a) First Interrupt Instruction Execution
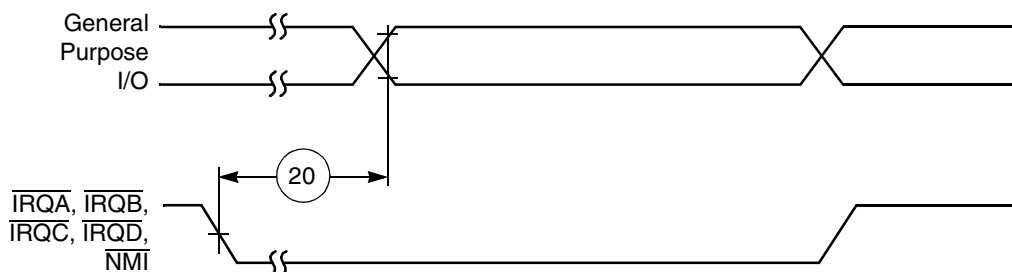
b) General Purpose I/O

Figure 4. External Fast Interrupt Timing
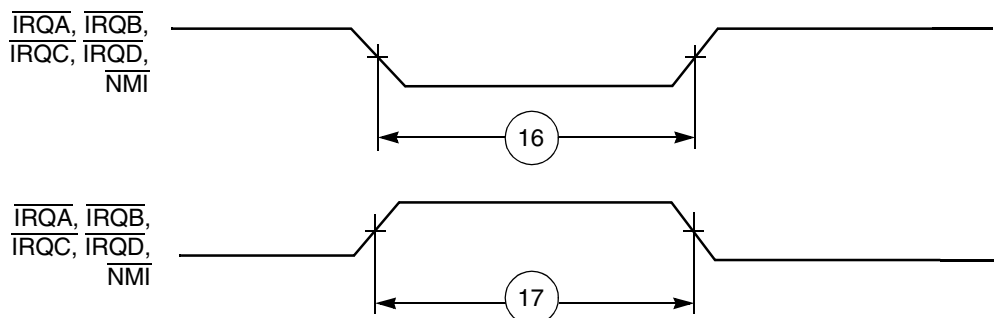
Figure 5. External Interrupt Timing (Negative Edge-Triggered)
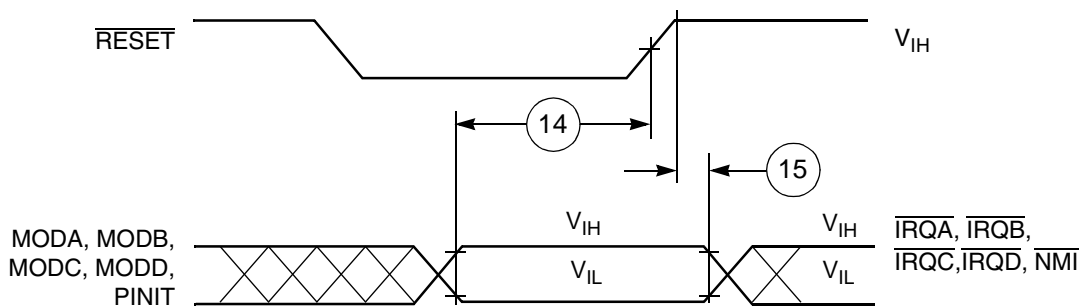
Figure 6. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

Table 22. SHI I^{2}C Protocol Timing (continued)

			Standard		Fast-Mode		Unit
No.	**Characteristics[1,2,3,4,5]**	**Symbol/ Expression**	**Min**	**Max**	**Min**	**Max**	

Note:
1. V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2. Pull-up resistor: R_P (min) = 1.5 kOhm
3. Capacitive load: C_b (max) = 50 pF
4. All times assume noise free inputs
5. All times assume internal clock frequency of 150MHz

15 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \qquad \textit{Eqn. 1}$$

where

— HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I^{2}C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \text{ (if HDM[7:0] = \$02 and HRS = 1)} \qquad \textit{Eqn. 2}$$

to

$$4096 \times T_C \text{ (if HDM[7:0] = \$FF and HRS = 0)} \qquad \textit{Eqn. 3}$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 23.

Table 23. SCL Serial Clock Cycle (T_{SCL}) Generated as Master

Nominal	$T_{I^2CCP} + 3 \times T_C + 45ns + T_R$
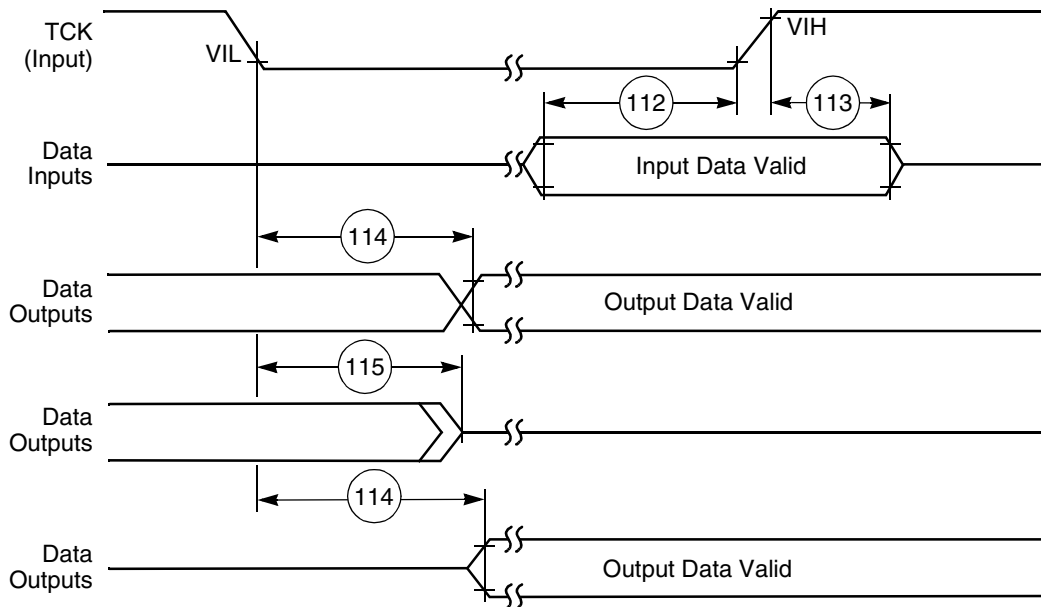
Figure 19. Debugger Port Timing Diagram
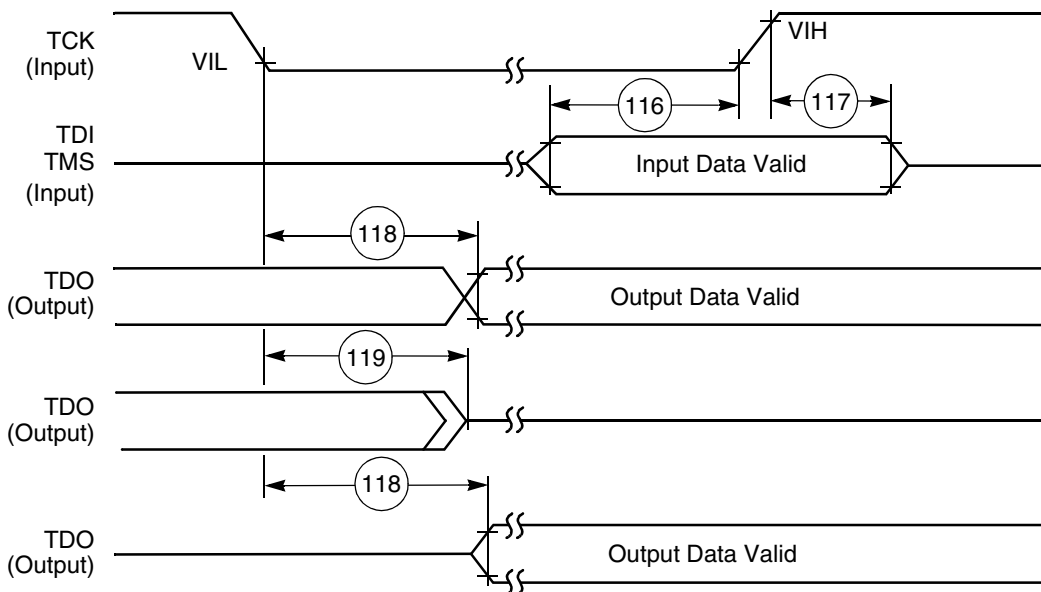
Figure 20. Test Access Port Timing Diagram

20 Watchdog Timer Timing

Table 28. Watchdog Timer Timing

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of TIO1	$2 \times T_C$	13.4	—	ns
121	Delay from timer clear to rise of TIO1	$2 \times Tc$	13.4	—	ns

Appendix A
Package Information

A.1   DSP56374 Pinout
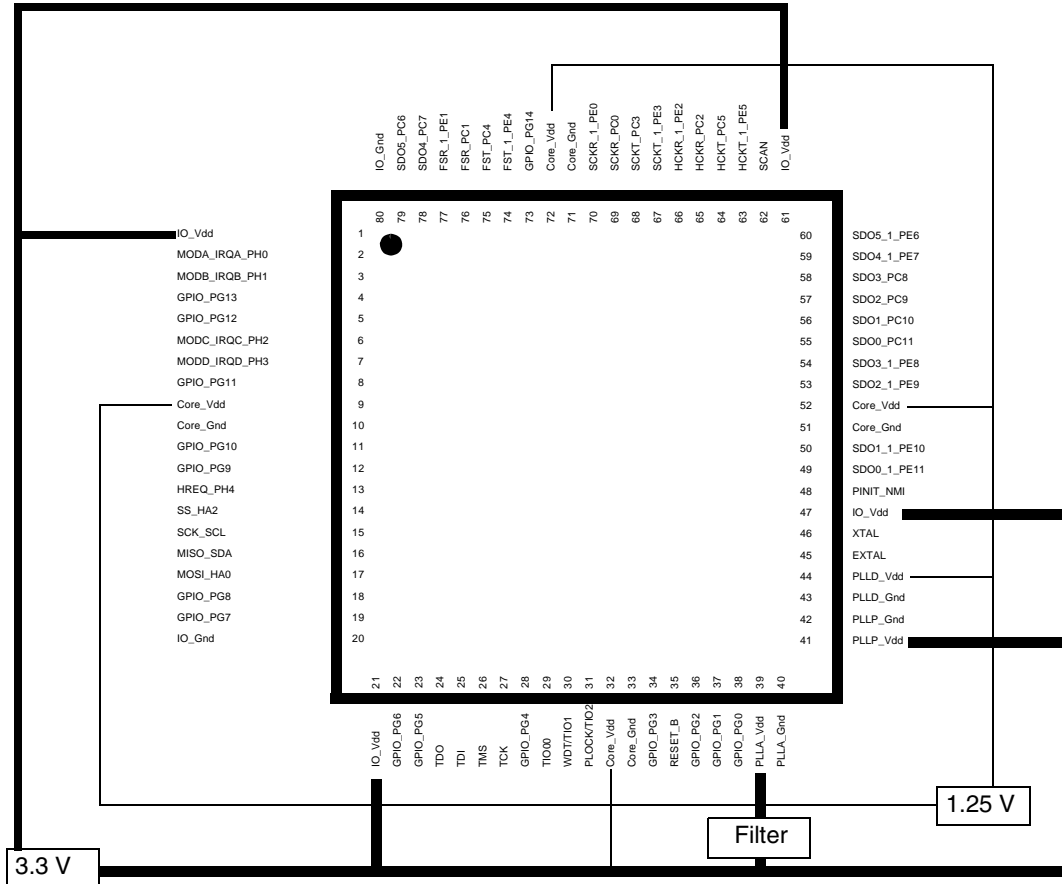
Figure A-1. 80-Pin Vdd Connections

	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23228W
freescale semiconductor		PAGE: 848D
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.	DO NOT SCALE THIS DRAWING	REV: E

NOTES

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS -L- , -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H- .

5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T- .

6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25(.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H- .

7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46(.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07(.003).

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX	DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.00 BSC		0.394 BSC						
A1	5.00 BSC		0.197 BSC						
B	10.00 BSC		0.394 BSC						
B1	5.00 BSC		0.197 BSC						
C	---	1.70	---	0.067					
C1	0.05	0.20	0.002	0.008					
C2	1.30	1.50	0.051	0.059					
D	0.20	0.40	0.008	0.016					
E	0.45	0.75	0.018	0.030					
F	0.22	0.35	0.009	0.014					
G	0.65 BSC		0.026 BSC						
J	0.07	0.20	0.003	0.008					
K	0.50 REF		0.020 REF						
R1	0.08	0.20	0.003	0.008					
S	12.00 BSC		0.472 BSC						
S1	6.00 BSC		0.236 BSC						
U	0.09	0.16	0.004	0.006					
V	12.00 BSC		0.472 BSC						
V1	6.00 BSC		0.236 BSC						
W	0.20 REF		0.008 REF						
Z	1.00 REF		0.039 REF						
θ	0°	7°	0°	7°					
θ1	0°	---	0°	---					
θ2	12° REF		12° REF						
θ3	12° REF		12° REF						

TITLE: 52LD TQFP 10 X 10 PKG, 0.65 PITCH, 1.4 THICK	CASE NUMBER: 848D-03
	STANDARD: FREESCALE
	PACKAGE CODE: 8260 SHEET: 3 OF 4

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

DSP56374
Rev. 4.2, 1/2007