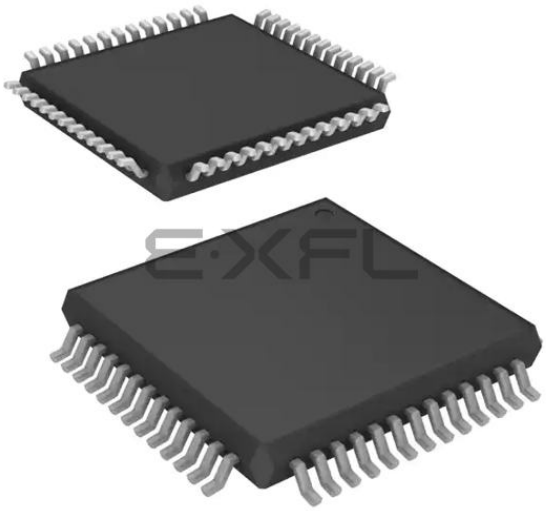


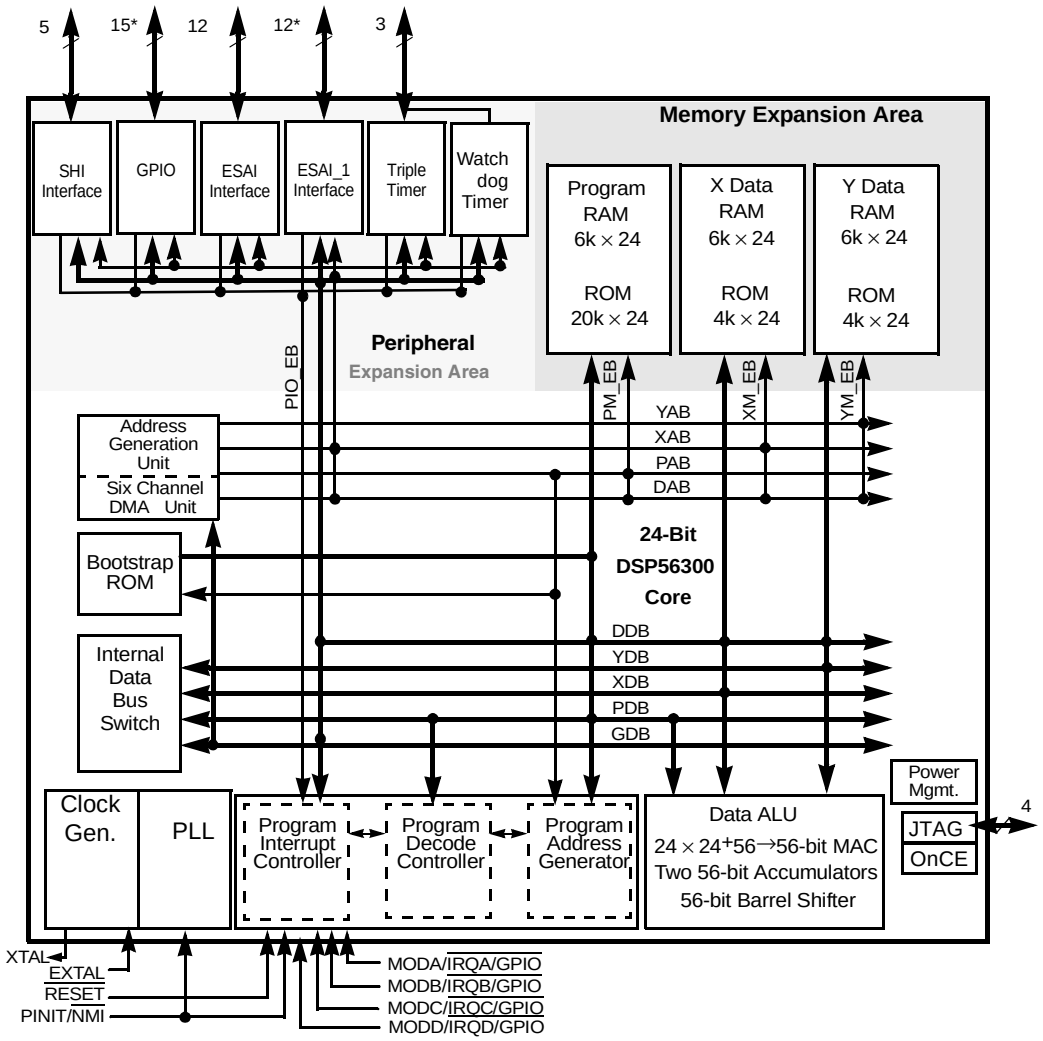
Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (84kB)
On-Chip RAM	54kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56374aec



* ESAI_1 and dedicated GPIO pins are not available in the 52-pin package.

Figure 1. DSP56374 Block Diagram

2 Features

2.1 DSP56300 Modular Chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at an internal logic supply (QVDDL) of 1.25 V
- Object Code Compatible with the 56K core
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter;16 bit arithmetic support
- Program Control with position independent code support

Table 3. DSP56374 Functional Signal Groupings (continued)

Functional Group		Number of Signals[1]	Detailed Description
Dedicated GPIO	Port G[3]	15	Table 12
Timer		3	Table 13
JTAG/OnCE Port		4	Table 14

Note:
1 Pins are not 5 V. tolerant unless noted.
2 Port H signals are the GPIO port signals which are multiplexed with the MOD and $\overline{\text{HREQ}}$ signals.
3 Port G signals are the dedicated GPIO port signals.
4 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
5 Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.

4.1 Power

Table 4. Power Inputs

Power Name	Description
PLLA_VDD (1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND. PLLA_VDD requires a filter as shown in Figure 1 and Figure 2 below. See the DSP56374 technical data sheet for additional details.
PLLP_VDD(1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_VDD (1)	PLL Power— The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_VDD (4)	Core Power—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
IO_VDD (80-pin 4) (52-pin 3)	SHI, ESAI, ESAI_1, WDT and Timer I/O Power —The voltage (3.3 V) should be well-regulated, and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, WDT and Timer I/O. The user must provide adequate external decoupling capacitors.

4.2 Ground

Table 5. Grounds

Ground Name	Description
PLLA_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND.

4.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is de-asserted, these inputs are hardware interrupt request lines.

Table 8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	MODA Input	Mode Select A/External Interrupt Request A—MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is de-asserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH0	Input, output, or disconnected		Port H0—When the MODA/IRQA is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODB/IRQB	Input	MODB Input	Mode Select B/External Interrupt Request B—MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH1	Input, output, or disconnected		Port H1—When the MODB/IRQB is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODC/IRQC	Input	MODC Input	Mode Select C/External Interrupt Request C—MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	Frame Sync for Receiver_1—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected		Port E1—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
FST_1	Input or output	GPIO disconnected	Frame Sync for Transmitter_1—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).
PE4	Input, output, or disconnected		Port E4—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2_1	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		Serial Data Input 3—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		Port E9—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1_1	Output	GPIO disconnected	Serial Data Output 1—SDO1_1 is used to transmit data from the TX1 serial transmit shift register.
PE10	Input, output, or disconnected		Port E10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1	Output	GPIO disconnected	Serial Data Output 0—SDO0_1 is used to transmit data from the TX0 serial transmit shift register.
PE11	Input, output, or disconnected		Port E11—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 15. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	−0.3 to + 1.6	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	−0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time[4]	Tr	10	ms
All “5.0V tolerant” input voltages	V_{IN}	GND − 0.3 to 6V	V
Current drain per pin excluding V_{DD} and GND(Except for pads listed below)	I	12	mA
SCK_SCL	I_{SCK}	16	mA
TDO	I_{JTAG}	24	ma
Operating temperature range[3]	T_J	80 LQFP = 105 52 LQFP = 110	°C
Storage temperature	T_{STG}	−55 to +125	°C
ESD protected voltage (Human Body Model)		2000	V
ESD protected voltage (Machine Model)		200	V

Note:
1. GND = 0 V, T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), CL = 50pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Operating temperature qualified for automotive applications. $T_J = T_A + \theta_{JA}$ x Power. Variables used were Core Current = 100 mA, I/O Current = 60 mA, Core Voltage = 1.3 V, I/O Voltage = 3.46 V, T_A = 85°C
4. If the power supply ramp to full supply time is longer than 10 ms, the POR circuitry will not operate correctly, causing erroneous operation.

6 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, the connection shown below is recommended to be made between the DSP56374 IO_VDD and Core_VDD power pins.

9 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56374 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 1.0 V and 1.8 V, respectively.

10 Internal Clocks

Table 18. INTERNAL CLOCKS[1]

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	5	—	20	MHz	Fref = FIN/NR
2	Input Clock Frequency	FIN	Fref*NR				NR is input divider value
3	Output clock Frequency (with PLL enabled)[2,3]	FOUT Tc	75 13.3	(Ef × MF x FM)/ (PDF × DF x OD)	150	MHz ns	FOUT=FVCO/NO where NO is output divider value
4	Output clock Frequency (with PLL disabled)[2,3]	FOUT	—	Ef	150	MHz	—
5	Duty Cycle	—	40	50	60	%	FVCO=300MHz~600MHz

Note:
1 See users manual for definition.
2 DF = Division Factor
Ef = External Frequency
Mf = Multiplication Factor
PDF = Predivision Factor
FM= Frequency Multiplier
OD = Output Divider
Tc = Internal Clock Period
3 Maximum frequency will vary depending on the ordered part number.

11 External Clock Operation

The DSP56374 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; an example is shown below.

Table 19. Clock Operation (continued)

No.	Characteristics	Symbol	Min	Max	Units

Note:

1 Measured at 50% of the input transition.

2 The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

3 A valid clock signal must be applied to the EXTAL pin within 3 ms of the DSP56374 being powered up.

12 Reset, Stop, Mode Select, and Interrupt Timing

Table 20. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4]				
	• Power on, external clock generator, PLL disabled	$2 \times T_C$	13.4	—	ns
	• Power on, external clock generator, PLL enabled	$2 \times T_C$	13.4	—	ns
13	Syn reset deassert delay time				
	• Minimum	$2 \times T_C$	13.4	—	ns
	• Maximum (PLL enabled)	$(2 \times T_C) + T_{LOCK}$	5.0	—	ms
14	Mode select setup time		10.0	—	ns
15	Mode select hold time		10.0	—	ns
16	Minimum edge-triggered interrupt request assertion width	$2 \times T_C$	13.4	—	ns
17	Minimum edge-triggered interrupt request deassertion width	$2 \times T_C$	13.4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_C + 5$	72	—	ns
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3]				
	• PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9 + (128 \times T_C)$	854	—	µs
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$25 \times T_C$	165	—	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9 + (128 \times T_C) + T_{LOCK}$	5.7		ms
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$(25 \times T_C) + T_{LOCK}$	5		ms
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	$10 \times T_C + 3.0$		69.0	ns

Table 20. Reset, Stop, Mode Select, and Interrupt Timing (continued)

No.	Characteristics	Expression	Min	Max	Unit
21	Interrupt Requests Rate[1]				
	• ESAI, ESAI_1, SHI, Timer	12 x T_C	—	80.0	ns
	• DMA	8 x T_C	—	53.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	8 x T_C	—	53.0	ns
	• $\overline{IRQ}$ (level trigger)	12 x T_C	—	80.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, SHI	6 x T_C	—	40.0	ns
	• Data write to ESAI, ESAI_1, SHI	7 x T_C	—	46.7	ns
	• Timer	2 x T_C	—	13.4	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	3 x T_C	—	20.0	ns

Note:

1 When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

2 For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.

For PLL enable, (if bet 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.

3 Periodically sampled and not 100% tested.

4 $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other “required $\overline{RESET}$ duration” conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

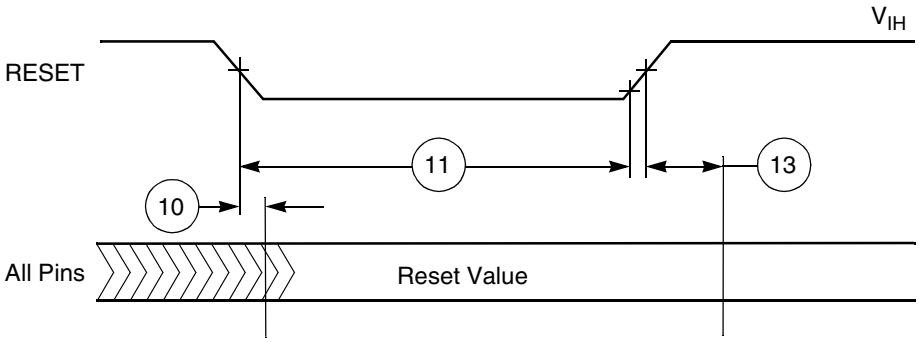


Figure 3. Reset Timing

13 Serial Host Interface SPI Protocol Timing

Table 21. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master/Slave	Bypassed	10.0 x T_C + 9	76.0	—	ns
			Very Narrow	10.0 x T_C + 9	76.0	—	ns
			Narrow	10.0 x T_C + 133	200.0	—	ns
			Wide	10.0 x T_C + 333	400.0	—	ns
XX	Tolerable Spike width on data or clock in.	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
25	Serial clock low period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
26	Serial clock rise/fall time	Master	—	—	—	—	ns
		Slave	—	—	—	5	ns
				—			

Table 21. Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	2.0 x T_C + 12.6	26	—	ns
			Very Narrow	2.0 x T_C + 2.6	16	—	ns
			Narrow	2.0 x T_C – 37.4[5]	0	—	ns
			Wide	2.0 x T_C – 87.4[5]	0	—	ns
	CPHA = 1	Slave	Bypassed	—	10	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	—	12	—	ns
			Very Narrow	—	22	—	ns
			Narrow	—	100	—	ns
			Wide	—	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	—	0	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	3.0 x T_C	20	—	ns
			Very Narrow	3.0 x T_C + 23.2	43.2	—	ns
			Narrow	3.0 x T_C + 53.2	73.2	—	ns
			Wide	3.0 x T_C + 80	100.0	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	3.0 x T_C + 26.1	—	46.2	ns
			Very Narrow	3.0 x T_C + 90.4	—	110.4	ns
			Narrow	3.0 x T_C + 116.4	—	136.4	ns
			Wide	3.0 x T_C + 203.4	—	223.4	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	2.0 x T_C	13.4	—	ns
			Very Narrow	2.0 x T_C + 1.6	15	—	ns
			Narrow	2.0 x T_C + 41.6	55	—	ns
			Wide	2.0 x T_C + 91.6	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	12.0	ns

Table 21. Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
36	SCK edge following the first SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	3.0 x T_C + 30	50	—	ns
			Very Narrow	3.0 x T_C + 40	60	—	ns
			Narrow	3.0 x T_C + 80	100	—	ns
			Wide	3.0 x T_C + 120	150	—	ns
37	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	4.0 x T_C	57.0	—	ns
			Very Narrow	4.0 x T_C	67.0	—	ns
			Narrow	4.0 x T_C	107.0	—	ns
			Wide	4.0 x T_C	157.0	—	ns
38	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	—	3.0 x T_C + 30	50.0	—	ns
39	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	—	2.0 x T_C	13.4	—	ns
40	$\overline{\text{HREQ}}$ in assertion to first SCK edge	Master	Bypassed	0.5 x T_{SPICC} + 3.0 x T_C + 5	63	—	ns
			Very Narrow	0.5 x T_{SPICC} + 3.0 x T_C + 5	63	—	ns
			Narrow	0.5 x T_{SPICC} + 3.0 x T_C + 5	125	—	ns
			Wide	0.5 x T_{SPICC} + 3.0 x T_C + 5	225	—	ns
41	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	—	—	0	—	ns
42	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	—	—	0	—	ns
43	$\overline{\text{HREQ}}$ assertion width	Master	—	3.0 x T_C	20	—	ns

Note:

1 V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2 Periodically sampled, not 100% tested
3 All times assume noise free inputs.
4 All times assume internal clock frequency of 150 MHz.
5 Equation applies when the result is positive T_C.

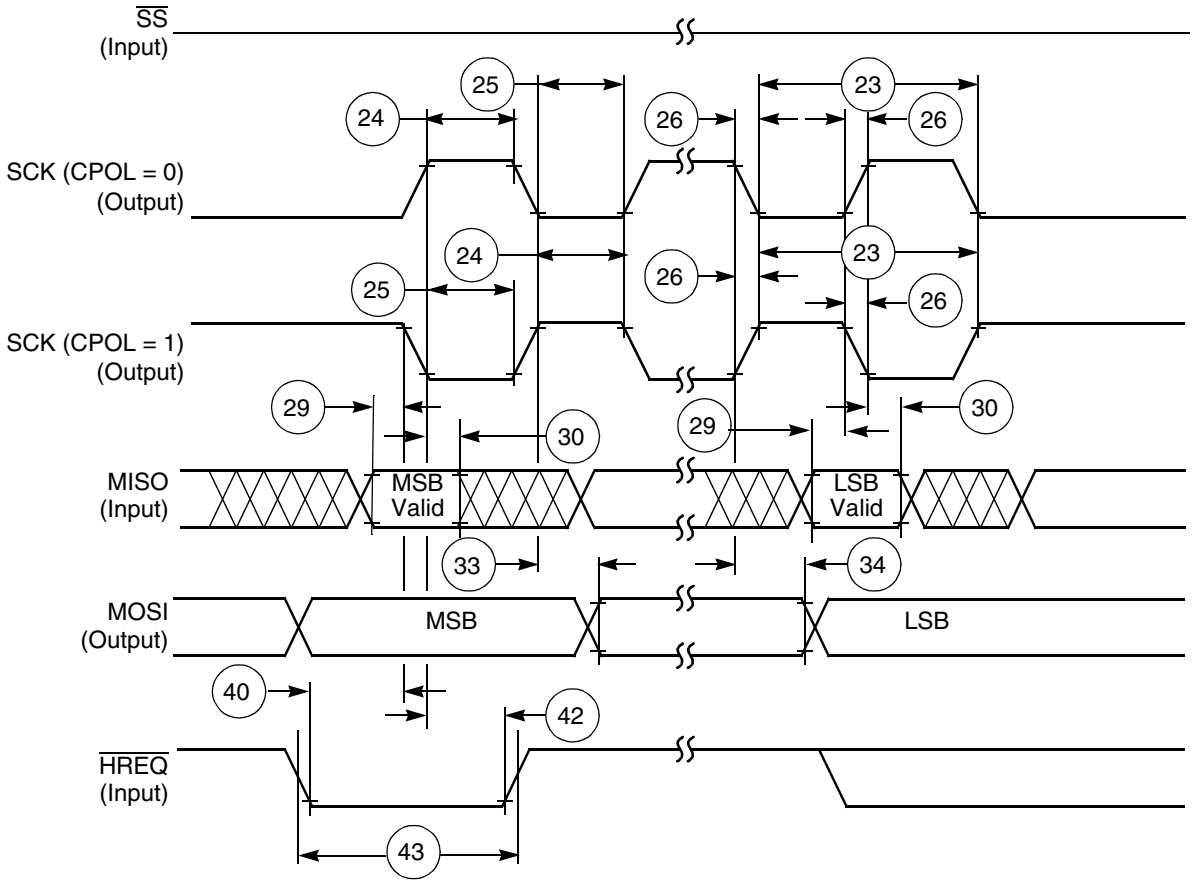


Figure 7. SPI Master Timing (CPHA = 0)

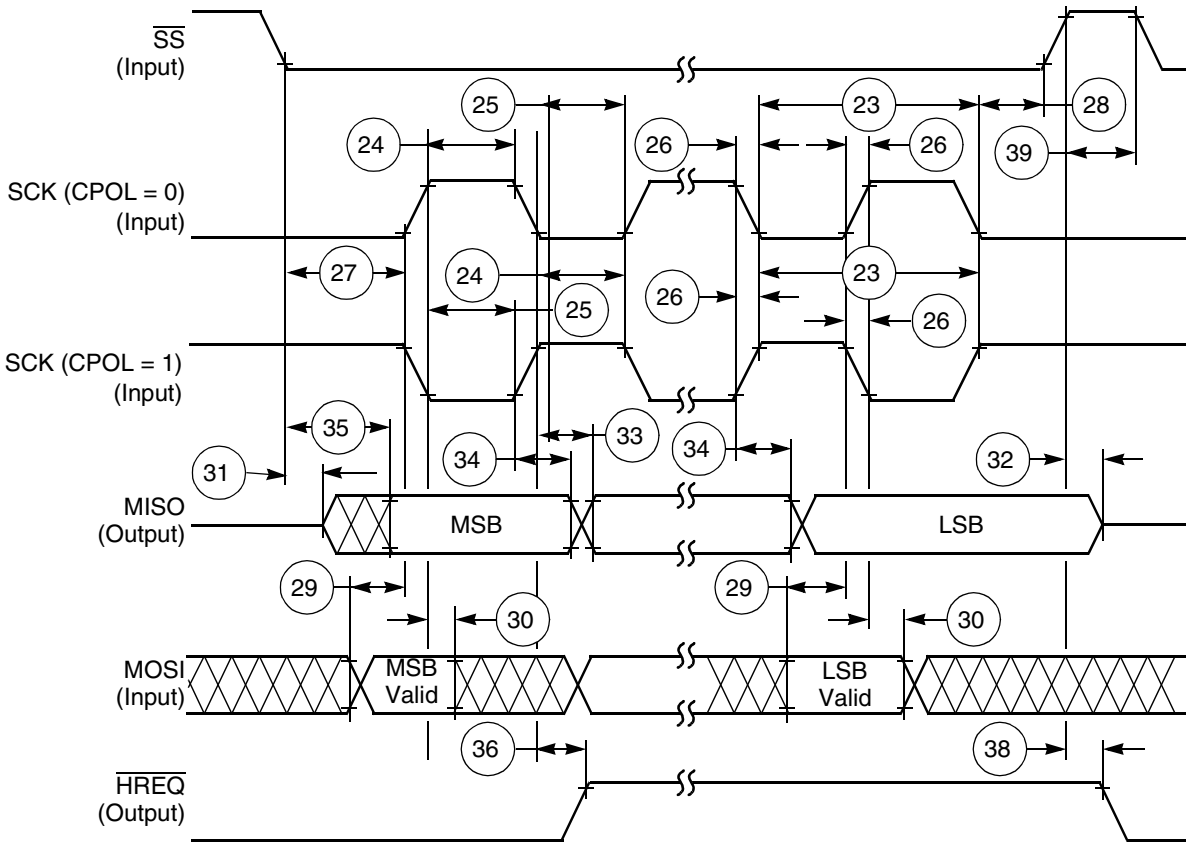


Figure 9. SPI Slave Timing (CPHA = 0)

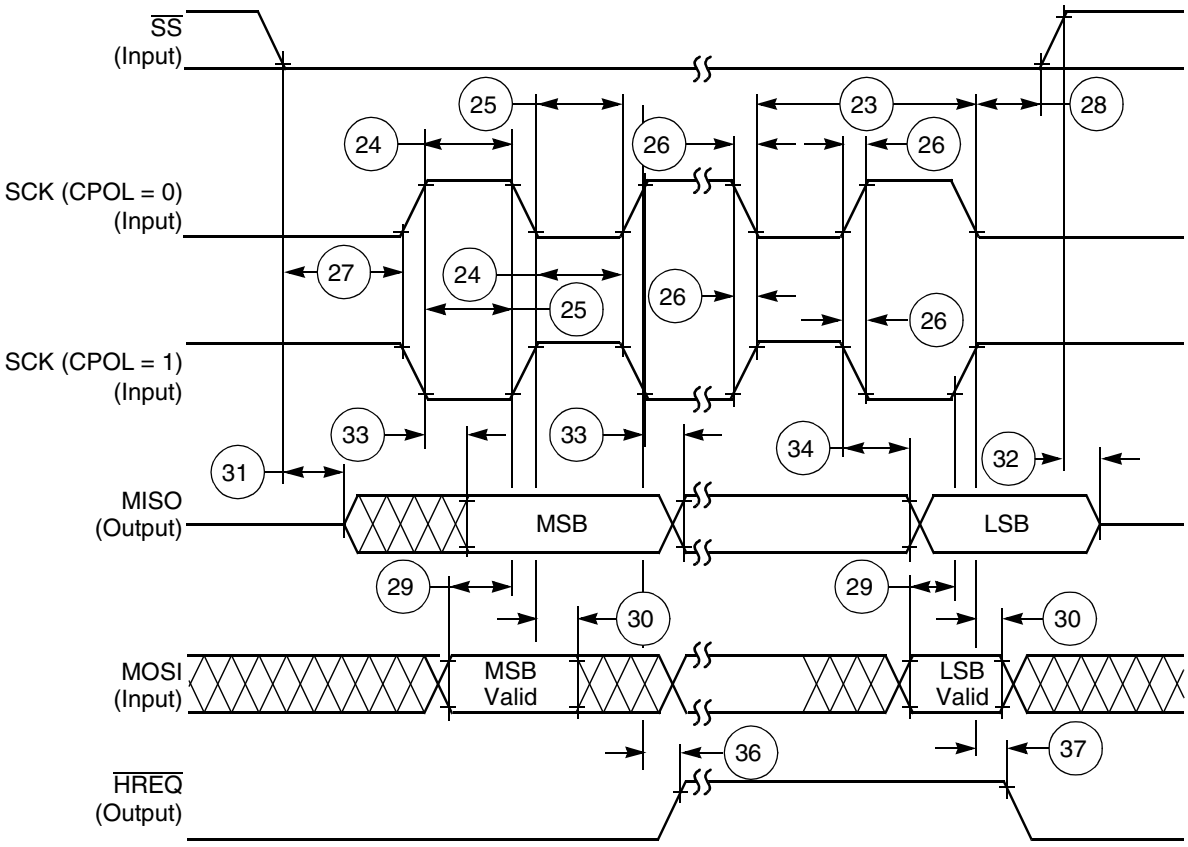
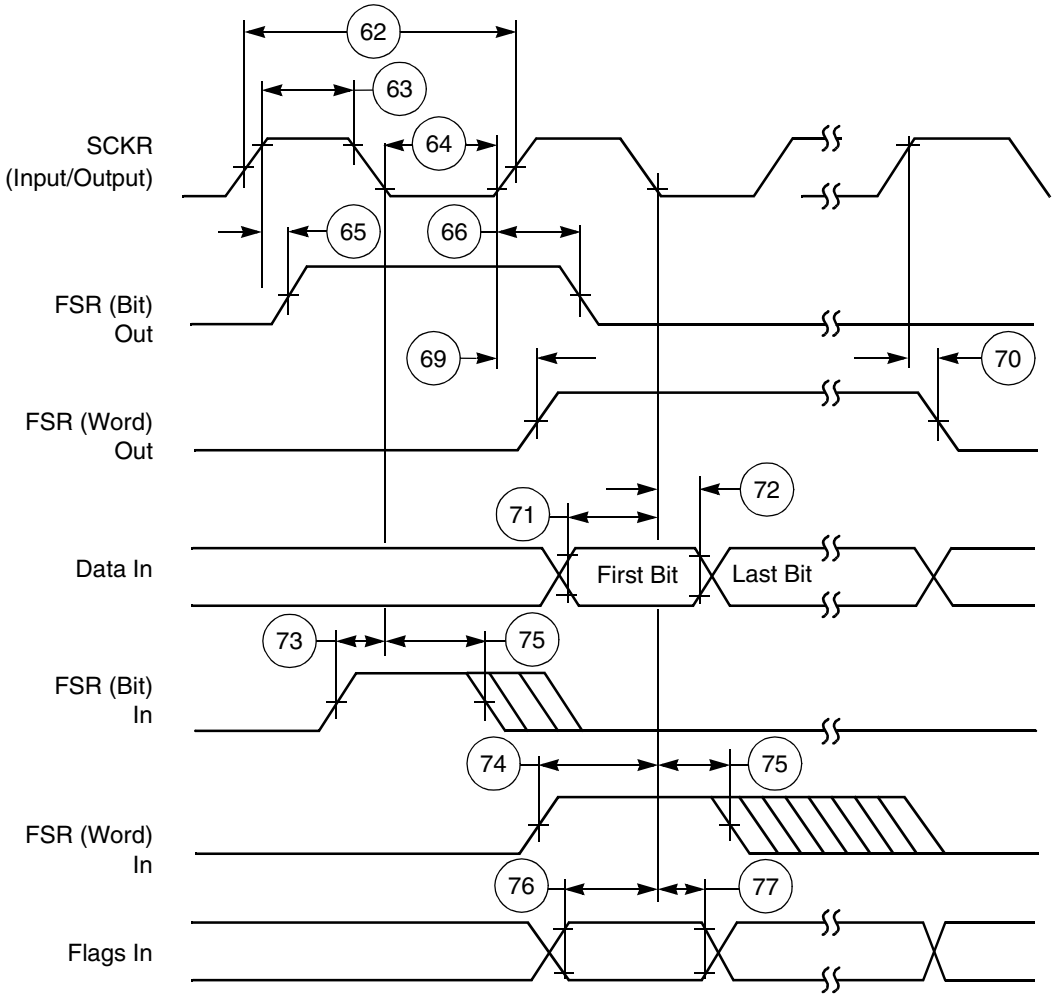


Figure 10. SPI Slave Timing (CPHA = 1)

14 Serial Host Interface (SHI) I2C Protocol Timing

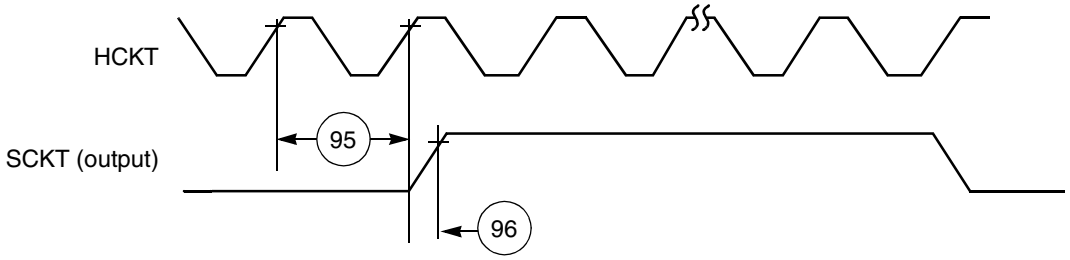
Table 22. SHI I2C Protocol Timing

Standard I2C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
XX	Tolerable Spike Width on SCL or SDA	—					
	Filters Bypassed		—	0	—	0	ns
	Very Narrow Filters enabled		—	10	—	10	ns
	Narrow Filters enabled		—	50	—	50	ns
	Wide Fileters enabled.		—	100	—	100	ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs



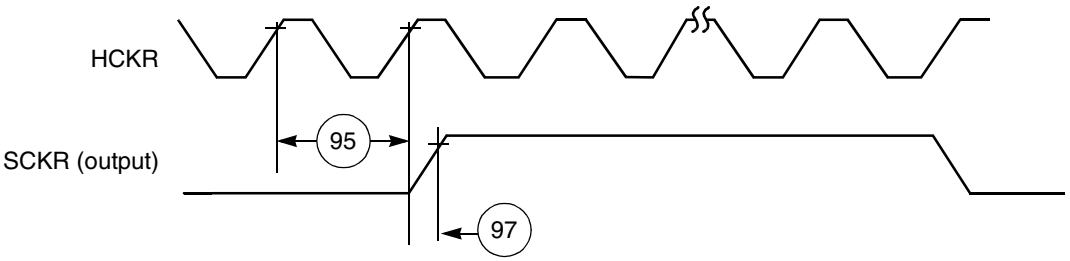
Note: Figure 13 is drawn assuming positive polarity bit clock (RCKP=0) and positive frame sync polarity (RFSP=0).

Figure 13. ESAI Receiver Timing



Note: Figure 14 is drawn assuming positive polarity high frequency clock (THCKP=0) and positive bit clock polarity (TCKP=0).

Figure 14. ESAI HCKT Timing



Note: Figure 15 is drawn assuming positive polarity high frequency clock (RHCKP=0) and positive bit clock polarity (RCKP=0).

Figure 15. ESAI HCKR Timing

17 Timer Timing

Table 25. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
99	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note: V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF					

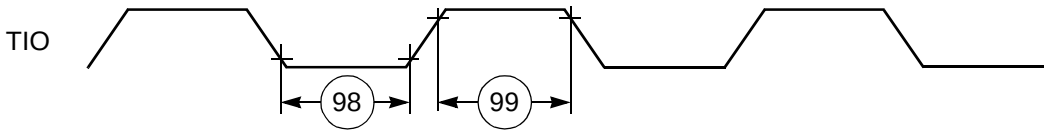


Figure 16. TIO Timer Event Input Restrictions

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4