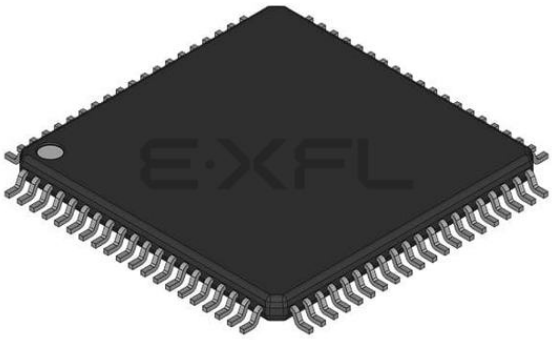

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (84kB)
On-Chip RAM	54kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dspb56374afc

(DMA). The DSP56374 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock.

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/ Symbol	Logic State	Signal State	Voltage*
PIN	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

- Hardware Watchdog Timer

2.4 Packages

80-pin and 52-pin plastic LQFP packages.

3 Documentation

Table 2 lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 2. DSP56374 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56374 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56374UM/D
DSP56374 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56374
DSP56374 Product Brief	Brief description of the chip	DSP56374PB/D

4 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 3.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 3. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals[1]	Detailed Description
Power (V_{DD})		11	Table 15
Ground (GND)		9	Table 5
Scan Pins		1	Table 6
Clock and PLL		3	Table 7
Interrupt and mode control	Port H[2]	5	Table 8
SHI	Port H[2]	5	Table 9
ESAI	Port C[4]	12	Table 10
ESAI_1	Port E[5]	12	Table 11

4.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is de-asserted, these inputs are hardware interrupt request lines.

Table 8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	MODA Input	Mode Select A/External Interrupt Request A—MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is de-asserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH0	Input, output, or disconnected		Port H0—When the MODA/IRQA is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODB/IRQB	Input	MODB Input	Mode Select B/External Interrupt Request B—MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH1	Input, output, or disconnected		Port H1—When the MODB/IRQB is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODC/IRQC	Input	MODC Input	Mode Select C/External Interrupt Request C—MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 8. Interrupt and Mode Control (continued)

Signal Name	Type	State during Reset	Signal Description
PH2	Input, output, or disconnected		Port H2—When the MODC/IRQC is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODD/$\overline{\text{IRQD}}$	Input	MODD Input	Mode Select D/External Interrupt Request D—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH3	Input, output, or disconnected		Port H3—When the MODD/IRQD is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
RESET	Input	Input	Reset—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is de-asserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.6 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		I^2C Serial Clock—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through an external pull-up resistor according to the I^2C specifications. This signal is tri-stated during hardware, software, and individual reset. This pin has an internal pull up resistor. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is de-asserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		I^2C Data and Acknowledge—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.7 Enhanced Serial Audio Interface

Table 10. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected		Port C2—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.
HCKT	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected		Port C5—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	Receiver Serial Clock—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		Port C0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	Transmitter Serial Clock—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		Port C3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5	Output	GPIO disconnected	Serial Data Output 5—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		Serial Data Input 0—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		Port C6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	Serial Data Output 4—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		Serial Data Input 1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		Port C7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		Port C8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.8 Enhanced Serial Audio Interface_1

Table 11. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		Port E2—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT_1	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		Port E5—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.9 Dedicated GPIO-Port G

Table 12. Dedicated GPIO-Port G Signals

Signal Name	Type	State During Reset	Signal Description
PG0	Input, output, or disconnected	GPIO disconnected	Port G0—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG1	Input, output, or disconnected	GPIO disconnected	Port G1—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG2	Input, output, or disconnected	GPIO disconnected	Port G2—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG3	Input, output, or disconnected	GPIO disconnected	Port G3—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG4	Input, output, or disconnected	GPIO disconnected	Port G4—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG5	Input, output, or disconnected	GPIO disconnected	Port G5—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG6	Input, output, or disconnected	GPIO disconnected	Port G6—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG7	Input, output, or disconnected	GPIO disconnected	Port G7—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG8	Input, output, or disconnected	GPIO disconnected	Port G8—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 13. Timer Signal (continued)

Signal Name	Type	State during Reset	Signal Description
PLOCK	Output		PLOCK—When this pin is configured as a PLL lock pin, this signal is asserted high when the on-chip PLL enabled and locked and de-asserted when the PLL enabled and unlocked. This pin is also asserted high when the PLL is disabled. Internal Pull down resistor. This input is 5 V tolerant

4.11 JTAG/OnCE Interface

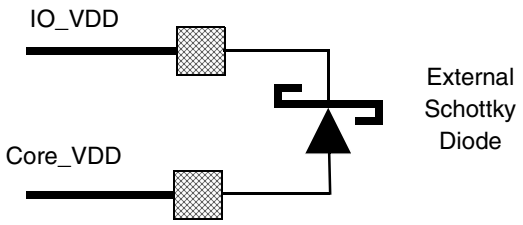
Table 14. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	Test Clock—TCK is a test clock input signal used to synchronize the JTAG test logic. Internal Pull up resistor. This input is 5 V tolerant.
TDI	Input	Input	Test Data Input—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	Test Data Output—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	Test Mode Select—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.

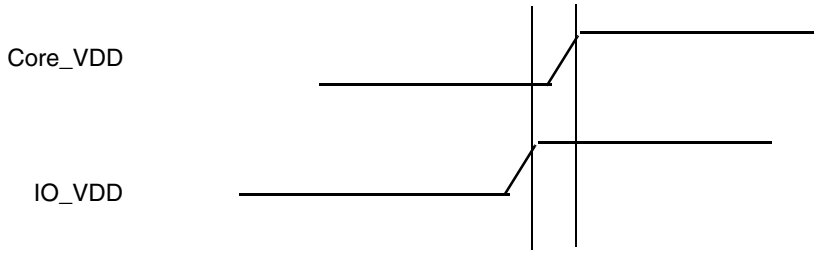
5 Maximum Ratings

CAUTION

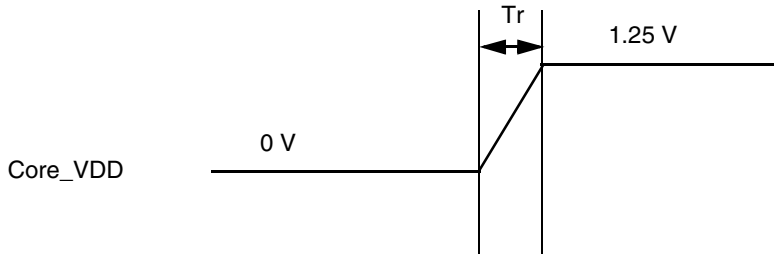
This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 4.7 kΩ.



To prevent a high current condition upon power up, the IO_VDD must be applied ahead of the Core_VDD as shown below if the external Schottky is not used.



For correct operation of the internal power on reset logic, the Core_VDD ramp rate (Tr) to full supply must be less than 10 ms. This is shown below.



7 Thermal Characteristics

Table 16. Thermal Characteristics

Characteristic	Symbol	LQFP Values	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	$R_{\theta JA}$ or θ_{JA}	68 (52 LQFP) 50 (80 LQFP)	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	17 (52 LQFP) 11 (80 LQFP)	°C/W

Note:
1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

13 Serial Host Interface SPI Protocol Timing

Table 21. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master/Slave	Bypassed	10.0 x T_C + 9	76.0	—	ns
			Very Narrow	10.0 x T_C + 9	76.0	—	ns
			Narrow	10.0 x T_C + 133	200.0	—	ns
			Wide	10.0 x T_C + 333	400.0	—	ns
XX	Tolerable Spike width on data or clock in.	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
25	Serial clock low period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
26	Serial clock rise/fall time	Master	—	—	—	—	ns
		Slave	—	—	—	5	ns
				—			

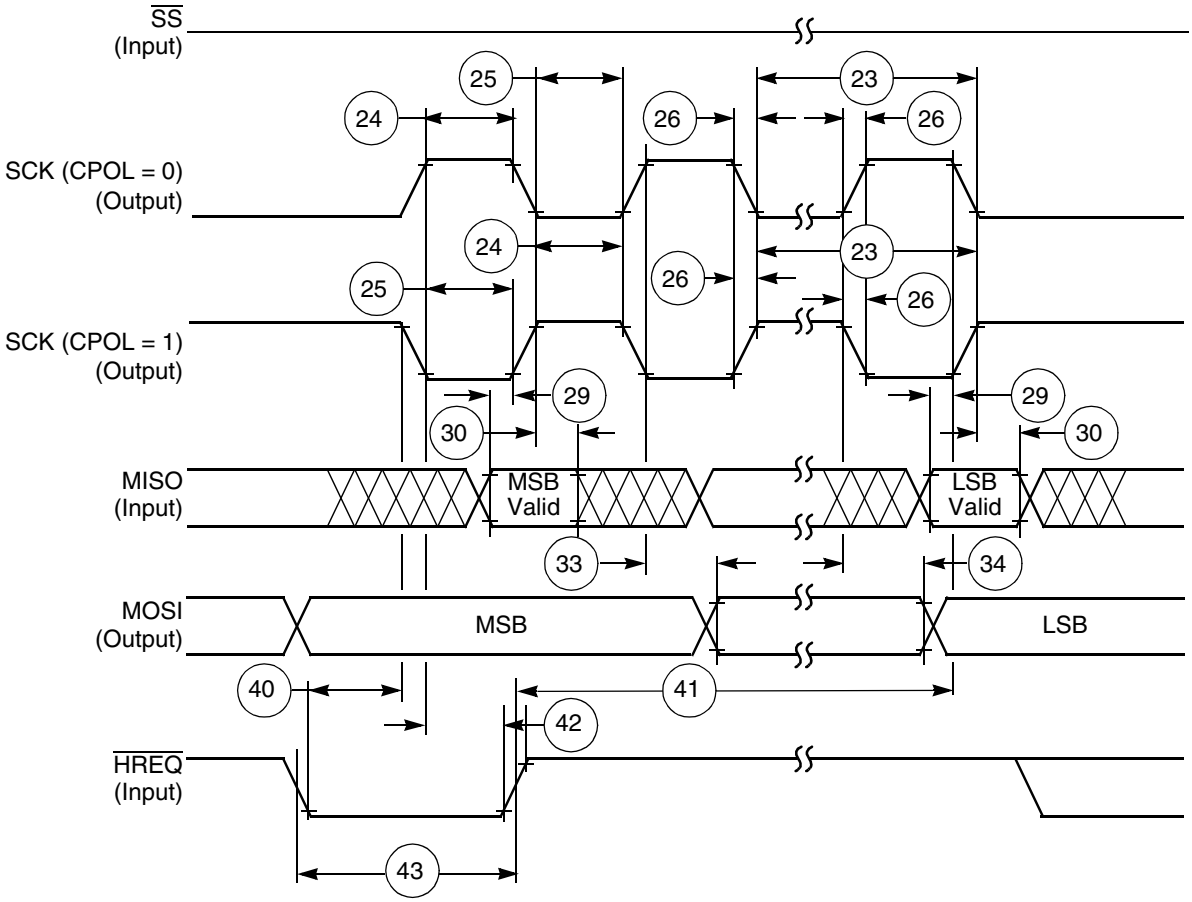


Figure 8. SPI Master Timing (CPHA = 1)

Table 22. SHI I²C Protocol Timing (continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time	T_R	—	5.0	—	5.0	ns
51	SCL and SDA fall time	T_F	—	5.0	—	5.0	ns
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency	F_{OSC}					
	• Filters bypassed		10.6	—	28.5	—	MHz
	• Very Narrrow filters enabled		10.6	—	28.5	—	MHz
	• Narrow filters enabled		11.8	—	39.7	—	MHz
	• Wide filters enabled		13.1	—	61.0	—	MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{HREQ}$ output deassertion[2]	$T_{NG;RQO}$					
	• Filters bypassed	$4 \times T_C + 30$	—	57.0	—	57.0	ns
	• Very Narrow filters enabled	$4 \times T_C + 50$	—	77.0	—	67.0	ns
	• Narrow filters enabled	$4 \times T_C + 130$	—	157.0	—	157.0	ns
	• Wide filters enabled	$4 \times T_C + 230$	—	257.0	—	257.0	ns
59	Last SCL edge to $\overline{HREQ}$ output not deasserted[2]	$T_{AS;RQO}$					
	• Filters bypassed	$2 \times T_C + 30$	44	—	44	—	ns
	• Very Narrow filters enabled	$2 \times T_C + 40$	54	—	54	—	ns
	• Narrow filters enabled	$2 \times T_C + 80$	94	—	94	—	ns
	• Wide filters enabled	$2 \times T_C + 130$	144	—	144	—	ns
60	$\overline{HREQ}$ in assertion to first SCL edge	$T_{AS;RQI}$					
	• Filters bypassed		4327	—	927	—	ns
	• Very Narrow filters enabled		4317	—	917	—	ns
	• Narrow filters enabled		4282	—	877	—	ns
	• Wide filters enabled		4227	—	827	—	ns
61	First SCL edge to $\overline{HREQ}$ is not asserted ($\overline{HREQ}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Table 24. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
88	SCKT edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT edge[6]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT edge	—	—	4.0 5.0	— —	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	13.4	—		ns
96	HCKT input edge to SCKT output	—	—	—	18.0		ns
97	HCKR input edge to SCKR output	—	—	—	18.0		ns

Note:

1 V_{CORE_VDD} = 1.25 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

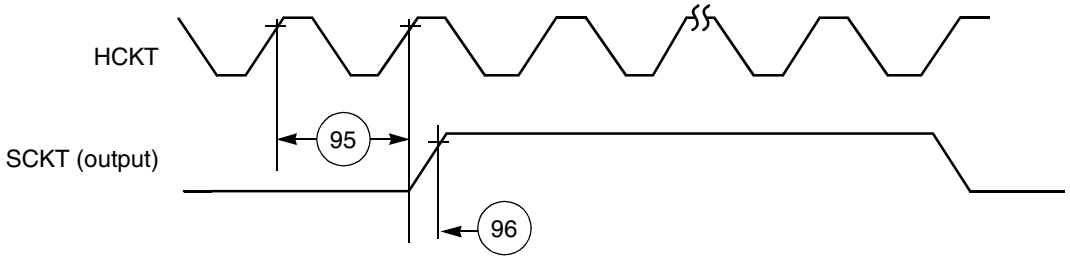
4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.

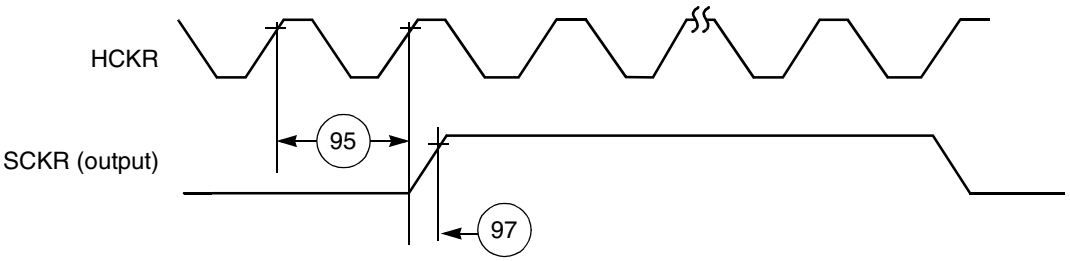
7 Periodically sampled and not 100% tested.

8 ESAI_1 specs match those of ESAI.



Note: Figure 14 is drawn assuming positive polarity high frequency clock (THCKP=0) and positive bit clock polarity (TCKP=0).

Figure 14. ESAI HCKT Timing



Note: Figure 15 is drawn assuming positive polarity high frequency clock (RHCKP=0) and positive bit clock polarity (RCKP=0).

Figure 15. ESAI HCKR Timing

17 Timer Timing

Table 25. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
99	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note: V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF					

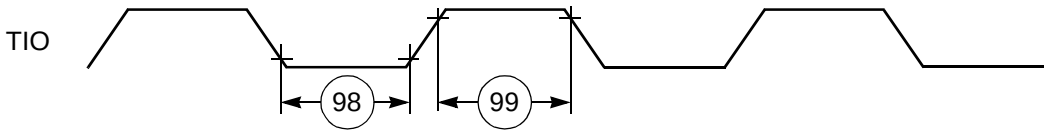


Figure 16. TIO Timer Event Input Restrictions

18 GPIO Timing

Table 26. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
100	EXTAL edge to GPIO out valid (GPIO out delay time)[2]		—	7	ns
101	EXTAL edge to GPIO out not valid (GPIO out hold time)[2]		—	7	ns
102	GPIO In valid to EXTAL edge (GPIO in set-up time)[2]		2	—	ns
103	EXTAL edge to GPIO in not valid (GPIO in hold time)[2]		0	—	ns
104	Minimum GPIO pulse high width	$T_C + 13$	19.7	—	ns
105	Minimum GPIO pulse low width	$T_C + 13$	19.7	—	ns
106	GPIO out rise time	—	—	13.0	ns
107	GPIO out fall time	—	—	13.0	ns

Note:
1 V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2 PLL Disabled, EXTAL driven by a square wave.

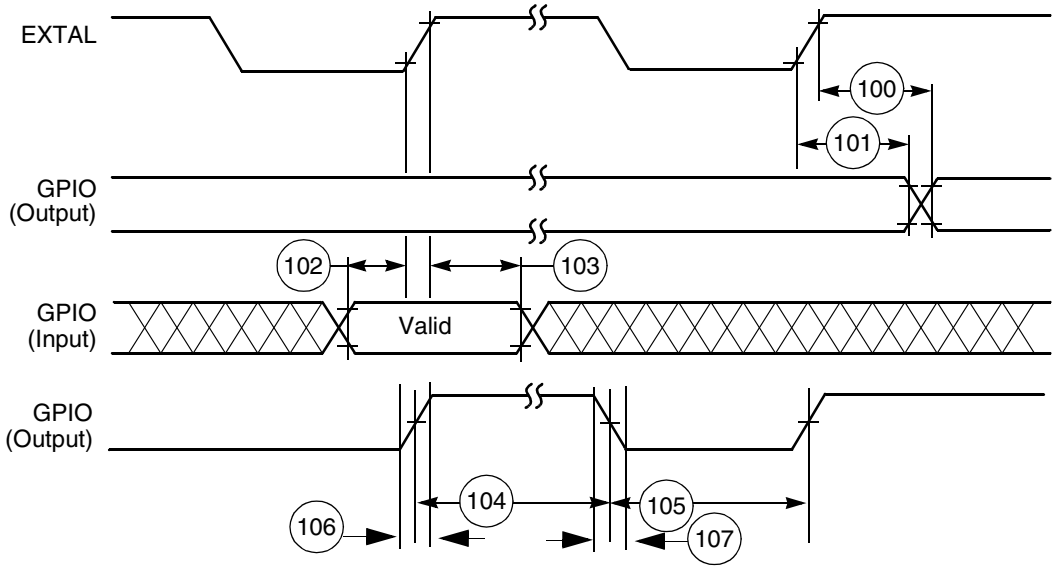


Figure 17. GPIO Timing

19 JTAG Timing

Table 27. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
108	TCK frequency of operation (1/($T_C \times 3$); maximum 10 MHz)	—	10.0	MHz

How to Reach Us:

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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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