Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8), 16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f35l23jfe-u0

1.2 Specifications

Table 1.1 to Table 1.4 list specifications of the M16C/5L Group, M16C/56 Group.

Table 1.1 Specifications (80-pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits)) • Basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V) • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash	See Table 1.5 and Table 1.6.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 71 CMOS inputs/outputs, a pull-up resistor selectable
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 41 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART4	4 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I^2C-bus, IEBus)
Multi-master I^2C-bus Interface		1 channel
A/D Converter		10-bit resolution × 27 channels

Table 1.2 Specifications (80-pin Package) (2/2)

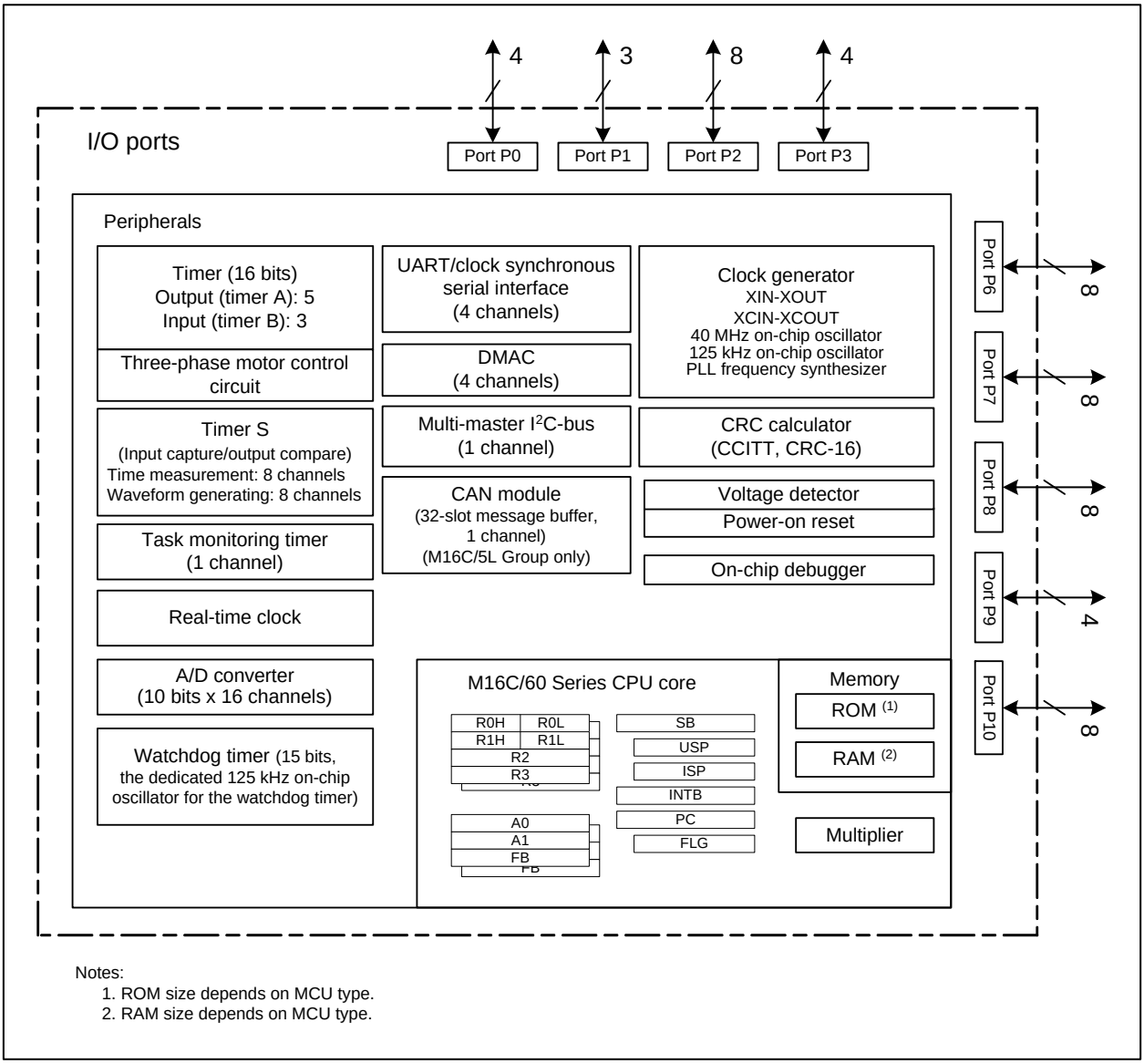
Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
CAN Module		32-slot message buffer × 1 channel (M16C/5L Group only)
Flash Memory		• Programming and erasure supply voltage: 3.0 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 5. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		80-pin plastic mold LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Note:

1. Refer to Table 1.5 “Product List of M16C/5L Group” and Table 1.6 “Product List of M16C/56 Group” for the Operating Temperature.

Table 1.3 Specifications (64-pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits)) • Basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V) • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash	See Table 1.5 and Table 1.6.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 55 CMOS inputs/outputs, a pull-up resistor selectable
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 39 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART3	3 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I^2C-bus, IEBus)
Multi-master I^2C-bus Interface		1 channel
A/D Converter		10-bit resolution × 16 channels



Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.4 64-Pin Block Diagram

Table 1.7 Pin Names, 80-Pin Package (1/2)

Pin No.	Control pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I²C-bus pin	Analog Pin
1		P9_5				CLK4		AN2_5
2		P9_3				CTX0 (1)		AN2_4
3		P9_2		TB2IN		CRX0 (1)		AN3_2
4		P9_1		TB1IN				AN3_1
5	CLKOUT	P9_0		TB0IN				AN3_0
6	CNVSS							
7	XCIN	P8_7						
8	XCOUT	P8_6						
9	$\overline{\text{RESET}}$							
10	XOUT							
11	VSS							
12	XIN							
13	VCC							
14		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP				
16		P8_3	$\overline{\text{INT1}}$					
17		P8_2	$\overline{\text{INT0}}$					
18		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
19		P8_0		TA4OUT/U	TSUDA			
20		P7_7		TA3IN				
21		P7_6		TA3OUT				
22		P7_5		TA2IN/$\overline{\text{W}}$				
23		P7_4		TA2OUT/W				
24		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
25		P7_2		TA1OUT/V		CLK2/RXD1		
26		P7_1		TA0IN		RXD2/SCL2/CLK1		
27		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
28		P6_7				TXD1		
29		P6_6				RXD1		
30		P6_5				CLK1		
31		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
32		P3_7						
33		P3_6						
34		P3_5						
35		P3_4						
36		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$		
37		P3_2				TXD3		
38		P3_1				RXD3		
39		P3_0				CLK3		
40		P6_3				TXD0		

Note 1. There are pins CTX0 and CRX0 only in the M16C/5L Group

1.6 Pin Functions

Table 1.11 Pin Functions (64-Pin and 80-Pin Packages) (1/2)

Signal Name	Pin Name	I/O	Description
Power supply	VCC, VSS	I	Apply 3.0 to 5.5 V to VCC pin and 0 V to VSS pin.
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. Pins AVCC and AVSS should be connected to VCC and VSS, respectively.
Reset input	$\overline{\text{RESET}}$	I	Driving this low resets the MCU.
CNVSS	CNVSS	I	Connect to VSS via a resistor.
Main clock input	XIN	I	Input/output for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. (1) To apply an external clock, connect it to XIN and leave XOUT open. When XIN is not used, connect XIN to VCC pin and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT. (1)
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	This pin outputs the clock having the same frequency as f1, f8, f32, or fC.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input for $\overline{\text{INT}}$ interrupt.
$\overline{\text{NMI}}$ input	$\overline{\text{NMI}}$	I	Input for $\overline{\text{NMI}}$ interrupt.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
	ZP	I	Input for Z-phase
Timer B	TB0IN to TB2IN	I	Timers B0 to B2 input
Three-phase motor control timer	U,$\overline{\text{U}}$,V,$\overline{\text{V}}$,W,$\overline{\text{W}}$	O	Output for three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I	Input for three-phase motor control timer
Real-time clock	RTCOUT	O	Output for real-time clock
Serial interface UART0 to UART3	$\overline{\text{CTS0}}$ to $\overline{\text{CTS3}}$	I	Input to control data transmission
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS3}}$	O	Output to control data reception
	CLK0 to CLK3	I/O	Transfer clock input/output
	RXD0 to RXD3	I	Serial data input
	TXD0 to TXD3	O	Serial data output
UART2 I^2C mode	SDA2	I/O	Serial data input/output
	SCL2	I/O	Transfer clock input/output
Multi-master I^2C-bus	SDAMM	I/O	Serial data input/output
	SCLMM		Transfer clock input/output

Note:
1. Please contact the manufacturer of crystal/ceramic resonator for oscillation characteristic.

Table 1.13 Pin Functions (80-Pin Package Only)

Signal Name	Pin Name	I/O	Description
Serial interface UART4	CLK4	I/O	Transfer clock I/O pin
	RXD4	I	Serial data input pin
	TXD4	O	Serial data output pin
A/D converter	AN0_4 to AN0_7 AN2_0 to AN2_3 AN2_5 to AN2_7	I	Analog input
I/O port	P0_4 to P0_7 P1_0 to P1_4 P3_4 to P3_7 P9_5 to P9_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, Pull-up resistor is selectable for every unit of 4 bits.

Table 4.18 SFR Information (18) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	000X 0000b
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.24 SFR Information (24) (1)

Address	Register	Symbol	Reset Value
D5F0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXh
D5F1h			XXh
D5F2h			XXh
D5F3h			XXh
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		XXh
D5F6h	CAN0 Mailbox 15: Data Field		XXh
D5F7h			XXh
D5F8h			XXh
D5F9h			XXh
D5FAh			XXh
D5FBh			XXh
D5FCh			XXh
D5FDh			XXh
D5FEh	CAN0 Mailbox 15: Time Stamp		XXh
D5FFh			XXh
D600h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXh
D601h			XXh
D602h			XXh
D603h			XXh
D604h			
D605h	CAN0 Mailbox 16: Data Length		XXh
D606h	CAN0 Mailbox 16: Data Field		XXh
D607h			XXh
D608h			XXh
D609h			XXh
D60Ah			XXh
D60Bh			XXh
D60Ch			XXh
D60Dh			XXh
D60Eh	CAN0 Mailbox 16: Time Stamp		XXh
D60Fh			XXh
D610h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXh
D611h			XXh
D612h			XXh
D613h			XXh
D614h			
D615h	CAN0 Mailbox 17: Data Length		XXh
D616h	CAN0 Mailbox 17: Data Field		XXh
D617h			XXh
D618h			XXh
D619h			XXh
D61Ah			XXh
D61Bh			XXh
D61Ch			XXh
D61Dh			XXh
D61Eh	CAN0 Mailbox 17: Time Stamp		XXh
D61Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.30 SFR Information (30) (1)

Address	Register	Symbol	Reset Value
D710h	CAN0 Mask Register 4	C0MKR4	XXh
D711h			XXh
D712h			XXh
D713h			XXh
D714h	CAN0 Mask Register 5	C0MKR5	XXh
D715h			XXh
D716h			XXh
D717h			XXh
D718h	CAN0 Mask Register 6	C0MKR6	XXh
D719h			XXh
D71Ah			XXh
D71Bh			XXh
D71Ch	CAN0 Mask Register 7	C0MKR7	XXh
D71Dh			XXh
D71Eh			XXh
D71Fh			XXh
D720h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXh
D721h			XXh
D722h			XXh
D723h			XXh
D724h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXh
D725h			XXh
D726h			XXh
D727h			XXh
D728h	CAN0 Mask Invalid Register	C0MKIVLR	XXh
D729h			XXh
D72Ah			XXh
D72Bh			XXh
D72Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXh
D72Dh			XXh
D72Eh			XXh
D72Fh			XXh
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	C0MCTL0	00h
D7A1h	CAN0 Message Control Register 1	C0MCTL1	00h
D7A2h	CAN0 Message Control Register 2	C0MCTL2	00h
D7A3h	CAN0 Message Control Register 3	C0MCTL3	00h
D7A4h	CAN0 Message Control Register 4	C0MCTL4	00h
D7A5h	CAN0 Message Control Register 5	C0MCTL5	00h
D7A6h	CAN0 Message Control Register 6	C0MCTL6	00h
D7A7h	CAN0 Message Control Register 7	C0MCTL7	00h
D7A8h	CAN0 Message Control Register 8	C0MCTL8	00h
D7A9h	CAN0 Message Control Register 9	C0MCTL9	00h
D7AAh	CAN0 Message Control Register 10	C0MCTL10	00h
D7ABh	CAN0 Message Control Register 11	C0MCTL11	00h
D7ACh	CAN0 Message Control Register 12	C0MCTL12	00h
D7ADh	CAN0 Message Control Register 13	C0MCTL13	00h
D7AEh	CAN0 Message Control Register 14	C0MCTL14	00h
D7AFh	CAN0 Message Control Register 15	C0MCTL15	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.31 SFR Information (31) (1)

Address	Register	Symbol	Reset Value
D7B0h	CAN0 Message Control Register 16	C0MCTL16	00h
D7B1h	CAN0 Message Control Register 17	C0MCTL17	00h
D7B2h	CAN0 Message Control Register 18	C0MCTL18	00h
D7B3h	CAN0 Message Control Register 19	C0MCTL19	00h
D7B4h	CAN0 Message Control Register 20	C0MCTL20	00h
D7B5h	CAN0 Message Control Register 21	C0MCTL21	00h
D7B6h	CAN0 Message Control Register 22	C0MCTL22	00h
D7B7h	CAN0 Message Control Register 23	C0MCTL23	00h
D7B8h	CAN0 Message Control Register 24	C0MCTL24	00h
D7B9h	CAN0 Message Control Register 25	C0MCTL25	00h
D7BAh	CAN0 Message Control Register 26	C0MCTL26	00h
D7BBh	CAN0 Message Control Register 27	C0MCTL27	00h
D7BCh	CAN0 Message Control Register 28	C0MCTL28	00h
D7BDh	CAN0 Message Control Register 29	C0MCTL29	00h
D7BEh	CAN0 Message Control Register 30	C0MCTL30	00h
D7BFh	CAN0 Message Control Register 31	C0MCTL31	00h
D7C0h	CAN0 Control Register	C0CTLR	0000 0101b
D7C1h			00h
D7C2h	CAN0 Status Register	C0STR	0000 0101b
D7C3h			00h
D7C4h	CAN0 Bit Configuration Register	C0BCR	00h
D7C5h			00h
D7C6h			00h
D7C7h	CAN0 Clock Select Register	C0CLKR	00h
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	XXh
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	00h
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	00h
D7CEh	CAN0 Receive Error Count Register	C0RECR	00h
D7CFh	CAN0 Transmit Error Count Register	C0TECR	00h
D7D0h	CAN0 Error Code Store Register	C0ECSR	00h
D7D1h	CAN0 Channel Search Support Register	C0CSSR	XXh
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
D7D4h	CAN0 Time Stamp Register	C0TSR	00h
D7D5h			00h
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	XXh
D7D7h			XXh
D7D8h	CAN0 Test Control Register	C0TCR	00h
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

J-Version

Table 5.10 Power-On Reset Circuit

The measurement condition is T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		2.0		50000	mV/ms
t_{fth}	External power V_{CC} fall gradient				50000	mV/ms
V_{por}	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

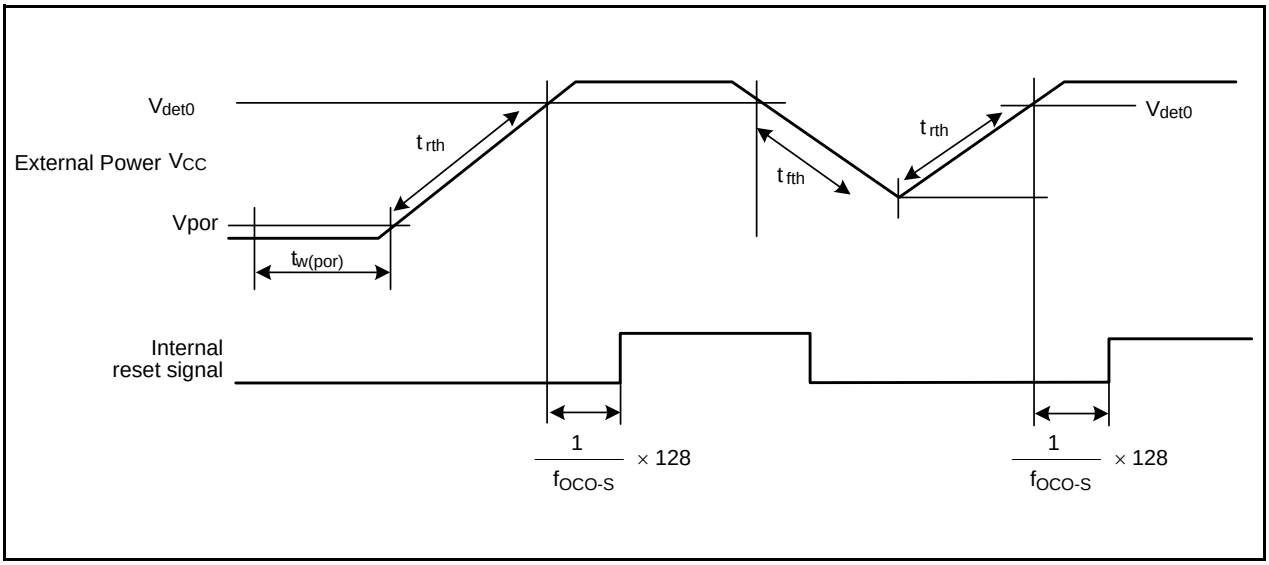


Figure 5.4 Power-On Reset Circuit Electrical Characteristics

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	VCC = 3.0 V to 5.5V			5	ms
$t_{d(R-S)}$	STOP release time				300	µs
$t_{d(W-S)}$	Low power mode wait mode release time				300	µs

Note:
1. When V_{CC} = 5 V.

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.38 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

Table 5.39 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.40 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

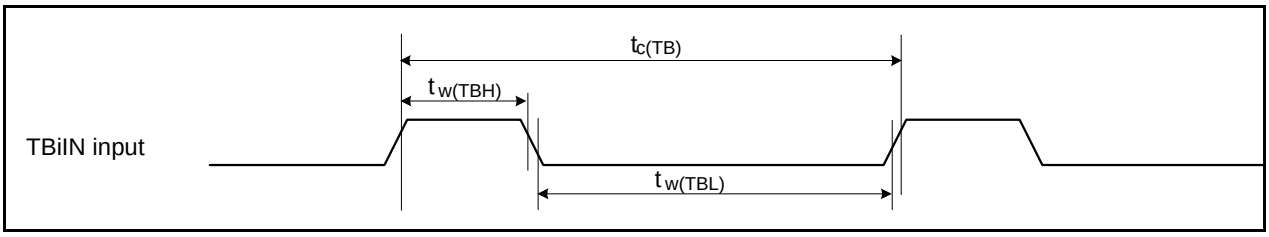


Figure 5.19 Timer B Input

K-Version

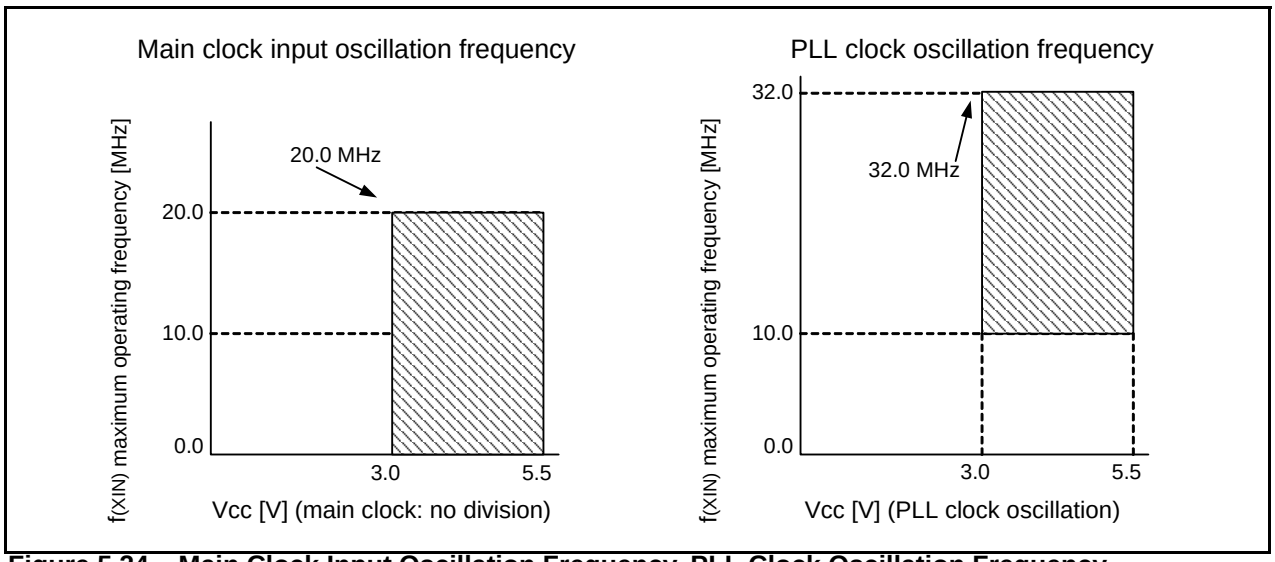


Figure 5.24 Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency

Table 5.47 Recommended Operating Conditions (2/2) (1)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -40°C to 125°C unless otherwise specified.
The ripple voltage must not exceed $V_{r(VCC)}$ and/or $dV_{r(VCC)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	V_{CC} = 5.0 V			0.3	V/ms
		V_{CC} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

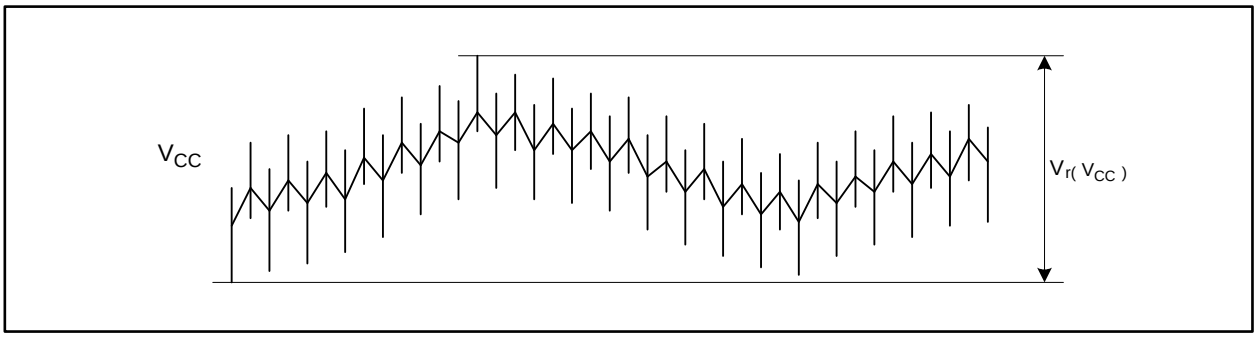


Figure 5.25 Ripple Waveform

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

Table 5.65 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

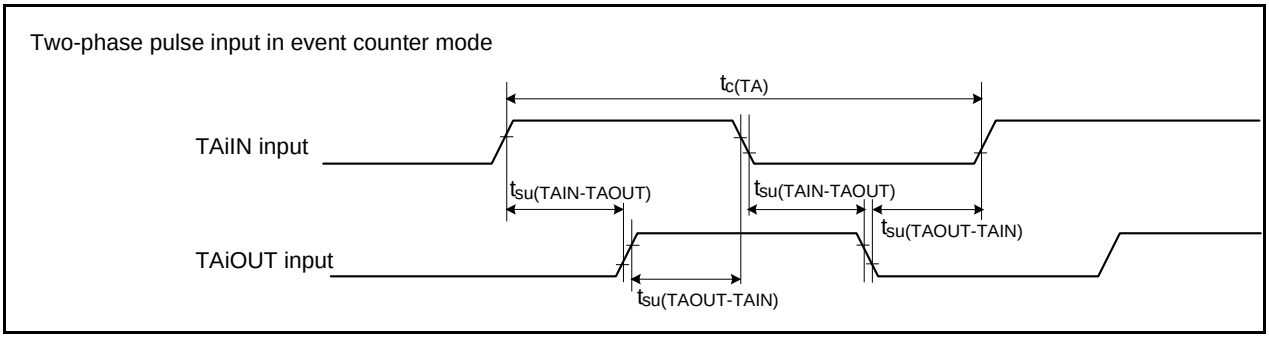


Figure 5.32 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

5.5.2.8 Multi-master I²C-bus

Table 5.72 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

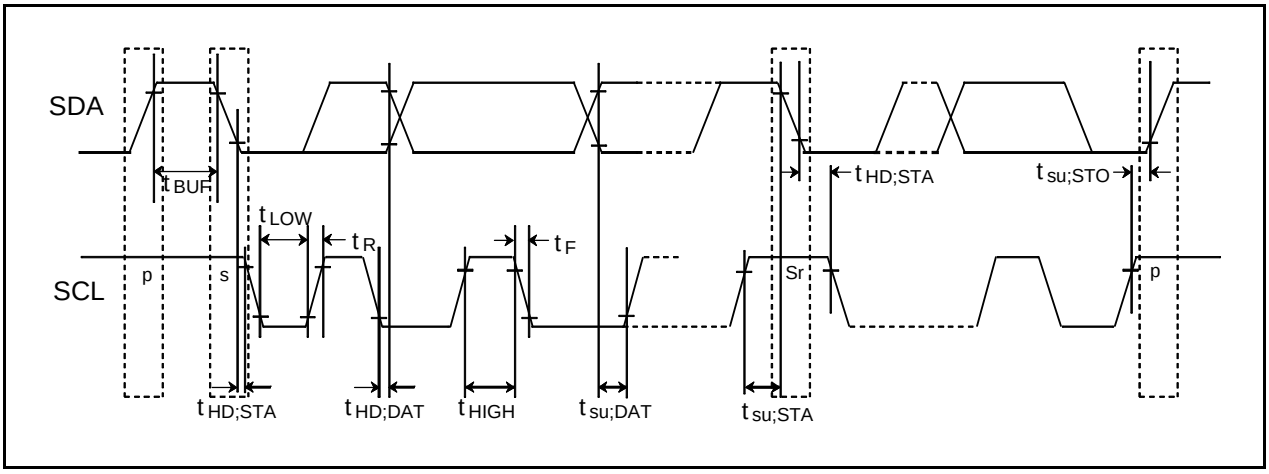


Figure 5.37 Multi-master I²C-bus

K-Version, V_{CC} = 3 V

5.6.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

5.6.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.75 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

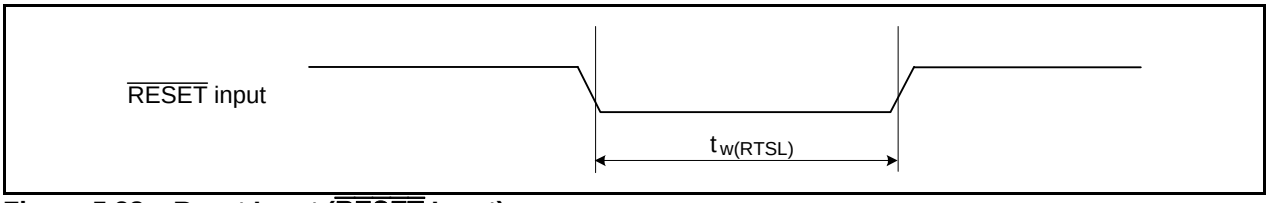


Figure 5.38 Reset Input ($\overline{\text{RESET}}$ Input)

5.6.2.2 External Clock Input

Table 5.76 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 3.0V.

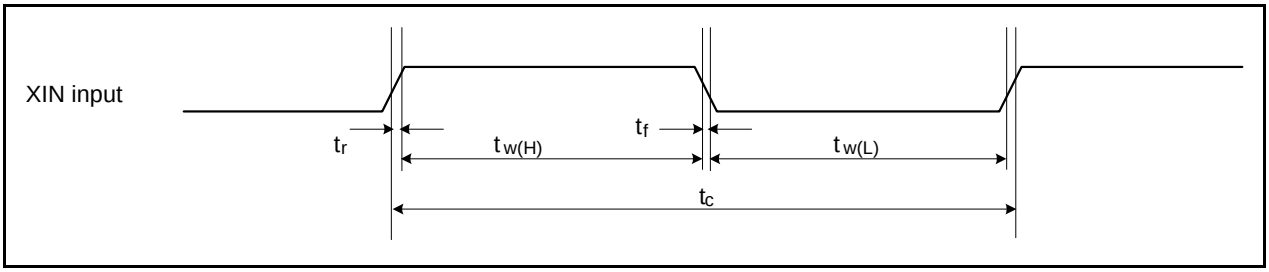


Figure 5.39 External Clock Input (XIN Input)

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

5.6.2.6 Serial Interface

Table 5.86 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

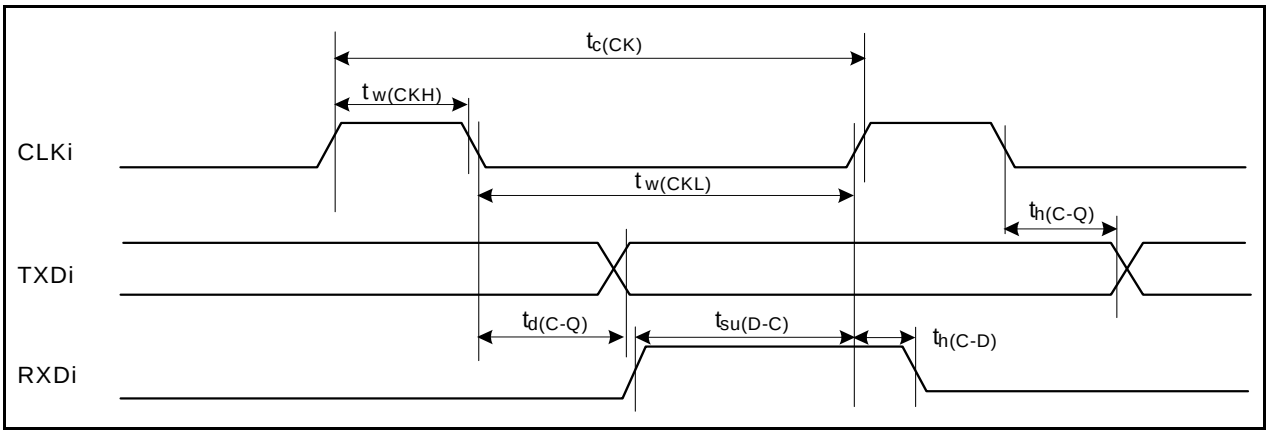


Figure 5.44 Serial Interface

5.6.2.7 External Interrupt $\overline{INTi}$ Input

Table 5.87 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

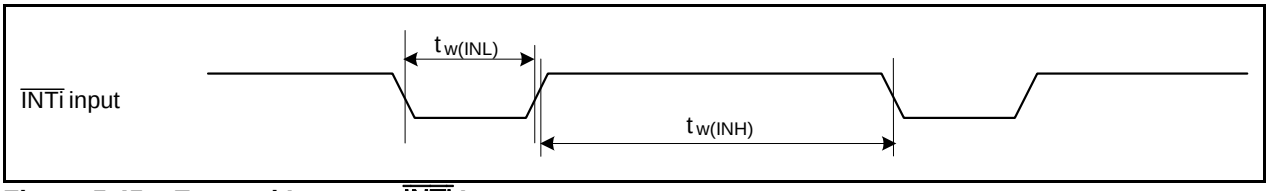


Figure 5.45 External Interrupt $\overline{INTi}$ Input

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

5.6.2.8 Multi-master I²C-bus

Table 5.88 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

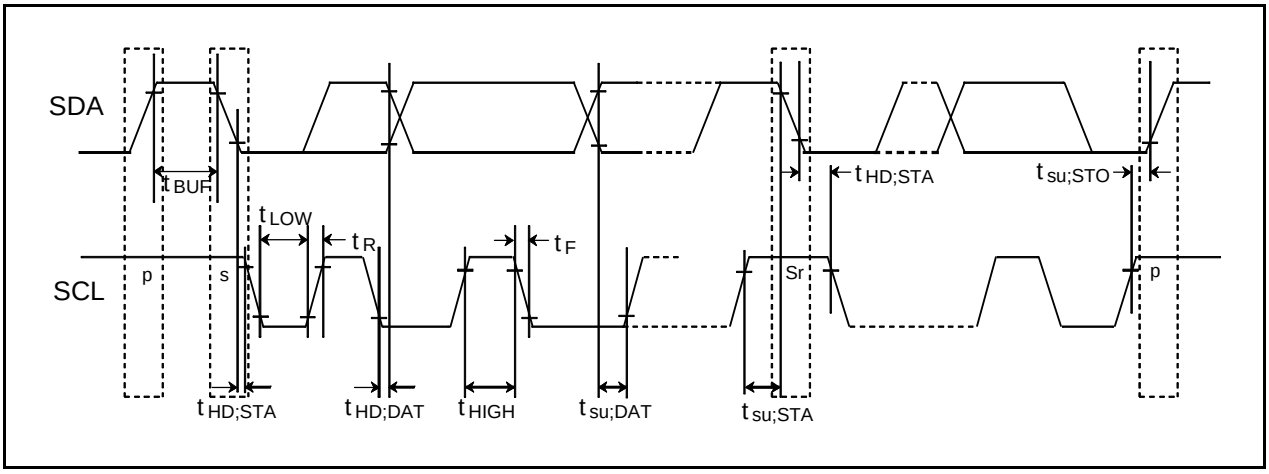


Figure 5.46 Multi-master I²C-bus

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.