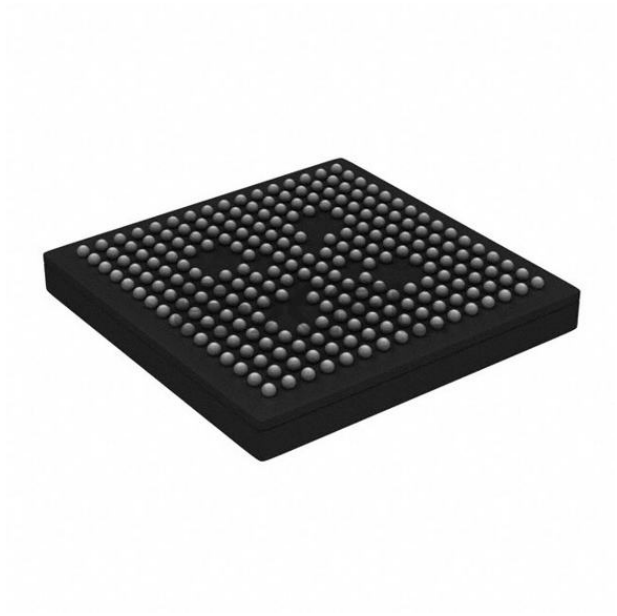


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	-
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 2.0 OTG (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	236-LFBGA
Supplier Device Package	236-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/scp2207vmu

Table 2. SCP220x Power Supply

3.0 V or 1.8V	VDD_SENSOR	IO supply for Sensor Interface block and I2C
3.0 V	VDD_OSC	Power supply for crystal pad
	VDD_SCCARD	IO supply for Smart Card Interface
	VDD_GPIO	IO supply for GPIOs and KeyScan
	VDD_DIP	IO supply for DIP block
	VDD_MISCIF	IO supply for MP2TS, UART, SPI, and JTAG interfaces.
	VDD_SDMMC	IO supply for SD/SDHC/MMC Interface
	VDD_AUDIO	IO supply for Audio Interface block
	VDD_NAND	IO supply for NAND Interface block
GND	VSS	Common ground
	VSSA_DAC	Ground for internal analog DAC
	VSS_USB	Ground for USB
	VSS_OSC	Ground for crystal pad
* See Figure 4 for VSSA_PLL connectivity		

Table 5. Configuring Boot Load Using dip_data[5:3] Pins

b001	Code is resident in a serial NAND flash connected to the SPI port. The serial Flash Memory is an industry standard memory that supports the “read data bytes” command (0x03).
[b010]	[RESERVED]
b100	Code is resident in NAND flash. The NAND flash block read sequence is: After reset is de-asserted, the bootloader will issue a “reset” command (“ff”) followed by a 25 µsec delay. The boot loader then issues the page read command (“00”) and 5 bytes of address (all “0”). This is followed by a read confirm command (“30”). Before proceeding further, a 50 µsec delay occurs. A 2 Kbyte page is then read. If ECC is enabled four 512 byte page reads are issued.

If booting from NAND Flash, there is an optional ECC checking mode that may be enabled via a software register. If ECC checking is enabled, the boot_loader checks for errors after a block is read from the device. Upon error detection, the boot loader keeps the ARM926EJ-S processor in reset.

For NAND Flash, the data must be organized in the 2K Flash sector as follows.

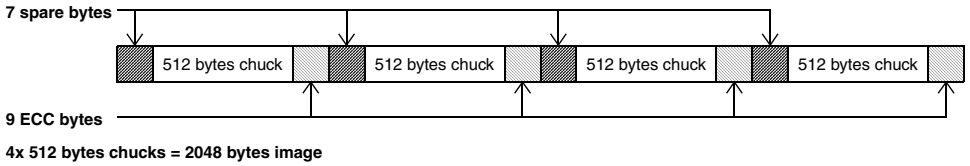


Figure 14. NAND Flash Data Organization

3.7 Low Power Configurations

The SCP220x chips offer three power consumption reduction features described below: voltage islands, clock gating and processor standby. They can be implemented independently for maximum control.

3.7.1 Voltage Islands

The SCP220x provides two voltage islands: Low Power Audio/Video domain and the IC Core domain (see Figure 2., SCP220x Internal Architecture).

The Low Power Audio/Video domain is powered through the VDD_LP pin. This domain allows for processing at reduced power consumption. The ARM926EJ-S processor runs along with some of the blocks offering some processing, audio and display capability (digital out only, see Figure 30., Display Sub-System (DSS) Internal Architecture). Apex is not running and there is no input of images.

The IC Core domain is powered through the VDD_CORE pin. This domain contains the high performance blocks such as the APEX, SIF and USB.

Low power consumption mode is achieved by removing power to the IC Core (VDD_CORE) by an external device (i.e. power MOSFET) optionally controlled via a SCP220x GPIO pin. CogniVue Reference Design Kit (RDK) has this low power option implemented. NOTE: it is recommended that all the other power lines be connected at all times even if the corresponding blocks are not active.

6-12	Double rate audio	Optional AC-link bandwidth for 88.2 or 96khz on L, C, R channels.

The AC-link input slots are described below. Data from slots 3-11 (if valid) is written into the receive fifo in the order that the channel arrives. Valid data from channel 1,2 and 12 is presented in a software register. An interrupt/status indicator informs software that the register contains new data.

Slot	Name	Description
0	SDATA_IN TAG	MSBs indicate which slots contain valid data.
1	STATUS ADDR read port	MSBs echo register address. LSBs indicate which slots request data.
2	STATUS DATA read port	16 bit command register read data.
3,4	PCM L&R ADC record	16,18,20 bit PCM data from left and right channels.
5	Modem line 1 ADC	16 bit modem data for modem line 1 input.
6	Dedicated Microphone ADC	16,18,20 bit PCM data from optional 3rd ADC input.
7,8,9	Vendor reserved	Vendor specific (enhanced input for docking, array mic, etc.
10	Modem Line 2 ADC	16 bit modem data for modem line 2 input.
11	Modem handset ADC	16 bit modem data for modem handset input.
12	Modem IO status	GPIO read port for modem status.

Channel 1&2 are used to read and write registers within the codec. The mechanism to utilize these channels is not through the fifo datapath. Instead software registers exist for the codec address, write data and read data. Configuration of these registers will enable channel 1&2 in the next audio frame. An interrupt/status indicator provides feedback on the completion of register writes or on the availability of register read data. More details of this operation is described in the register definitions. In a similar fashion, the modem IO control and status (channel 12) are also controlled by software registers.

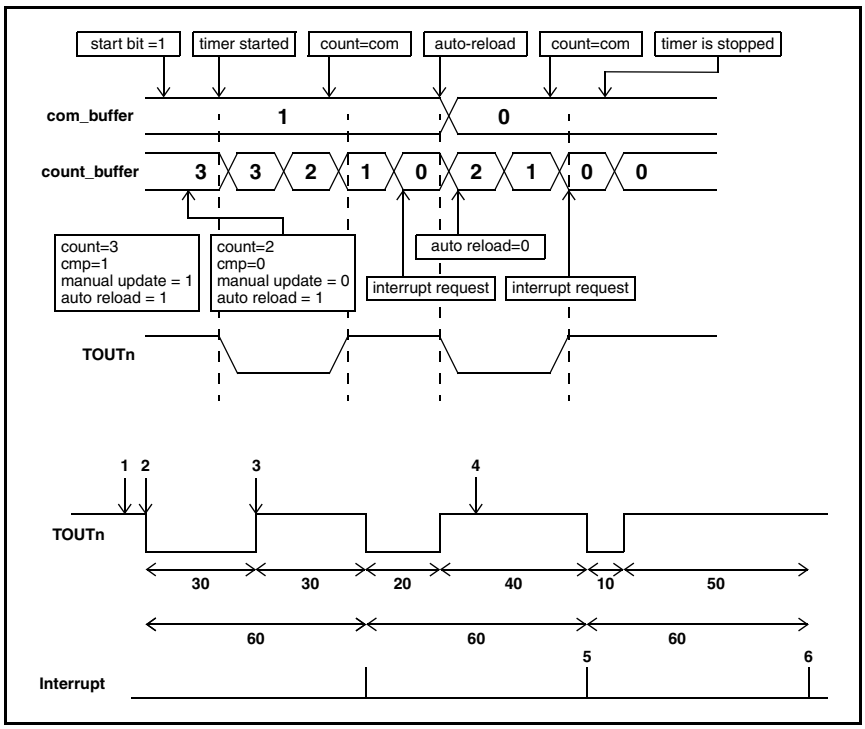
AC97 codecs have a reset input. It is assumed that this is a GPIO and under software control. Whether or not the codec sinks or sources the bit clock is determined by the conditions when the reset is removed. If the codec detects a bit clock present (minimum 5 clocks) while reset is asserted it will be configured to sink the bit clock, otherwise it will source the bit clock. Depending on the application (ASIC sinking or sourcing the bit clock) software must appropriately configure and enable the bit clock generation prior to releasing the codec reset if the application requires the ASIC to source the bit clock. This sequence of events must occur everytime the codec is reset.

There are 3 types of codec resets. The external pin reset (as described above) is a “cold” reset. When a cold reset occurs all codec registers are reset and bit clock sourcing is re-determined. A “warm” reset will re-activate the AC-link without resetting the codec registers. A “warm” reset is indicated by a 1 µsec pulse on the sync line. Software can initiate this process through register configuration. The third reset mechanism is a register bit in the codec. Software has access to this mechanism through the regular codec register configuration process.

The codec can also be placed in “power-down” mode. This is achieved by writing to a particular register in the codec. Since this mechanism requires the hardware to enter a particular state after channel 2 has been sent, in addition to the codec register configuration process, a software indicator bit must be set. To exit from this state a “warm” reset must be issued.

The AC-link provides 12 channels (@ 20 bits) with a frame rate of 48 Khz. The interface also supports a mechanism that allows for sampling rates other than 48 Khz. Data rates of 44.1 Khz, 88.2 Khz and 96 Khz are also supported. The double-rate audio (88.2 Khz or 96 Khz) is supported by combining two slots per DAC channel. This would utilize the optional alternate channel source for channels 6-12.

Up-sampling is not required to support the 44.1 Khz or 88.2 Khz data rates. Channel 0 (in both the incoming and outgoing data stream) contains valid channel flags. This provides the mechanism to send valid data in a sub-set of



The following events refer to the numbering in the above diagram

1. count=60, cmp=30, update=1, auto_reload=1, update=0. The update must be toggled from “1” to “0”. The value of the next count and cmp can be set at step 3. In the case where these values have been set prior to step 1, the update should be disabled. If the next value is set in the enable state, this next value goes into the first value of count and cmp at the “start”.
2. start=1.
3. cmp=20. This can be set as soon as the start was issued in step 2. In the case where auto_reload is enabled, the count is updated when the interrupt occurs so count and cmp must be set prior to the interrupt event. If the cmp value is enough until the next reflection, it can be set after the interrupt.
4. cmp=10.
5. auto_reload=0.
6. start=0.

4.10.2.2 PWM as general timer

Another use of the PWM is as a general timer. For this scenario, the cmp value is deducted from the PWM timer. The rest of the settings are identical to the PWM usage. For example to get an interrupt every 10msec (100hz) for a 24 Mhz clock source, the following settings are required.

- 24 Mhz / 100hz = 240,000
- 240,000 = (prescaler + 1) x (1/Tn_clk_sel) x (count + 1)
- Prescaler=99, 1/Tn_clk_sel=16, count=149

4.10.2.3 PWM dead zones

Another PWM usage is to have dead zones. A dead-zone delays the low to high transition point. The following diagram illustrates the concept.

Table 32. System Clock Configuration Register

arm_clk_div	24-22	This divide value is applied to the PLL output clock to generate the primary ARM926EJ-S processor clock. 0,7 : arm_clk = F_{PLLOUT} /12 6 : arm_clk = F_{PLLOUT} /10 5 : arm_clk = F_{PLLOUT} /8 4 : arm_clk = F_{PLLOUT} /6 3 : arm_clk = F_{PLLOUT} /4 2 : arm_clk = F_{PLLOUT} /3 1 : arm_clk = F_{PLLOUT} /2	3
sys_clk_div	21-20	This divide value is applied to the ARM926EJ-S processor clock to generate the system clock. The system clock runs all internal logic except the ARM926EJ-S processor and array processor. 11 : sys_clk = arm_clk/4 10 : sys_clk = arm_clk/3 01 : sys_clk = arm_clk/2 00 : sys_clk = arm_clk	0
	19		
Range	18-16	This field must be set according the configured post reference divide frequency. 0=bypass, 1=10-16 Mhz, 2=16-26 Mhz, 3=26-42 Mhz, 4=42-65 Mhz, 5=65-104 Mhz, 6=104-166 Mhz, 7=166 Mhz+	0
NO	15-13	PLL Output Divider value.	0
NR	12-8	PLL Input Divider value. Power-up default of this field is controlled by configuration settings on the EBI address bus.	0
NF	7-0	PLL Feedback divider value.	0

5.2.2 AP Clock Configuration Register

Table 33. AP Clock Configuration Register

AP Clock Configuration			
Address: 0x04		**Reset = 0x2000_0000**	**Type: RW**
Name	**Bit**	**Function**	**Reset**

Table 37. Memory Clock Configuration Register

NO	15-13	PLL Output Divider value.	0
NR	12-8	PLL Input Divider value.	0
NF	7-0	PLL Feedback divider value.	0

5.2.7 Interface PLL Select Register

Table 38. Interface PLL Select Register

Interface PLL Select		
Address: 0xF8	**Reset = 0x1800**	**Type: RW**

Name	Bit	Function	Reset
	31-28		
tvout_clk_gate	27	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0
usb_clk_gate	26	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0
ap_clk_gate	25	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0
mem_clk_gate	24	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0
sif_clk_gate	23	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0
xga_clk_gate	22	This field controls the clock gating cell between the PLL clock source and the clock divide circuitry. If the PLL or ref_clk_sel is being updated, the clock gating cell must be activated first. 0 = normal operation. Clock output is not gated. 1 = Clock output is gated.	0x0

Table 44. PAD has a pull-up or pull-down

17-PD	audio_clkr_p		41-PU	dip_csn1_p		65-PD	mp2ts_clk_p mp2ts_d_p mp2ts_valid_p mp2ts_sync_p		89-PD	spi1_txd_p	
18-PD	audio_fsr_p		42-PU	dip_csn2_p		66	reserved		90-PD	spi1_rxd_p	
19-PD	audio_clkx_p		43-PU	dip_csn3_p		67	reserved		91-PD	spi1_sck_p	
20-PD	audio_dr_p		44-PD	spi_rxd_p		68	reserved		92-PD	uart_cts_p	
21-PD	audio_dx_p		45-PD	spi_sck_p		69	reserved		93-PD	uart_rts_p	
22-PD	audio_fsx_p		46-PU	spi_ssn_p		70	reserved		94	reserved	
23	reserved		47-PD	spi_txd_p		71	reserved		95	reserved	

5.4 Reset and Clock Gating

The system reset bits are spread out into two registers: System Reset and System Reset1.

The system power down bits are spread out into two registers: System Power Down and System Power Down1.

5.4.1 System Power Down

This timing generation block has clock gating logic for most of the internal blocks. This register provides software with a mechanism to gate the clock of any block that is not required for the application at hand. This will reduce power for certain applications. When a block has its clock gated the block is “disabled” and unusable.

Table 45. System Power Down

System Power Down			
Address: 0x d003_001c		**Reset = 0xffed_d5ff**	**Type: RW**
Name	**Bit**	**Function**	**Reset**
Reserved	31	Reserved	1
mp2ts1_pdown	30	When this bit is written “1” the peripheral has its clock gated.	1
spi1_pdown	29	When this bit is written “1” the peripheral has its clock gated.	1
Pwi_pdown	28	When this bit is written “1” the peripheral has its clock gated.	1
Mmcplus_pdown	27	When this bit is written “1” the peripheral has its clock gated.	1

Qos_master_bits	20-18	Encodes the 4 bits of the 8 bit AXI ARID that select one of the 16 QOS values. 000=ARID[3:0], 001=ARID[4:1], 010=ARID[5:2], 011=ARID[6:3], 100=ARID[7:4]	d0
Memory_burst	17-15	Encodes the number of data accesses that are performed to the SDRAM for each read or write command. 000=burst1, 001=burst2, 010=burst4, 011=burst8, 100=burst16 The value must also be programmed into the SDRAM mode register using the direct_cmd register at offset 0x8 and must match it.	d3
Stop_mem_clk	14	When enabled, the memory clock is dynamically stopped when not performing an access to the SDRAM.	d0
Auto_power_down	13	When this is set, the memory interface automatically places the SDRAM into the power-down state by de-asserting CKE when the command FIFO has been empty for the PowerDownPrd memory clock cycles.	d0
Power_down_prd	12-7	Number of memory clock cycles for auto power-down of the SDRAM.	d0
Ap_bit	6	Encodes the position of the auto-precharge bit in the memory address. 0=addr10, 1=addr8	d2
Row_bits	5-3	Encodes the number of the AXI address that comprise the row address. 000=11bits, 001=12bits, 010=13bits, 011=14bits, 100=15bits, 101=16bits The combination of row size, column size, BRC/RBC and memory width must ensure that neither the MSB of the row address nor the MSB of the bank address exceed address range [27:0].	d0
Column_bits	2-0	Encodes the number of the AXI address that comprise the column address. 000=8bits, 001=9bits, 010=10bits, 011=11bits, 100=12bits	d0

5.6.6 refresh_prd register

This sets the memory refresh period. It can only be read/written to in the config or low-power state.

Refresh_prd		
Address: 0x10	**Reset = 0xa60**	**Type: RW**

Name	**Bit**	**Function**	**Reset**
Reserved	31-15	Reserved	
Refresh_prd	14-0	Memory refresh period in memory clock cycles.	0xa60

5.6.7 cas_latency register

This sets the cas_latency in memory clock cycles. It can only be read/written to in the config or low-power state.

Cas_latency		
Address: 0x14	**Reset = 0x6**	**Type: RW**

Address: 0x40		Reset = 0x1	Type: RW
Name	**Bit**	**Function**	**Reset**
Reserved	31-8	Reserved	
Txp	7-0	Sets the exit power-down command time in memory clock cycles.	0x1

5.6.19 Txsr Register

It can only be read/written to in the config or low-power state.

Txsr			
Address: 0x44		**Reset = 0xa**	**Type: RW**
Name	**Bit**	**Function**	**Reset**
Reserved	31-8	Reserved	
Txsr	7-0	Sets the exit self-refresh command time in memory clock cycles.	0xa

5.6.20 Tesr Register

It can only be read/written to in the config or low-power state.

Tesr			
Address: 0x48		**Reset = 0x14**	**Type: RW**
Name	**Bit**	**Function**	**Reset**
Reserved	31-8	Reserved	
Tesr	7-0	Sets the self-refresh command time in memory clock cycles.	0x14

5.6.21 Memory_cfg2 Register

It can only be read/written to in the config or low-power state.

Memory_cfg2			
Address: 0x4c		**Reset = 0x0**	**Type: RW**
Name	**Bit**	**Function**	**Reset**
Reserved	31-11	Reserved	
Read_delay	10-9	Sets the latency in clocks cycles of the PAD interface.	0x0

Table 54. Interrupt Clear Register

rx_fe	3	Clears the interrupt when written ‘1’.	0x0
tx_ff	2	Clears the interrupt when written ‘1’.	0x0
tx_hf	1	Clears the interrupt when written ‘1’.	0x0
tx_fe	0	Clears the interrupt when written ‘1’.	0x0

5.7.5 Interface Timing

All timing parameters refer to increments of the internal reference clock and a value of .0. means 1x refclk, a value of .1. means 2x refclk, etc.

Table 55. Interface Timing

Interface Timing			
Address: 0x0C		**Reset = 0x01001000**	**Type: RW**
Name	**Bit**	**Function**	**Reset**
Chip_select_sel	31-28	The nand interface supports 4 external chip selects (of which only one can be active at any one time). This “one-hot” field indicates which external chip select is active. The chip select that is active is turned on and off by the controlling bits in the NAND Action register. 0001 – chip select 0 selected 0010 – chip select 1 selected 0100 – chip select 2 selected 1000 – chip select 3 selected Any other value will disabled all chip selects.	0x0
t7	27-24	Indicates the number of system clocks from NAND_CLE/NAND_ALE inactive to NAND_ALE/ NAND_CLE active. Also indicates the number of system clocks from NAND_ALE inactive to NAND_WE/NAND_RE active. A value of ‘0’ is invalid for this field.	0x1
t6	23-20	Indicates the number of system clocks for the NAND_RE inactive pulse width	0x0
t5	19-16	Indicates the number of system clocks for the NAND_RE active pulse width	0x0
t4	15-12	Indicates the number of system clocks for the NAND_WE inactive pulse width. A value of ‘0’ is invalid for this field.	0x1
t3	11-8	Indicates the number of system clocks from NAND_WE inactive to NAND_CLE inactive	0x0
t2	7-4	Indicates the number of system clocks for the NAND_WE active pulse width	0x0
t1	3-0	Indicates the number of system clocks from NAND_CLE active to NAND_WE active	0x0

Read_parity	31-0	Bits [63:32] of the read parity	0x0

Table 69. RS ECC read parity

RS ECC read parity3			
Address: 0x74		Reset = 0x0	Type: RW
Name	**Bit**	**Function**	**Reset**
Reserved	31-8	Reserved	
Read_parity	7-0	Bits [71:64] of the read parity	0x0

5.7.20 RS ECC write parity

These registers contain the 9 bytes of generated parity that are generated by the RS ECC engine after a 512 bytes block is written to NAND flash. The 9 bytes can be read and then written to nand flash.

RS ECC write parity1			
Address: 0x78		Reset = 0x0	Type: RO
Name	**Bit**	**Function**	**Reset**
Write_parity	31-0	Bits 31:0 of the write parity	0x0

RS ECC write parity2			
Address: 0x7C		Reset = 0x0	Type: RO
Name	**Bit**	**Function**	**Reset**
Write_parity	31-0	Bits [63:32] of the write parity	0x0

Table 70. RS ECC write parity

RS ECC write parity3			
Address: 0x80		Reset = 0x0	Type: RO
Name	**Bit**	**Function**	**Reset**
Reserved	31-8	Reserved	
Write_parity	7-0	Bits [71:64] of the write parity	0x0

5.7.21 RS ECC Status

Table 71. RS ECC Status

RS ECC Status			
Address: 0x84		Reset = 0x0	Type: RO
Name	**Bit**	**Function**	**Reset**
Reserved	31-2	Reserved	
rs_ecc_read_status	1-0	After the 512 byte read operation is completed and the “read_ecc_complete” interrupt is asserted, this field indicates the status of the block read. 00 = no errors 01 = correctable errors 1x = uncorrectable errors	0x0

5.7.22 Transmit FIFO

The Transmit FIFO operates as a FIFO even though it has a range of addresses. The wider range allows bus bursting to fill the FIFO.

Table 72. Transmit FIFO

Transmit FIFO			
Address: 0x1000-0x1fff		Reset = 0x0	Type: WO
Name	**Bit**	**Function**	**Reset**
data	31-0	This field contains the data to be written to the FIFO. This register supports 8,16 or 32 bit writes and pushes the appropriate amount of data into the FIFO.	0x0

5.7.23 Receive FIFO

The Receive FIFO operates as a FIFO even though it has a range of addresses. The wider range allows bus bursting to drain the FIFO.

Table 73. Receive FIFO

Receive FIFO			
Address: 0x2000-0x2fff		Reset = 0x0	Type: WO
Name	**Bit**	**Function**	**Reset**
data	31-0	This field contains the data to be read from the FIFO. This register supports 8,16 or 32 bit reads and pops the appropriate amount of data from the FIFO.	0x0

Address: 0x18	Reset = 0x0	Type: RW	
Name	**Bit**	**Function**	**Reset**
Reserved	31	Reserved	0x0
tx_dly	30-24	This field provides the capability to delay the first bit period of valid data from the assertion of the transmit frame clock. This field contains the number of transmit bit clocks from the active edge of the frame clock to the first valid bit of transmitted data.	0x0
tx_frame_width	23-16	This field controls the active width of the transmit frame clock. The field represents the number of transmit bit clocks and has a minimum value of 1.	0x0
tx_frame_period	15-0	This field contains the divider value applied to the transmit bit clock to produce the transmit frame clock. Values of 2 or greater are valid.	0x0

5.10.8 C97 Configuration

AC97 Configuration			
Address: 0x1C	**Reset = 0x0**	**Type: RW**	
Name	**Bit**	**Function**	**Reset**
Reserved	31-16	Reserved	0x0
codec_id	15-14	This field contains the codec ID that will be transmitted during slot 0. Multiple codecs are not supported so the ID will probably always be ‘0’ for a primary codec. The field has been made configurable just in case the flexibility is required.	0x0
warm_reset	13	Writing a ‘1’ to this bit will initiate a “warm” reset on the AC-link interface. This should only be initiated if the codec is in the power-down mode. This bit will cause the hardware to assert the sync signal for 1µsec initiating a warm reset within the codec. The bit is self resetting after the reset activity is complete. Prior to writing to this bit initiate a warm reset, the codec_pdown bit must be cleared in the AC97 command register. 0 = no action 1 = hardware initiates a warm reset	0x0
tx_slot_ena	12 -3	Enables the transmit channel for slots 3 to 12. If variable sampling rates are enabled, this bit is ignored and the slot enable information is obtained from the received TAG slot information. 0 = disable slot 1 = enable slot	0x0
Reserved	2-1	Reserved	0x0

	31-18		
data_complete	17	Clears the interrupt when written ‘1’.	0x0
data_crc	16	Clears the interrupt when written ‘1’.	0x0
response	15	Clears the interrupt when written ‘1’.	0x0
response_crc	14	Clears the interrupt when written ‘1’.	0x0
dat3_low	13	Clears the interrupt when written ‘1’.	0x0
dat3_high	12	Clears the interrupt when written ‘1’.	0x0
cmd_complete	11	Clears the interrupt when written ‘1’.	0x0
busy	10	Clears the interrupt when written ‘1’.	0x0
tx_pop_error	9	Clears the interrupt when written ‘1’.	0x0
rx_push_error	8	Clears the interrupt when written ‘1’.	0x0
dma_pop_error	7	Clears the interrupt when written ‘1’.	0x0
dma_push_error	6	Clears the interrupt when written ‘1’.	0x0
rx_ff	5	Clears the interrupt when written ‘1’.	0x0
rx_hf	4	Clears the interrupt when written ‘1’.	0x0
rx_fe	3	Clears the interrupt when written ‘1’.	0x0
tx_ff	2	Clears the interrupt when written ‘1’.	0x0
tx_hf	1	Clears the interrupt when written ‘1’.	0x0
tx_fe	0	Clears the interrupt when written ‘1’.	0x0

5.11.4 MMC/SD Clock Rate

MMC/SD clock rate			
Address: 0x0C	**Reset = 0x80000000**	**Type: RW**	
Name	**Bit**	**Function**	**Reset**
disable	31	This bit provides a lower power standby condition when the SD interface is in use. Setting this bit will halt the clock such that the external serial clock is low. Power-up default is a disabled clock. Software must ensure that the proper divide is programmed prior to enabling the clock. Also, it is recommended to disable the clock whenever a clock_rate_divider change is required so that spurious clock pulses do not occur.	0x1
Reserved	30-16	Reserved	
clock_divider	15-0	The interface PLL clock is divided by the contents of this field to produce the serial clock. A divider of 2 or greater is valid.	0x0

MMCPLUS clock rate	0x0C	RW
MMCPLUS Configuration	0x10	RW
MMCPLUS Data Control	0x14	RW
MMCPLUS argument	0x18	RW
MMCPLUS command	0x1C	RW
MMCPLUS command response	0x20	RO
MMCPLUS response	0x24-0x30	RO
fifo status	0x34	RO/WO
fifo flag Configuration	0x38	RW
reserved	0x3C-0xfff	
transmit fifo	0x1000-0x1fff	WO
receive fifo	0x2000-0x2fff	RO

5.12.1 Interrupt Source Register

The interrupt source register contains the raw unmasked interrupts and can be used for polling purposes (instead of the external interrupt pin) or for determining which interrupt(s) have caused the external interrupt pin to assert.

Interrupt Source Register			
Address: 0x00		**Reset = 0x0**	**Type: RO**
Name	**Bit**	**Function**	**Reset**
Reserved	31-20	Reserved	
dat3	19	This is not an interrupt but reflects the current state of the mmc_data3 signal.	0x0
sdio_interrupt	18	SDIO cards have a card interrupt mechanism. This bit is the indicator for that interrupt and is only applicable to SDIO cards. This interrupt source can be masked but not cleared by the interrupt clear register. It must be cleared within the SDIO card itself.	0x0
data_complete	17	Indicates that an MMCPLUS data operation (read or write) is complete.	0x0
data_crc	16	Indicates that for an MMCPLUS data operation, the CRC check failed.	0x0
response	15	Indicates that for MMCPLUS operation, an MMCPLUS response is available in the response buffer.	0x0
response_crc	14	Indicates that the received MMCPLUS response has a CRC check failure.	0x0
dat3_low	13	This interrupt is asserted when the data state machine is idle and the mmc_data3 is low.	0x0
dat3_high	12	This interrupt is asserted when the data state machine is idle and the mmc_data3 is high.	0x0
cmd_complete	11	Indicates that the current MMCPLUS command has been sent.	0x0

command_index	5-0	Contains the command index field of the last received response. If the response is type R2 or R3 the field will be ’111111’.	0x0

5.12.10 MMCPLUS Response

MMCPLUS response			
Address: 0x24	**Reset = 0x0**	**Type: RO**	
Name	**Bit**	**Function**	**Reset**
card_status CID/CSD[39:8]	31-0	These registers are used to store the current SD response. If the response is type R1, R1b or R6 only the first 32 bits of the response field are valid Contains the card status field of the response or contains either the CID fields or CSD fields if a command is issued that queries this information.	0x0

MMCPLUS response			
Address: 0x28	**Reset = 0x0**	**Type: RO**	
Name	**Bit**	**Function**	**Reset**
CID/CSD[71:40]	31-0	Contains either the CID fields or CSD fields if a command is issued that queries this information.	0x0

MMCPLUS response			
Address: 0x2C	**Reset = 0x0**	**Type: RO**	
Name	**Bit**	**Function**	**Reset**
CID/CSD[103:72]	31-0	Contains either the CID fields or CSD fields if a command is issued that queries this information.	0x0

MMCPLUS response			
Address: 0x30	**Reset = 0x0**	**Type: RO**	
Name	**Bit**	**Function**	**Reset**
Reserved	31-24	Reserved	
CID/CSD[127:104]	23-0	Contains either the CID fields or CSD fields if a command is issued that queries this information.	0x0

5.12.11 FIFO Status

FIFO status		

keyscan2_en	2	Keyscan2 enable 1 : enable 0 : disable	0x0
keyscan1_en	1	Keyscan1 enable 1 : enable 0 : disable	0x0
keyscan0_en	0	Keyscan0 enable 1 : enable 0 : disable	0x0

5.15.6 Keypad Time

Keypad time		
Address: 0x14	**Reset = 0x1FFF**	**Type: RW**

Name	Bit	Function	Reset
Reserved	31-13	Reserved	0x0
scan_time	12-0	Key scan driving time. Scan_time_freq = sys_freq / (scan_time+1)	0x1FFF

5.15.7 Keypad Value

Keypad value		
Address: 0x18	Reset = 0x0	Type: RO

Name	Bit	Function	Reset
Reserved	31-16	Reserved	0x0
sense_value	15-0	Contains the sense value vector. This vector is a dynamic view of the key sense information and will change for every key scan interval. If a latched version of this field is desired, please read the interrupt source register.	0x0

The following table illustrates the sense_value vector.

	key_sense3	key_sense2	key_sense1	key_sense0
key_scan3	sense_value15	sense_value14	sense_value13	sense_value12
key_scan2	sense_value11	sense_value10	sense_value9	sense_value8
key_scan1	sense_value7	sense_value6	sense_value5	sense_value4
key_scan0	sense_value3	sense_value2	sense_value1	sense_value0

5.16 GPIO Registers

The General Purpose Input Output (GPIO) pins are controlled with several registers.

- GPIO Enable Registers activate the pin for GPIO use, otherwise the pin has its primary or alternate function.
- GPIO Direction Registers determine the GPIO as input or output.

Table 88. SCP220x Pinout

sd_clk	SDMMC	Bi-dir. 4 mA / 8 mA	-	F1
sd_cmd	SDMMC	Bi-dir. 4 mA / 8 mA	-	F2
sd_D[0]	SDMMC	Bi-dir. 4 mA / 8 mA	-	F3
sd_D[1]	SDMMC	Bi-dir. 4 mA / 8 mA	-	G1
sd_D[2]	SDMMC	Bi-dir. 4 mA / 8 mA	-	G2
sd_D[3]	SDMMC	Bi-dir. 4 mA / 8 mA	-	G3
Audio				
audio_clkr	AUDIO	Bi-dir. 2 mA / 4 mA	-	P10
audio_clkx	AUDIO	Bi-dir. 2 mA / 4 mA	-	N10
audio_dr	AUDIO	Bi-dir. 2 mA / 4 mA	-	M10
audio_dx	AUDIO	Bi-dir. 2 mA / 4 mA	-	N9
audio_fsr	AUDIO	Bi-dir. 2 mA / 4 mA	-	M9
audio_fsx	AUDIO	Bi-dir. 2 mA / 4 mA	-	N8
mclk	AUDIO	Bi-dir. 2 mA / 4 mA	-	M8
MP2TS				
mp2ts_clk	MISCIF	Input	n.a.	E1
mp2ts_valid	MISCIF	Input	n.a.	E2
mp2ts_sync	MISCIF	Input	n.a.	E3
mp2ts_data	MISCIF	Input	n.a.	E4
USB				
usb_phy_id	USB	USB PAD	n.a.	J5
usb_phy_vbus	USB	USB PAD	n.a.	J4
usb_phy_Plus	USB	USB PAD	n.a.	K1
usb_phy_Minus	USB	USB PAD	n.a.	J1
usb_phy_res	USB	USB PAD	n.a.	J3
utmiotg_drvvbus	AUDIO	Bi-dir. 4 mA / 8 mA	PU	R10
Smart Card				
sc_io	SCCARD	Bi-dir. 4 mA / 8 mA	-	H1
sc_card_detect	SCCARD	Bi-dir. 4 mA / 8 mA	-	H2
sc_card_voltage	SCCARD	Bi-dir. 4 mA / 8 mA	-	H3
sc_fcb	SCCARD	Bi-dir. 4 mA / 8 mA	-	H4
sc_clk	SCCARD	Bi-dir. 4 mA / 8 mA	PU	H5

Table 88. SCP220x Pinout

DQS[3]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[0]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[1]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[2]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[3]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[4]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[5]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[6]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[7]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[8]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[9]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[10]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[11]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[12]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[13]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[14]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[15]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[16]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[17]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[18]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[19]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[20]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[21]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[22]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[23]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[24]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[25]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[26]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[27]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[28]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[29]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-
DQ[30]	SDRAM	Bi-dir. 4 mA / 8 mA	-	-

Table 88. SCP220x Pinout

reserved_20	NAND	Bi-dir. 2 mA / 4 mA	PU	-
reserved_21	NAND	Bi-dir. 2 mA / 4 mA	PU	-
reserved_22	NAND	Bi-dir. 2 mA / 4 mA	PU	-
reserved_23	DIP	Bi-dir. 4 mA / 8 mA	-	-
reserved_24	DIP	Bi-dir. 4 mA / 8 mA	-	-
reserved_25	NAND	Bi-dir. 2 mA / 4 mA	-	-
reserved_26	DIP	Bi-dir. 4 mA / 8 mA	-	-
reserved_27	DIP	Bi-dir. 4 mA / 8 mA	-	-
reserved_28	DIP	Bi-dir. 4 mA / 8 mA	-	-
reserved_29	DIP	Bi-dir. 4 mA / 8 mA	-	-

Notes:
(1) Must be pulled-up to VDD_DIP (100 KOhms 1/16 W 5% suggested) for correct operation on SCP2201 and SCP2207.
(2) Software queries the SCP2207 pkg_opt[2:0] and jtag_sel_p[2:0] pins to determine the SDRAM used in the system. Currently CogniVue supports a 128 MB Micron mobile DDR SDRAM, and the pkg_opt[2:0] and jtag_sel_p[2:0] must both be set to binary '101' (decimal value 5). Consult the factory for interfacing to any other memory.

Table 89. SCP220x Power Pin

Power Pin Name	Description	SCP2201 and SCP2207 Ball #
VDD_CORE	Core supply	G8, G9, H8, H9
VDD_LP	Low-power audio/video supply	J7, J10, K11, K12
VDDA_PLL	Analog PLL supply	J14
VSSA_PLL	Return for PLL VDD (**DO NOT CONNECT TO GROUND**)	H14
VDD_SDRAM	SDRAM core and EBI/SDRAM IO supply	F7,L7
VDD_OSC	Analog supply for crystal pad	J15
VDD_USB	Analog supply for USB	K2
VDDL_USB	USB core supply	-
VDDA_DAC	Analog supply for internal DAC	P1
VDD_SENSOR	Sensor Interface (SIF) and I2C IO supply	F10
VDD_GPIO	GPIO and keyscan supply	D12