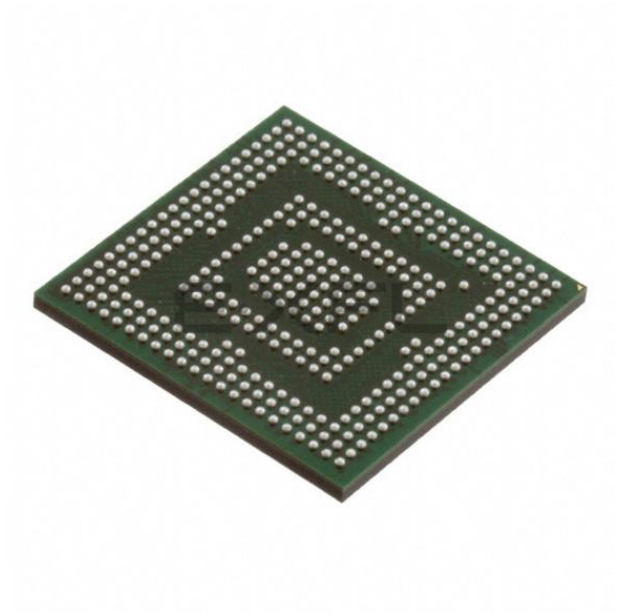

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21583wcbcz4a10

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REVISION HISTORY

10/2016—Revision 0: Initial Version

Generic Interrupt Controller (GIC), PL390 (ADSP-SC58x Only)

The generic interrupt controller (GIC) is a centralized resource for supporting and managing interrupts. The GIC splits into the distributor block (GICPORT0) and the CPU interface block (GICPORT1).

Generic Interrupt Controller Port0 (GICPORT0)

The GICPORT0 distributor block performs interrupt prioritization and distribution to the GICPORT1 blocks that connect to the processors in the system. It centralizes all interrupt sources, determines the priority of each interrupt, and forwards the interrupt with the highest priority to the interface, for priority masking and preemption handling.

Generic Interrupt Controller Port1 (GICPORT1)

The GICPORT1 CPU interface block performs priority masking and preemption handling for a connected processor in the system. GICPORT1 supports 8 software generated interrupts (SGIs) and 254 shared peripheral interrupts (SPIs).

L2 Cache Controller, PL310 (ADSP-SC58x Only)

The L2 cache controller, PL310 (see Figure 2), works efficiently with the ARM Cortex-A5 processors that implement system fabric. The cache controller directly interfaces on the data and instruction interface. The internal pipelining of the cache controller is optimized to enable the processors to operate at the same clock frequency. The cache controller supports the following:

- Two read/write 64-bit slave ports, one connected to the ARM Cortex-A5 instruction and data interfaces, and one connecting the ARM Cortex-A5 and SHARC+ cores for data coherency.
- Two read/write 64-bit master ports for interfacing with the system fabric.

SHARC PROCESSOR

Figure 3 shows the SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I/D cache controller, L1 memory blocks, and the master/slave ports. Figure 4 shows the SHARC+ SIMD core block diagram.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

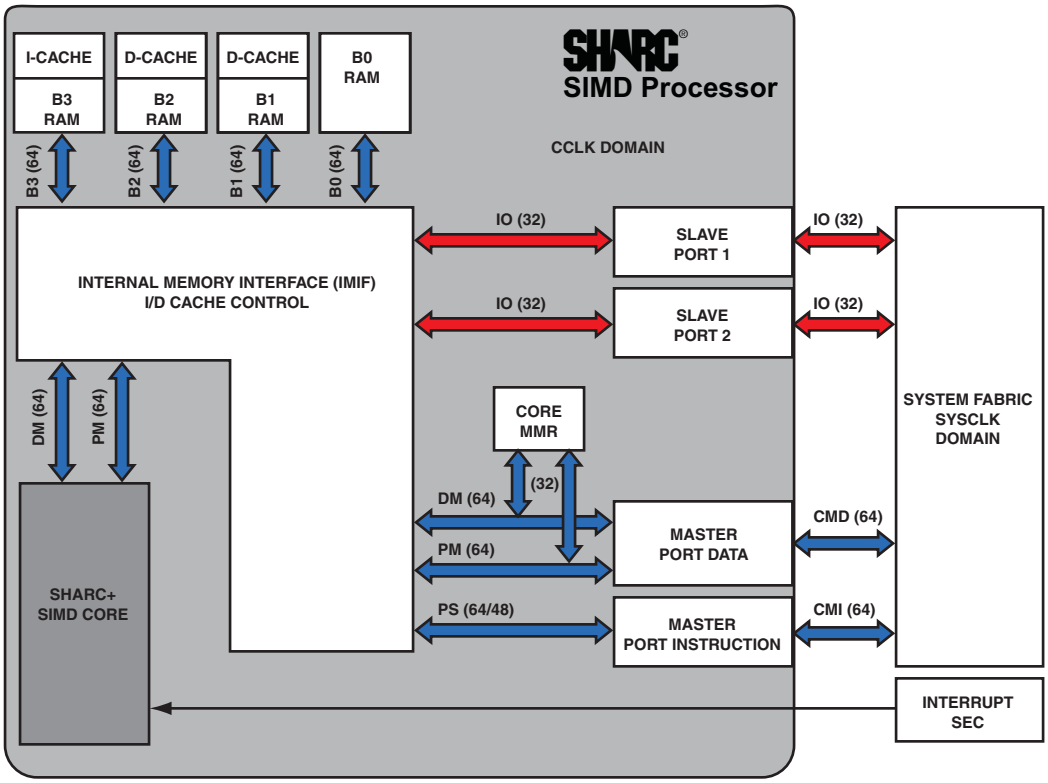

Figure 3. SHARC Processor Block Diagram

- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, RMII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Controller Area Network (CAN)

There are two controller area network (CAN) modules. A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to the capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on the first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- Interrupts, including transmit and receive complete, error, and global

An additional crystal is not required to supply the CAN clock because it is derived from a system clock through a programmable divider.

Timers

The processors include several timers that are described in the following sections.

General-Purpose (GP) Timers (TIMER)

There is one general-purpose (GP) timer unit, providing eight general-purpose programmable timers. Each timer has an external pin that can be configured either as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM_TMR[n] pins, an external TM_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and/or stopped by any TRU master without core intervention.

Watchdog Timer (WDT)

Two on-chip software watchdog timers (WDT) can be used by the ARM Cortex-A5 and/or SHARC+ cores. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

General-Purpose Counters (CNT)

A 32-bit counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

PCI Express (PCIe)

A PCI express interface (PCIe) is available on some product variants (see Table 2 and Table 3). This single, bidirectional lane can be configured to be either a root complex (RC) or end point (EP) system. The PCIe interface has the following features:

- Compliance with the *PCI Express Base Specification 3.0*
- Support for transfers at either 2.5 Gbps (Gen 1) or 5.0 Gbps (Gen 2) in each direction
- Support for 8b/10b encode and decode
- Lane reversal and lane polarity inversion
- Flow control of data in both the transmit and receive directions
- Support for removal of corrupted packets for error detection and recovery
- Maximum transaction payload of 256 bytes

Housekeeping Analog-to-Digital Converter (HADC)

The housekeeping analog-to-digital converter (HADC) provides a general-purpose, multichannel successive approximation ADC. It supports the following set of features:

- 12-bit ADC core (10-bit accuracy) with built in sample and hold.
- Eight single-ended input channels that can be extended to 15 channels by adding an external channel multiplexer.
- Throughput rates up to 1 MSPS.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DAI1_PIN01	DAI1 Pin 1	Not Muxed	DAI1_PIN01
DAI1_PIN02	DAI1 Pin 2	Not Muxed	DAI1_PIN02
DAI1_PIN03	DAI1 Pin 3	Not Muxed	DAI1_PIN03
DAI1_PIN04	DAI1 Pin 4	Not Muxed	DAI1_PIN04
DAI1_PIN05	DAI1 Pin 5	Not Muxed	DAI1_PIN05
DAI1_PIN06	DAI1 Pin 6	Not Muxed	DAI1_PIN06
DAI1_PIN07	DAI1 Pin 7	Not Muxed	DAI1_PIN07
DAI1_PIN08	DAI1 Pin 8	Not Muxed	DAI1_PIN08
DAI1_PIN09	DAI1 Pin 9	Not Muxed	DAI1_PIN09
DAI1_PIN10	DAI1 Pin 10	Not Muxed	DAI1_PIN10
DAI1_PIN11	DAI1 Pin 11	Not Muxed	DAI1_PIN11
DAI1_PIN12	DAI1 Pin 12	Not Muxed	DAI1_PIN12
DAI1_PIN19	DAI1 Pin 19	Not Muxed	DAI1_PIN19
DAI1_PIN20	DAI1 Pin 20	Not Muxed	DAI1_PIN20
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_A14	DMC0 Address 14	Not Muxed	DMC0_A14
DMC0_A15	DMC0 Address 15	Not Muxed	DMC0_A15
DMC0_BA0	DMC0 Bank Address 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
$\overline{\text{DMC0\_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09

Table 17. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	PPI0_D09	PWM2_CL		SMC0_D04	
PE_01	PPI0_FS2	SPI0_SEL5	UART1_CTS	C1_FLG0	
PE_02	PPI0_FS1	SPI0_SEL6	UART1_RTS	C2_FLG0	
PE_03	PPI0_CLK	SPI0_SEL7	SPI2_SEL2	C1_FLG1	
PE_04	PPI0_D08	PWM2_DH	SPI2_SEL3	C2_FLG1	
PE_05	PPI0_D07	PWM2_SYNC	SPI2_SEL4	C1_FLG2	
PE_06	PPI0_D06		SPI2_SEL5	C2_FLG2	
PE_07	PPI0_D05		SPI1_SEL2	C1_FLG3	
PE_08	PPI0_D04	SPI1_SEL5	SPI1_RDY	C2_FLG3	
PE_09	PPI0_D03	PWM0_SYNC	TM0_TMR0	SMC0_D03	
PE_10	PPI0_D02	PWM2_DL	UART2_RTS	SMC0_D02	
PE_11	PPI0_D01	SPI1_SEL3	UART2_CTS	SMC0_D01	SPI1_SS
PE_12	PPI0_D00	SPI1_SEL4	SPI2_RDY	SMC0_D00	
PE_13	SPI1_CLK		PPI0_D20	SMC0_AMS1	
PE_14	SPI1_MISO		PPI0_D21	SMC0_ABE0	
PE_15	SPI1_MOSI		PPI0_D22	SMC0_ABE1	

Table 18 shows the internal timer signal routing. This table applies to both the 349-ball and 529-ball CSP_BGA packages.

Table 18. Internal Timer Signal Routing

Timer Input Signal	Internal Source
TM0_ACLK0	SYS_CLKIN1
TM0_ACI5	DAI0_CRS_PB04_O
TM0_ACLK5	DAI0_CRS_PB03_O
TM0_ACI6	DAI1_CRS_PB04_O
TM0_ACLK6	DAI1_CRS_PB03_O
TM0_ACI7	CNT0_TO
TM0_ACLK7	SYS_CLKIN0

Table 22. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	LP1_CLK	PWM0_BL	SPI0_SEL4	SMC0_ARE	
PC_01	SPI2_CLK				
PC_02	SPI2_MISO				
PC_03	SPI2_MOSI				
PC_04	SPI2_D2				
PC_05	SPI2_D3				
PC_06	SPI2_SEL1				SPI2_SS
PC_07	CAN0_RX	SPI0_SEL1		SMC0_AMS2	TM0_ACI3
PC_08	CAN0_TX			SMC0_AMS3	
PC_09	SPI0_CLK				
PC_10	SPI0_MISO				
PC_11	SPI0_MOSI				TM0_CLK
PC_12	SPI0_SEL3	SPI0_RDY	ACM0_T0	SMC0_A25	
PC_13	UART0_TX	SPI1_SEL1	ACM0_A0		
PC_14	UART0_RX		ACM0_A1		TM0_ACI0
PC_15	UART0_RTS	PPI0_FS3	ACM0_A2	SMC0_AMS0	

Table 23. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00	UART0_CTS	PPI0_D23	ACM0_A3	SMC0_D07	
PD_01	SPI0_SEL2		ACM0_A4	SMC0_AOE	SPI0_SS
PD_02	LP0_D0	PWM1_TRIP0	TRACE0_D00		
PD_03	LP0_D1	PWM1_AH	TRACE0_D01		
PD_04	LP0_D2	PWM1_AL	TRACE0_D02		
PD_05	LP0_D3	PWM1_BH	TRACE0_D03		
PD_06	LP0_D4	PWM1_BL	TRACE0_D04		
PD_07	LP0_D5	PWM1_CH	TRACE0_D05		
PD_08	LP0_D6	PWM1_CL	TRACE0_D06		TM0_ACLK1
PD_09	LP0_D7	PWM1_DH	TRACE0_D07		TM0_ACLK2
PD_10	LP0_CLK	PWM1_DL	TRACE0_CLK		
PD_11	LP0_ACK	PWM1_SYNC			
PD_12	UART2_TX		PPI0_D19	SMC0_A06	
PD_13	UART2_RX		PPI0_D18	SMC0_A05	TM0_ACI2
PD_14	PPI0_D11	PWM2_TRIP0	MLB0_CLKOUT	SMC0_D06	
PD_15	PPI0_D10	PWM2_CH		SMC0_D05	

Table 24. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	PPI0_D09	PWM2_CL		SMC0_D04	
PE_01	PPI0_FS2	SPI0_SEL5	UART1_CTS	C1_FLG0	
PE_02	PPI0_FS1	SPI0_SEL6	UART1_RTS	C2_FLG0	

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC1_BA2	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 2 Notes: No notes
$\overline{\text{DMC1\_CAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Column Address Strobe Notes: No notes
DMC1_CK	Output	C	none	none	L	VDD_DMC	Desc: DMC1 Clock Notes: No notes
DMC1_CKE	Output	B	none	none	L	VDD_DMC	Desc: DMC1 Clock enable Notes: No notes
$\overline{\text{DMC1\_CK}}$	Output	C	none	none	L	VDD_DMC	Desc: DMC1 Clock (complement) Notes: No notes
$\overline{\text{DMC1\_CS0}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Chip Select 0 Notes: No notes
DMC1_DQ00	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 0 Notes: No notes
DMC1_DQ01	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 1 Notes: No notes
DMC1_DQ02	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 2 Notes: No notes
DMC1_DQ03	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 3 Notes: No notes
DMC1_DQ04	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 4 Notes: No notes
DMC1_DQ05	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 5 Notes: No notes
DMC1_DQ06	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 6 Notes: No notes
DMC1_DQ07	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 7 Notes: No notes
DMC1_DQ08	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 8 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PD_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 8 | LP0 Data 6 | PWM1 Channel C Low Side | TRACE0 Trace Data 6 | TIMER0 Alternate Clock 1 Notes: No notes
PD_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 9 | LP0 Data 7 | PWM1 Channel D High Side | TRACE0 Trace Data 7 | TIMER0 Alternate Clock 2 Notes: No notes
PD_10	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTD Position 10 | LP0 Clock | PWM1 Channel D Low Side | TRACE0 Trace Clock Notes: No notes
PD_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 11 | LP0 Acknowledge | PWM1 PWMTMR Grouped Notes: No notes
PD_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 12 | EPPI0 Data 19|SMC0 Address 6|UART2 Transmit Notes: No notes
PD_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 13 | EPPI0 Data 18|SMC0 Address 5|UART2 Receive | TIMER0 Alternate Capture Input 2 Notes: No notes
PD_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 14 | EPPI0 Data 11 | MLB0 Single-Ended Clock Out | PWM2 Shutdown Input 0 | SMC0 Data 6 Notes: No notes
PD_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 15 | EPPI0 Data 10 | PWM2 Channel C High Side | SMC0 Data 5 Notes: No notes
PE_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 0 | EPPI0 Data 9 | PWM2 Channel C Low Side | SMC0 Data 4 Notes: No notes
PE_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 1 | EPPI0 Frame Sync 2 (VSYNC) | SPI0 Slave Select Output 5 | SHARC Core 1 Flag Pin | UART1 Clear to Send Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 12 | EPPI0 Data 0 | SMC0 Data 0 | SPI1 Slave Select Output 4 | SPI2 Ready Notes: No notes
PE_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 13 | EPPI0 Data 20 | SMC0 Memory Select 1 | SPI1 Clock Notes: No notes
PE_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 14 | EPPI0 Data 21 | SMC0 Byte Enable 0 | SPI1 Master In, Slave Out Notes: No notes
PE_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 15 | EPPI0 Data 22 | SMC0 Byte Enable 1 | SPI1 Master Out, Slave In Notes: No notes
PF_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 0 | SPI1 Slave Select Output 6 | TIMER0 Timer 6 Notes: No notes
PF_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 1 | SPI1 Slave Select Output 7 | TIMER0 Timer 7 Notes: No notes
PF_02	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 2 | HADC0 End of Conversion / Serial Data Out | MSI0 Data 0 Notes: No notes
PF_03	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 3 | HADC0 Controls to external multiplexer | MSI0 Data 1 Notes: No notes
PF_04	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 4 | HADC0 Controls to external multiplexer | MSI0 Data 2 Notes: No notes
PF_05	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 5 | HADC0 Controls to external multiplexer | MSI0 Data 3 Notes: No notes
PF_06	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 6 | MSI0 Data 4 | PWM2 Channel A Low Side Notes: No notes
PF_07	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 7 | MSI0 Data 5 | PWM2 Channel A High Side Notes: No notes

Clock Related Operating Conditions

Table 29 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the table applies to all speed grades except where noted.

Table 29. Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$			450	MHz
f_{SYSCLK}	SYSCLK Frequency				225	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$	30		112.5	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			112.5	MHz
f_{DCLK}	LPDDR Clock Frequency				200	MHz
f_{DCLK}	DDR2 Clock Frequency				400	MHz
f_{DCLK}	DDR3 Clock Frequency				450	MHz
f_{OCLK}	Output Clock Frequency[2]				225	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[3, 4]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				75	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				45	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[5]	$f_{PCLKEXT} \leq f_{SCLK1}$			75	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[5, 6]	$f_{PCLKEXT} \leq f_{SCLK1}$			45	MHz
$f_{LCLKTPROG}$	Programmed Link Port Transmit Clock				150	MHz
$f_{LCLKREXT}$	External Link Port Receive Clock[5, 6]	$f_{LCLKEXT} \leq f_{CLKO8}$			150	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				56.25	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				28.125	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[5, 6]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			56.25	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[5, 6]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			28.125	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				75	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				75	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[5, 6]	$f_{SPICLKEXT} \leq f_{SCLK1}$			75	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[5, 6]	$f_{SPICLKEXT} \leq f_{SCLK1}$			45	MHz
$f_{ACLKPROG}$	Programmed ACM Clock				56.25	MHz

[1] The minimum frequency for SCLK0 applies only when using the USB.
[2] f_{OCLK} must not exceed f_{SCLK0} when selected as SYS_CLKOUT.
[3] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors, the measured jitter may be higher or lower than this typical specification for each end application.
[4] The typical value is the percentage of the SYS_CLKOUT period.
[5] The maximum achievable frequency for any peripheral in external clock mode is dependent on the ability to meet the setup and hold times in the ac timing specifications section for that peripheral.
[6] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} (f_{SCLK0} or f_{SCLK1}) that clocks the peripheral.

Mobile DDR (LPDDR) SDRAM Clock and Control Cycle Timing

Table 54 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the DMC.

Table 54. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	1		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

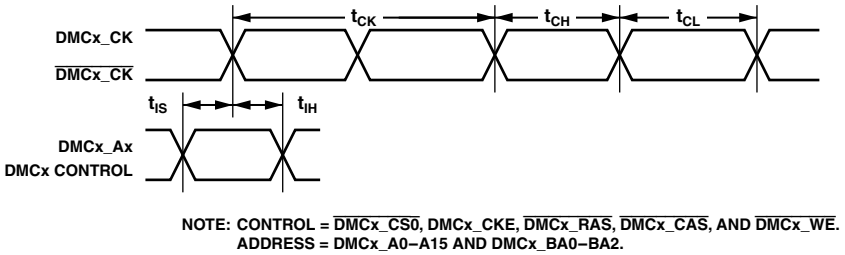

Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Read Cycle Timing

Table 55 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the DMC.

Table 55. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	Max	Unit
Timing Requirements				
t_{QH}	DMCx_DQ, DMCx_DQS Output Hold Time From DMCx_DQS	1.75		ns
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQ Signals		0.4	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

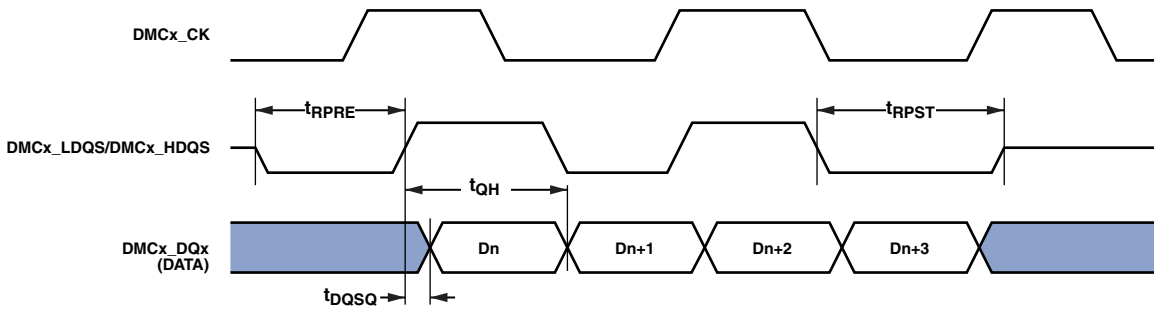

Figure 21. Mobile DDR SDRAM Controller Input AC Timing

DDR3 SDRAM Clock and Control Cycle Timing

Table 57 and Figure 23 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 57. DDR3 SDRAM Clock and Control Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[3]	Minimum Clock Pulse Width	0.43	0.57	t_{CK}
$t_{CL(abs)}$[3]	Maximum Clock Pulse Width	0.43	0.57	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	0.275		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-3F definition.

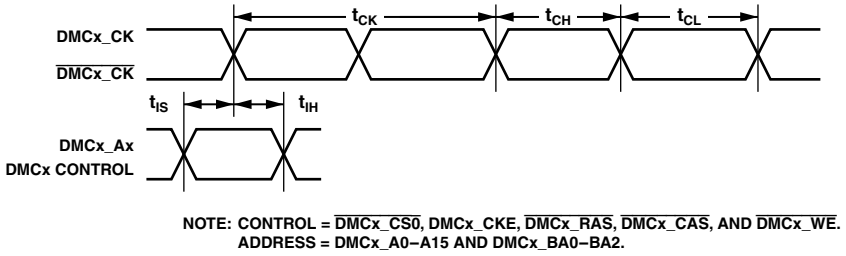

Figure 23. DDR3 SDRAM Clock and Control Cycle Timing

SPI Port—SPIx_RDY Slave Timing

SPIx_RDY is used to provide flow control. CPOL, CPHA, and FCCH are configuration bits in the SPIx_CTL register.

Table 73. SPI Port—SPIx_RDY Slave Timing[1]

Parameter		Conditions	Min	Max	Unit
Switching Characteristic					
$t_{DSPISCKRDYS}$	SPIx_RDY Deassertion from Last Valid Input SPIx_CLK Edge	FCCH = 0	$3 \times t_{SCLK1}$	$4 \times t_{SCLK1} + 10$	ns
		FCCH = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.

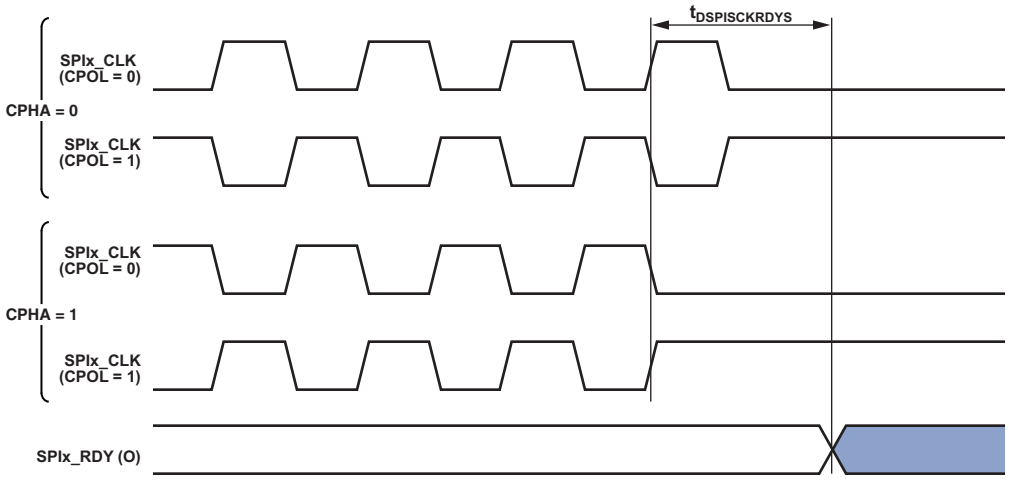

Figure 45. SPIx_RDY Deassertion from Valid Input SPIx_CLK Edge in Slave Mode

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 76. SPI Port—SPIx_RDY Master Timing[1]

Parameter		Conditions	Min	Max	Unit
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	Baud = 0, CPHA = 0	$4.5 \times t_{SCLK1}$	$5.5 \times t_{SCLK1} + 10$	ns
		Baud = 0, CPHA = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 0	$(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 1	$(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

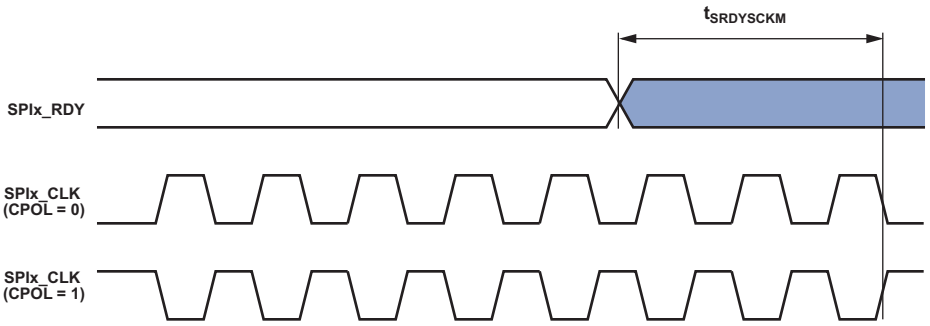

Figure 48. SPIx_RDY Setup Before SPIx_CLK

General-Purpose I/O Port Timing

Table 78 and Figure 51 describe I/O timing, related to the general-purpose I/O port (PORT).

Table 78. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

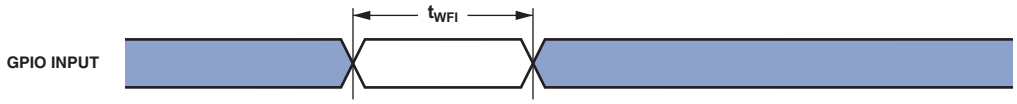

Figure 51. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 79, Table 80, and Figure 52 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of $f_{SCLK}/4$ MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 79. Timer Cycle Timing (Internal Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)[2]	$t_{SCLK} \times WIDTH - 1.5$	$t_{SCLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Table 80. Timer Cycle Timing (External Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times WIDTH - 1.5$	$t_{EXT\_CLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency see the $f_{TMRCLKEXT}$ specification in Table 29.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

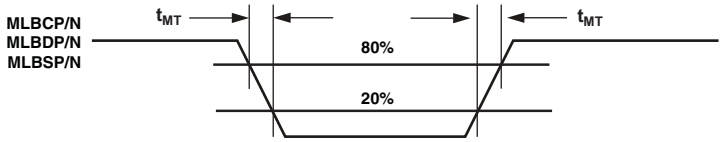

Figure 70. MLB 6-Pin Transition Time

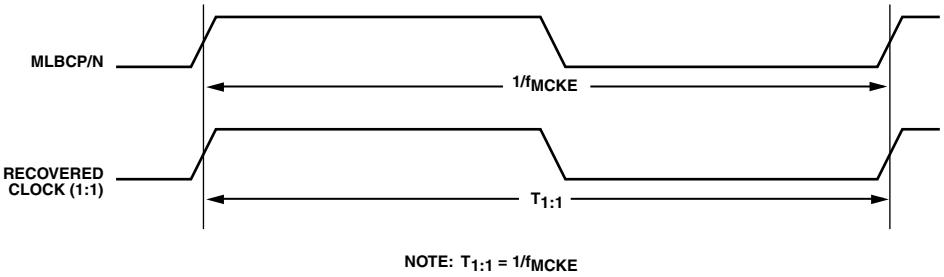

Figure 71. MLB 6-Pin Clock Definitions

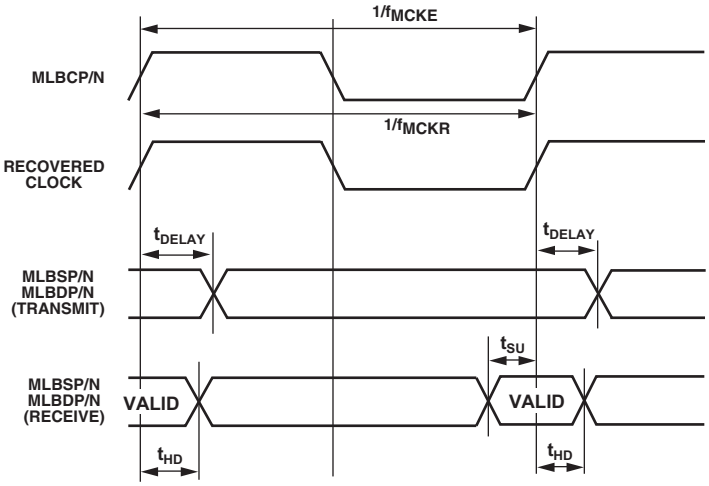

Figure 72. MLB 6-Pin Delay, Setup, and Hold Times

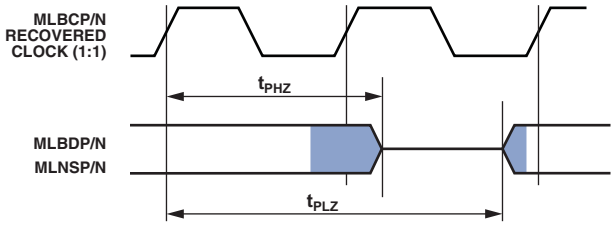

Figure 73. MLB 6-Pin Disable and Enable Turnaround Times

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
PF_11	K21	VDD_DMC	G13	VDD_INT	E10	VDD_INT	W16
PF_12	P22	VDD_DMC	G14	VDD_INT	E11	VDD_INT	W17
PF_13	R23	VDD_DMC	G15	VDD_INT	E12	VDD_INT	W18
PF_14	J21	VDD_DMC	G16	VDD_INT	E13	VDD_INT	W19
PF_15	P21	VDD_DMC	G17	VDD_INT	E14	VDD_PCIE	W07
PG_00	P23	VDD_DMC	G18	VDD_INT	E15	VDD_PCIE_RX	V07
PG_01	R20	VDD_DMC	H06	VDD_INT	E16	VDD_PCIE_TX	V08
PG_02	T22	VDD_DMC	H07	VDD_INT	E17	VDD_RTC	W14
PG_03	T21	VDD_DMC	H08	VDD_INT	E18	VDD_USB	Y08
PG_04	R22	VDD_DMC	H09	VDD_INT	F07		
PG_05	R21	VDD_DMC	H10	VDD_INT	F08		
RTC0_CLKIN	AC15	VDD_DMC	H11	VDD_INT	F10		
RTC0_XTAL	AB15	VDD_DMC	H12	VDD_INT	F11		
SYS_BMODE0	R04	VDD_DMC	H13	VDD_INT	F12		
SYS_BMODE1	R02	VDD_DMC	H14	VDD_INT	F13		
SYS_BMODE2	R03	VDD_DMC	H15	VDD_INT	F14		
SYS_CLKIN0	V01	VDD_DMC	H16	VDD_INT	F15		
SYS_CLKIN1	T01	VDD_DMC	H17	VDD_INT	F17		
SYS_CLKOUT	H20	VDD_DMC	H18	VDD_INT	F18		
SYS_FAULT	P03	VDD_DMC	J06	VDD_INT	F19		
$\overline{\text{SYS\_FAULT}}$	M04	VDD_DMC	K06	VDD_INT	G05		
$\overline{\text{SYS\_HWRST}}$	N03	VDD_DMC	L06	VDD_INT	G19		
$\overline{\text{SYS\_RESOUT}}$	U02	VDD_DMC	M06	VDD_INT	H05		
SYS_XTAL0	U01	VDD_EXT	J18	VDD_INT	H19		
SYS_XTAL1	R01	VDD_EXT	K18	VDD_INT	J05		
TWI0_SCL	Y10	VDD_EXT	L18	VDD_INT	K05		
TWI0_SDA	AB11	VDD_EXT	M18	VDD_INT	K19		
TWI1_SCL	AA10	VDD_EXT	N06	VDD_INT	L05		
TWI1_SDA	AA11	VDD_EXT	N18	VDD_INT	L19		
TWI2_SCL	AB10	VDD_EXT	P06	VDD_INT	M05		
TWI2_SDA	Y11	VDD_EXT	P18	VDD_INT	N05		
USB0_DM	AC11	VDD_EXT	R06	VDD_INT	N19		
USB0_DP	AC10	VDD_EXT	R18	VDD_INT	P05		
USB0_ID	Y07	VDD_EXT	T06	VDD_INT	R05		
USB0_VBC	Y09	VDD_EXT	T18	VDD_INT	R19		
USB0_VBUS	AA09	VDD_EXT	U06	VDD_INT	T05		
USB1_DM	AC08	VDD_EXT	U18	VDD_INT	T19		
USB1_DP	AC09	VDD_EXT	V06	VDD_INT	U05		
USB1_VBUS	AA08	VDD_EXT	V09	VDD_INT	V05		
USB_CLKIN	AB09	VDD_EXT	V10	VDD_INT	V19		
USB_XTAL	AB08	VDD_EXT	V11	VDD_INT	W05		
VDD_DMC	G06	VDD_EXT	V13	VDD_INT	W06		
VDD_DMC	G07	VDD_EXT	V14	VDD_INT	W08		
VDD_DMC	G08	VDD_EXT	V15	VDD_INT	W09		
VDD_DMC	G09	VDD_EXT	V16	VDD_INT	W10		
VDD_DMC	G10	VDD_EXT	V17	VDD_INT	W11		
VDD_DMC	G11	VDD_EXT	V18	VDD_INT	W13		
VDD_DMC	G12	VDD_HADC	AC13	VDD_INT	W15		

PLANNED AUTOMOTIVE PRODUCTION PRODUCTS

Model [1, 2]	Processor Instruction Rate (Max)	Temperature Range[3]	ARM Cores[4]	SHARC+ Cores	SHARC+ SRAM	PCIe Lanes[4]	Package Description	Package Option
AD21583WCBCZ4Axx	450 MHz	–40°C to +105°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
AD21584WCBCZ4Axx	450 MHz	–40°C to +105°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC582WCBCZ4Axx	450 MHz	–40°C to +105°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC583WCBCZ3Axx	300 MHz	–40°C to +105°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC583WCBCZ4Axx	450 MHz	–40°C to +105°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC584WCBCZ3Axx	300 MHz	–40°C to +105°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC584WCBCZ4Axx	450 MHz	–40°C to +105°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSC587WCBCZ4Bxx	450 MHz	–40°C to +90°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1

[1] Z = RoHS Compliant Part.
[2] xx denotes the current die revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.
[4] N/A means not applicable.

ORDERING GUIDE

Model[1]	Processor Instruction Rate (Max)	Temperature Range[2]	ARM Cores[3]	SHARC+ Cores	SHARC+ SRAM	PCIe Lanes[3]	Package Description	Package Option
ADSP-21583KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21587KBCZ-4B	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-21587BBCZ-4B	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC582KBCZ-4A	450 MHz	0°C to +70°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582BBCZ-4A	450 MHz	–40°C to +85°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582CBCZ-4A	450 MHz	–40°C to +95°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-3A	300 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-3A	300 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-3A	300 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-4A	450 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-4A	450 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-4A	450 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-3A	300 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-3A	300 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-3A	300 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-4A	450 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-4A	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-4A	450 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC587KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC587BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC589KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1
ADSP-SC589BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1

[1] Z =RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.

[3] N/A means not applicable.