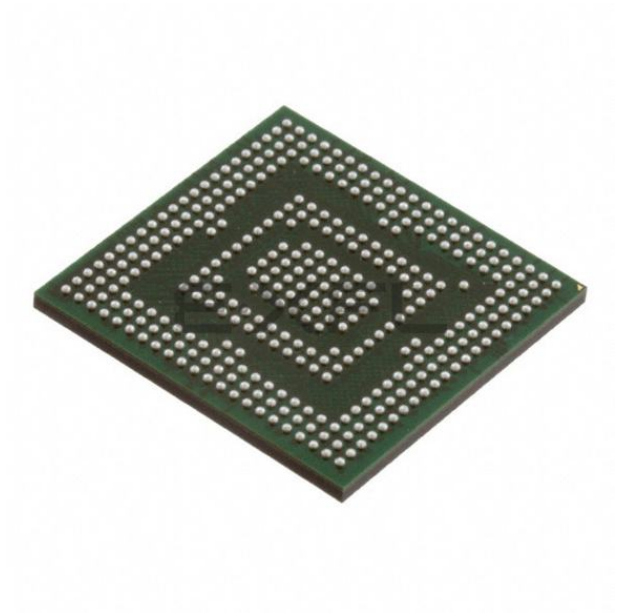

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsc583wcbcz3a10

blocks on the processor. The digital audio interface carries three types of information: audio data, nonaudio data (compressed data), and timing information.

The S/PDIF interface supports one stereo channel or compressed audio streams. The S/PDIF transmitter and receiver are AES3 compliant and support the sample rate from 24 KHz to 192 KHz. The S/PDIF receiver supports professional jitter standards.

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S, or right justified with word widths of 16, 18, 20, or 24 bits. The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from various sources, such as the SPORTs, external pins, and the precision clock generators (PCGs), and are controlled by the SRU control registers.

Precision Clock Generators (PCG)

The precision clock generators (PCG) consist of four units: units A/B located in the DAI0 block, and units C/D located in the DAI1 block. The PCG can generate a pair of signals (clock and frame sync) derived from a clock input signal (CLKIN1-0, SCLK0, or DAI pin buffer). Each unit can also access the opposite DAI unit. All units are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Enhanced Parallel Peripheral Interface (EPPI)

The processors provide an enhanced parallel peripheral interface (EPPI) that supports data widths up to 24 bits. The EPPI supports direct connection to TFT LCD panels, parallel ADCs and DACs, video encoders and decoders, image sensor modules, and other general-purpose peripherals.

The features supported in the EPPI module include the following:

- Programmable data length of 8 bits, 10 bits, 12 bits, 14 bits, 16 bits, 18 bits, and 24 bits per clock.
- Various framed, nonframed, and general-purpose operating modes. Frame syncs can be generated internally or can be supplied by an external device.
- ITU-656 status word error detection and correction for ITU-656 receive modes and ITU-656 preamble and status word decoding.
- Optional packing and unpacking of data to/from 32 bits from/to 8 bits, 16 bits, and 24 bits. If packing/unpacking is enabled, configure endianness to change the order of packing/unpacking of the bytes/words.
- RGB888 can be converted to RGB666 or RGB565 for transmit modes.
- Various deinterleaving/interleaving modes for receiving/transmitting 4:2:2 YCrCb data.
- Configurable LCD data enable output available on Frame Sync 3.

Universal Asynchronous Receiver/Transmitter (UART) Ports

The processors provide three full-duplex universal asynchronous receiver/transmitter (UART) ports, fully compatible with PC standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits as well as no parity, even parity, or odd parity.

Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multidrop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion first in, first out (FIFO) levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable interframe space.

Serial Peripheral Interface (SPI) Ports

The processors have three industry-standard SPI-compatible ports that allow the processors to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, four-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An extra two (optional) data pins are provided to support quad SPI operation. Enhanced modes of operation, such as flow control, fast mode, and dual-I/O mode (DIOM), are also supported. A direct memory access (DMA) mode allows for transferring several words with minimal central processing unit (CPU) interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other devices, acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI_RDY) which flexibly controls the transfers.

The baud rate and clock phase/polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

Link Ports (LP)

Two 8-bit wide link ports (LP) can connect to the link ports of other DSPs or peripherals. LP are bidirectional ports that have eight data lines, an acknowledge line, and a clock line.

- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, RMII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Controller Area Network (CAN)

There are two controller area network (CAN) modules. A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to the capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on the first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- Interrupts, including transmit and receive complete, error, and global

An additional crystal is not required to supply the CAN clock because it is derived from a system clock through a programmable divider.

Timers

The processors include several timers that are described in the following sections.

General-Purpose (GP) Timers (TIMER)

There is one general-purpose (GP) timer unit, providing eight general-purpose programmable timers. Each timer has an external pin that can be configured either as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM_TMR[n] pins, an external TM_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and/or stopped by any TRU master without core intervention.

Watchdog Timer (WDT)

Two on-chip software watchdog timers (WDT) can be used by the ARM Cortex-A5 and/or SHARC+ cores. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

General-Purpose Counters (CNT)

A 32-bit counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

PCI Express (PCIe)

A PCI express interface (PCIe) is available on some product variants (see Table 2 and Table 3). This single, bidirectional lane can be configured to be either a root complex (RC) or end point (EP) system. The PCIe interface has the following features:

- Compliance with the *PCI Express Base Specification 3.0*
- Support for transfers at either 2.5 Gbps (Gen 1) or 5.0 Gbps (Gen 2) in each direction
- Support for 8b/10b encode and decode
- Lane reversal and lane polarity inversion
- Flow control of data in both the transmit and receive directions
- Support for removal of corrupted packets for error detection and recovery
- Maximum transaction payload of 256 bytes

Housekeeping Analog-to-Digital Converter (HADC)

The housekeeping analog-to-digital converter (HADC) provides a general-purpose, multichannel successive approximation ADC. It supports the following set of features:

- 12-bit ADC core (10-bit accuracy) with built in sample and hold.
- Eight single-ended input channels that can be extended to 15 channels by adding an external channel multiplexer.
- Throughput rates up to 1 MSPS.

This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in circuit programming of the on-board Flash device to store user specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend the capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product.

Middleware Packages

Analog Devices offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos2
- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/ucusbh
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see "Analog Devices JTAG Emulation Technical Reference" (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-SC58x/ADSP-2158x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D02	SMC0 Data 2	E	PE_10
SMC0_D03	SMC0 Data 3	E	PE_09
SMC0_D04	SMC0 Data 4	E	PE_00
SMC0_D05	SMC0 Data 5	D	PD_15
SMC0_D06	SMC0 Data 6	D	PD_14
SMC0_D07	SMC0 Data 7	D	PD_00
SMC0_D08	SMC0 Data 8	B	PB_14
SMC0_D09	SMC0 Data 9	B	PB_13
SMC0_D10	SMC0 Data 10	B	PB_12
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_10
SMC0_D13	SMC0 Data 13	B	PB_09
SMC0_D14	SMC0 Data 14	B	PB_08
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_10
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_11
SPI0_RDY	SPI0 Ready	C	PC_12
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_07
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	D	PD_01
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	C	PC_12
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	C	PC_00
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	E	PE_01
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	E	PE_02
$\overline{\text{SPI0\_SEL7}}$	SPI0 Slave Select Output 7	E	PE_03
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	D	PD_01
SPI1_CLK	SPI1 Clock	E	PE_13
SPI1_MISO	SPI1 Master In, Slave Out	E	PE_14
SPI1_MOSI	SPI1 Master Out, Slave In	E	PE_15
SPI1_RDY	SPI1 Ready	E	PE_08
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_13
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	E	PE_07
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	E	PE_11
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	E	PE_12
$\overline{\text{SPI1\_SEL5}}$	SPI1 Slave Select Output 5	E	PE_08
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	E	PE_11
SPI2_CLK	SPI2 Clock	C	PC_01
SPI2_D2	SPI2 Data 2	C	PC_04
SPI2_D3	SPI2 Data 3	C	PC_05
SPI2_MISO	SPI2 Master In, Slave Out	C	PC_02
SPI2_MOSI	SPI2 Master Out, Slave In	C	PC_03
SPI2_RDY	SPI2 Ready	E	PE_12
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	C	PC_06
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	E	PE_03
$\overline{\text{SPI2\_SEL3}}$	SPI2 Slave Select Output 3	E	PE_04
$\overline{\text{SPI2\_SEL4}}$	SPI2 Slave Select Output 4	E	PE_05
$\overline{\text{SPI2\_SEL5}}$	SPI2 Slave Select Output 5	E	PE_06
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	C	PC_06

Table 15. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	LP1_CLK	PWM0_BL	SPI0_SEL4	SMC0_ARE	
PC_01	SPI2_CLK				
PC_02	SPI2_MISO				
PC_03	SPI2_MOSI				
PC_04	SPI2_D2				
PC_05	SPI2_D3				
PC_06	SPI2_SEL1				SPI2_SS
PC_07	CAN0_RX	SPI0_SEL1		SMC0_AMS2	TM0_ACI3
PC_08	CAN0_TX			SMC0_AMS3	
PC_09	SPI0_CLK				
PC_10	SPI0_MISO				
PC_11	SPI0_MOSI				TM0_CLK
PC_12	SPI0_SEL3	SPI0_RDY	ACM0_T0	SMC0_A25	
PC_13	UART0_TX	SPI1_SEL1	ACM0_A0		
PC_14	UART0_RX		ACM0_A1		TM0_ACI0
PC_15	UART0_RTS	PPI0_FS3	ACM0_A2	SMC0_AMS0	

Table 16. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00	UART0_CTS	PPI0_D23	ACM0_A3	SMC0_D07	
PD_01	SPI0_SEL2		ACM0_A4	SMC0_AOE	SPI0_SS
PD_02	LP0_D0	PWM1_TRIP0	TRACE0_D00		
PD_03	LP0_D1	PWM1_AH	TRACE0_D01		
PD_04	LP0_D2	PWM1_AL	TRACE0_D02		
PD_05	LP0_D3	PWM1_BH	TRACE0_D03		
PD_06	LP0_D4	PWM1_BL	TRACE0_D04		
PD_07	LP0_D5	PWM1_CH	TRACE0_D05		
PD_08	LP0_D6	PWM1_CL	TRACE0_D06		TM0_ACLK1
PD_09	LP0_D7	PWM1_DH	TRACE0_D07		TM0_ACLK2
PD_10	LP0_CLK	PWM1_DL	TRACE0_CLK		
PD_11	LP0_ACK	PWM1_SYNC			
PD_12	UART2_TX		PPI0_D19	SMC0_A06	
PD_13	UART2_RX		PPI0_D18	SMC0_A05	TM0_ACI2
PD_14	PPI0_D11	PWM2_TRIP0	MLB0_CLKOUT	SMC0_D06	
PD_15	PPI0_D10	PWM2_CH		SMC0_D05	

529-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown Table 19 for the 529-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference for complete information on the use of the DAIs and SRUs.

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	C	PC_13
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	D	PD_00
ACM0_A4	ACM0 ADC Control Signals	D	PD_01
ACM0_T0	ACM0 External Trigger n	C	PC_12
C1_FLG0	SHARC Core 1 Flag Pin	E	PE_01
C1_FLG1	SHARC Core 1 Flag Pin	E	PE_03
C1_FLG2	SHARC Core 1 Flag Pin	E	PE_05
C1_FLG3	SHARC Core 1 Flag Pin	E	PE_07
C2_FLG0	SHARC Core 2 Flag Pin	E	PE_02
C2_FLG1	SHARC Core 2 Flag Pin	E	PE_04
C2_FLG2	SHARC Core 2 Flag Pin	E	PE_06
C2_FLG3	SHARC Core 2 Flag Pin	E	PE_08
CAN0_RX	CAN0 Receive	C	PC_07
CAN0_TX	CAN0 Transmit	C	PC_08
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_09
CNT0_DG	CNT0 Count Down and Gate	B	PB_14
CNT0_UD	CNT0 Count Up and Direction	B	PB_12
CNT0_ZM	CNT0 Count Zero Marker	B	PB_11
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN13	DAI0 Pin 13	Not Muxed	DAI0_PIN13
DAI0_PIN14	DAI0 Pin 14	Not Muxed	DAI0_PIN14

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC1_BA2	DMC1 Bank Address 2	Not Muxed	DMC1_BA2
$\overline{\text{DMC1\_CAS}}$	DMC1 Column Address Strobe	Not Muxed	$\overline{\text{DMC1\_CAS}}$
DMC1_CK	DMC1 Clock	Not Muxed	DMC1_CK
DMC1_CKE	DMC1 Clock enable	Not Muxed	DMC1_CKE
$\overline{\text{DMC1\_CK}}$	DMC1 Clock (complement)	Not Muxed	$\overline{\text{DMC1\_CK}}$
$\overline{\text{DMC1\_CS0}}$	DMC1 Chip Select 0	Not Muxed	$\overline{\text{DMC1\_CS0}}$
DMC1_DQ00	DMC1 Data 0	Not Muxed	DMC1_DQ00
DMC1_DQ01	DMC1 Data 1	Not Muxed	DMC1_DQ01
DMC1_DQ02	DMC1 Data 2	Not Muxed	DMC1_DQ02
DMC1_DQ03	DMC1 Data 3	Not Muxed	DMC1_DQ03
DMC1_DQ04	DMC1 Data 4	Not Muxed	DMC1_DQ04
DMC1_DQ05	DMC1 Data 5	Not Muxed	DMC1_DQ05
DMC1_DQ06	DMC1 Data 6	Not Muxed	DMC1_DQ06
DMC1_DQ07	DMC1 Data 7	Not Muxed	DMC1_DQ07
DMC1_DQ08	DMC1 Data 8	Not Muxed	DMC1_DQ08
DMC1_DQ09	DMC1 Data 9	Not Muxed	DMC1_DQ09
DMC1_DQ10	DMC1 Data 10	Not Muxed	DMC1_DQ10
DMC1_DQ11	DMC1 Data 11	Not Muxed	DMC1_DQ11
DMC1_DQ12	DMC1 Data 12	Not Muxed	DMC1_DQ12
DMC1_DQ13	DMC1 Data 13	Not Muxed	DMC1_DQ13
DMC1_DQ14	DMC1 Data 14	Not Muxed	DMC1_DQ14
DMC1_DQ15	DMC1 Data 15	Not Muxed	DMC1_DQ15
DMC1_LDM	DMC1 Data Mask for Lower Byte	Not Muxed	DMC1_LDM
DMC1_LDQS	DMC1 Data Strobe for Lower Byte	Not Muxed	DMC1_LDQS
$\overline{\text{DMC1\_LDQS}}$	DMC1 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC1\_LDQS}}$
DMC1_ODT	DMC1 On-die termination	Not Muxed	DMC1_ODT
$\overline{\text{DMC1\_RAS}}$	DMC1 Row Address Strobe	Not Muxed	$\overline{\text{DMC1\_RAS}}$
$\overline{\text{DMC1\_RESET}}$	DMC1 Reset (DDR3 only)	Not Muxed	$\overline{\text{DMC1\_RESET}}$
DMC1_RZQ	DMC1 External calibration resistor connection	Not Muxed	DMC1_RZQ
DMC1_UDM	DMC1 Data Mask for Upper Byte	Not Muxed	DMC1_UDM
DMC1_UDQS	DMC1 Data Strobe for Upper Byte	Not Muxed	DMC1_UDQS
$\overline{\text{DMC1\_UDQS}}$	DMC1 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC1\_UDQS}}$
DMC1_VREF	DMC1 Voltage Reference	Not Muxed	DMC1_VREF
$\overline{\text{DMC1\_WE}}$	DMC1 Write Enable	Not Muxed	$\overline{\text{DMC1\_WE}}$
ETH0_CRS	ETH0 Carrier Sense/RMII Receive Data Valid	A	PA_07
ETH0_MDC	ETH0 Management Channel Clock	A	PA_02
ETH0_MDIO	ETH0 Management Channel Serial Data	A	PA_03
ETH0_PTPAUXIN0	ETH0 PTP Auxiliary Trigger Input 0	B	PB_03
ETH0_PTPAUXIN1	ETH0 PTP Auxiliary Trigger Input 1	B	PB_04
ETH0_PTPAUXIN2	ETH0 PTP Auxiliary Trigger Input 2	B	PB_05
ETH0_PTPAUXIN3	ETH0 PTP Auxiliary Trigger Input 3	B	PB_06
ETH0_PTPCLKIN0	ETH0 PTP Clock Input 0	B	PB_02
ETH0_PTPPPS0	ETH0 PTP Pulse-Per-Second Output 0	B	PB_01
ETH0_PTPPPS1	ETH0 PTP Pulse-Per-Second Output 1	B	PB_00
ETH0_PTPPPS2	ETH0 PTP Pulse-Per-Second Output 2	A	PA_15
ETH0_PTPPPS3	ETH0 PTP Pulse-Per-Second Output 3	A	PA_14
ETH0_RXCLK_REFCLK	ETH0 RXCLK (GigE) or REFCLK (10/100)	A	PA_06
ETH0_RXCTL_CRS	ETH0 RXCTL (GigE) or CRS (10/100)	A	PA_07

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D00	EPPI0 Data 0	E	PE_12
PPI0_D01	EPPI0 Data 1	E	PE_11
PPI0_D02	EPPI0 Data 2	E	PE_10
PPI0_D03	EPPI0 Data 3	E	PE_09
PPI0_D04	EPPI0 Data 4	E	PE_08
PPI0_D05	EPPI0 Data 5	E	PE_07
PPI0_D06	EPPI0 Data 6	E	PE_06
PPI0_D07	EPPI0 Data 7	E	PE_05
PPI0_D08	EPPI0 Data 8	E	PE_04
PPI0_D09	EPPI0 Data 9	E	PE_00
PPI0_D10	EPPI0 Data 10	D	PD_15
PPI0_D11	EPPI0 Data 11	D	PD_14
PPI0_D12	EPPI0 Data 12	B	PB_04
PPI0_D13	EPPI0 Data 13	B	PB_05
PPI0_D14	EPPI0 Data 14	B	PB_00
PPI0_D15	EPPI0 Data 15	B	PB_01
PPI0_D16	EPPI0 Data 16	B	PB_02
PPI0_D17	EPPI0 Data 17	B	PB_03
PPI0_D18	EPPI0 Data 18	D	PD_13
PPI0_D19	EPPI0 Data 19	D	PD_12
PPI0_D20	EPPI0 Data 20	E	PE_13
PPI0_D21	EPPI0 Data 21	E	PE_14
PPI0_D22	EPPI0 Data 22	E	PE_15
PPI0_D23	EPPI0 Data 23	D	PD_00
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_02
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_01
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_15
PWM0_AH	PWM0 Channel A High Side	B	PB_07
PWM0_AL	PWM0 Channel A Low Side	B	PB_08
PWM0_BH	PWM0 Channel B High Side	B	PB_06
PWM0_BL	PWM0 Channel B Low Side	C	PC_00
PWM0_CH	PWM0 Channel C High Side	B	PB_13
PWM0_CL	PWM0 Channel C Low Side	B	PB_14
PWM0_DH	PWM0 Channel D High Side	B	PB_11
PWM0_DL	PWM0 Channel D Low Side	B	PB_12
PWM0_SYNC	PWM0 PWMTMR Grouped	E	PE_09
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	B	PB_15
PWM1_AH	PWM1 Channel A High Side	D	PD_03
PWM1_AL	PWM1 Channel A Low Side	D	PD_04
PWM1_BH	PWM1 Channel B High Side	D	PD_05
PWM1_BL	PWM1 Channel B Low Side	D	PD_06
PWM1_CH	PWM1 Channel C High Side	D	PD_07
PWM1_CL	PWM1 Channel C Low Side	D	PD_08
PWM1_DH	PWM1 Channel D High Side	D	PD_09
PWM1_DL	PWM1 Channel D Low Side	D	PD_10
PWM1_SYNC	PWM1 PWMTMR Grouped	D	PD_11
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	D	PD_02
PWM2_AH	PWM2 Channel A High Side	F	PF_07

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_AMS2	SMC0 Memory Select 2	C	PC_07
SMC0_AMS3	SMC0 Memory Select 3	C	PC_08
SMC0_AOE	SMC0 Output Enable	D	PD_01
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_04
SMC0_ARE	SMC0 Read Enable	C	PC_00
SMC0_AWE	SMC0 Write Enable	B	PB_15
SMC0_D00	SMC0 Data 0	E	PE_12
SMC0_D01	SMC0 Data 1	E	PE_11
SMC0_D02	SMC0 Data 2	E	PE_10
SMC0_D03	SMC0 Data 3	E	PE_09
SMC0_D04	SMC0 Data 4	E	PE_00
SMC0_D05	SMC0 Data 5	D	PD_15
SMC0_D06	SMC0 Data 6	D	PD_14
SMC0_D07	SMC0 Data 7	D	PD_00
SMC0_D08	SMC0 Data 8	B	PB_14
SMC0_D09	SMC0 Data 9	B	PB_13
SMC0_D10	SMC0 Data 10	B	PB_12
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_10
SMC0_D13	SMC0 Data 13	B	PB_09
SMC0_D14	SMC0 Data 14	B	PB_08
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_10
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_11
SPI0_RDY	SPI0 Ready	C	PC_12
SPI0_SEL1	SPI0 Slave Select Output 1	C	PC_07
SPI0_SEL2	SPI0 Slave Select Output 2	D	PD_01
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_12
SPI0_SEL4	SPI0 Slave Select Output 4	C	PC_00
SPI0_SEL5	SPI0 Slave Select Output 5	E	PE_01
SPI0_SEL6	SPI0 Slave Select Output 6	E	PE_02
SPI0_SEL7	SPI0 Slave Select Output 7	E	PE_03
SPI0_SS	SPI0 Slave Select Input	D	PD_01
SPI1_CLK	SPI1 Clock	E	PE_13
SPI1_MISO	SPI1 Master In, Slave Out	E	PE_14
SPI1_MOSI	SPI1 Master Out, Slave In	E	PE_15
SPI1_RDY	SPI1 Ready	E	PE_08
SPI1_SEL1	SPI1 Slave Select Output 1	C	PC_13
SPI1_SEL2	SPI1 Slave Select Output 2	E	PE_07
SPI1_SEL3	SPI1 Slave Select Output 3	E	PE_11
SPI1_SEL4	SPI1 Slave Select Output 4	E	PE_12
SPI1_SEL5	SPI1 Slave Select Output 5	E	PE_08
SPI1_SEL6	SPI1 Slave Select Output 6	F	PF_00
SPI1_SEL7	SPI1 Slave Select Output 7	F	PF_01
SPI1_SS	SPI1 Slave Select Input	E	PE_11
SPI2_CLK	SPI2 Clock	C	PC_01
SPI2_D2	SPI2 Data 2	C	PC_04

Table 22. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	LP1_CLK	PWM0_BL	SPI0_SEL4	SMC0_ARE	
PC_01	SPI2_CLK				
PC_02	SPI2_MISO				
PC_03	SPI2_MOSI				
PC_04	SPI2_D2				
PC_05	SPI2_D3				
PC_06	SPI2_SEL1				SPI2_SS
PC_07	CAN0_RX	SPI0_SEL1		SMC0_AMS2	TM0_ACI3
PC_08	CAN0_TX			SMC0_AMS3	
PC_09	SPI0_CLK				
PC_10	SPI0_MISO				
PC_11	SPI0_MOSI				TM0_CLK
PC_12	SPI0_SEL3	SPI0_RDY	ACM0_T0	SMC0_A25	
PC_13	UART0_TX	SPI1_SEL1	ACM0_A0		
PC_14	UART0_RX		ACM0_A1		TM0_ACI0
PC_15	UART0_RTS	PPI0_FS3	ACM0_A2	SMC0_AMS0	

Table 23. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00	UART0_CTS	PPI0_D23	ACM0_A3	SMC0_D07	
PD_01	SPI0_SEL2		ACM0_A4	SMC0_AOE	SPI0_SS
PD_02	LP0_D0	PWM1_TRIP0	TRACE0_D00		
PD_03	LP0_D1	PWM1_AH	TRACE0_D01		
PD_04	LP0_D2	PWM1_AL	TRACE0_D02		
PD_05	LP0_D3	PWM1_BH	TRACE0_D03		
PD_06	LP0_D4	PWM1_BL	TRACE0_D04		
PD_07	LP0_D5	PWM1_CH	TRACE0_D05		
PD_08	LP0_D6	PWM1_CL	TRACE0_D06		TM0_ACLK1
PD_09	LP0_D7	PWM1_DH	TRACE0_D07		TM0_ACLK2
PD_10	LP0_CLK	PWM1_DL	TRACE0_CLK		
PD_11	LP0_ACK	PWM1_SYNC			
PD_12	UART2_TX		PPI0_D19	SMC0_A06	
PD_13	UART2_RX		PPI0_D18	SMC0_A05	TM0_ACI2
PD_14	PPI0_D11	PWM2_TRIP0	MLB0_CLKOUT	SMC0_D06	
PD_15	PPI0_D10	PWM2_CH		SMC0_D05	

Table 24. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	PPI0_D09	PWM2_CL		SMC0_D04	
PE_01	PPI0_FS2	SPI0_SEL5	UART1_CTS	C1_FLG0	
PE_02	PPI0_FS1	SPI0_SEL6	UART1_RTS	C2_FLG0	

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 2 | EMAC0 Management Channel Clock | SMC0 Address 24 Notes: No notes
PA_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 3 | EMAC0 Management Channel Serial Data | SMC0 Address 23 Notes: No notes
PA_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 4 | EMAC0 Receive Data 0 | SMC0 Address 19 Notes: No notes
PA_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 5 | EMAC0 Receive Data 1 | SMC0 Address 18 Notes: No notes
PA_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 6 | EMAC0 RXCLK (GigE) or REFCLK (10/100) | SMC0 Address 17 Notes: No notes
PA_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 RXCTL (GigE) or CRS (10/100) | PORTA Position 7 | EMAC0 Carrier Sense/RMII Receive Data Valid | SMC0 Address 16 Notes: No notes
PA_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 8 | EMAC0 Receive Data 2 | SMC0 Address 12 Notes: No notes
PA_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 9 | EMAC0 Receive Data 3 | SMC0 Address 11 Notes: No notes
PA_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 TXCTL (GigE) or TXEN (10/100) | PORTA Position 10 | EMAC0 Transmit Enable | SMC0 Address 22 Notes: No notes
PA_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 11 | EMAC0 Transmit Clock | SMC0 Address 15 Notes: No notes
PA_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 12 | EMAC0 Transmit Data 2 | SMC0 Address 14 Notes: No notes
PA_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 13 | EMAC0 Transmit Data 3 | SMC0 Address 13 Notes: No notes
PA_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 14 | EMAC0 PTP Pulse-Per-Second Output 3 | SINC0 Data 0 | SMC0 Address 10 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 15 | EMAC0 PTP Pulse-Per-Second Output 2 | SINC0 Data 1 | SMC0 Address 9 Notes: No notes
PB_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 0 | EMAC0 PTP Pulse-Per-Second Output 1 | EPPI0 Data 14 | SINC0 Data 2 | SMC0 Address 8 | TIMER0 Alternate Clock 3 Notes: No notes
PB_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 1 | EMAC0 PTP Pulse-Per-Second Output 0 | EPPI0 Data 15 | SINC0 Clock 0 | SMC0 Address 7 | TIMER0 Alternate Clock 4 Notes: No notes
PB_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 2 | EMAC0 PTP Clock Input 0 | EPPI0 Data 16 | SMC0 Address 4 | UART1 Transmit Notes: No notes
PB_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 3 | EMAC0 PTP Auxiliary Trigger Input 0 | EPPI0 Data 17 | SMC0 Address 3 | UART1 Receive | TIMER0 Alternate Capture Input 1 Notes: No notes
PB_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 4 | EPPI0 Data 12 | MLB0 Single-Ended Clock | SINC0 Data 3 | SMC0 Asynchronous Ready | EMAC0 PTP Auxiliary Trigger Input 1 Notes: No notes
PB_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 5 | EPPI0 Data 13 | MLB0 Single-Ended Signal | SMC0 Address 1 | EMAC0 PTP Auxiliary Trigger Input 2 Notes: No notes
PB_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 6 | MLB0 Single-Ended Data | PWM0 Channel B High Side | SMC0 Address 2 | EMAC0 PTP Auxiliary Trigger Input 3 Notes: No notes
PB_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 7 | LP1 Data 0 | PWM0 Channel A High Side | SMC0 Data 15 | TIMER0 Timer 3 Notes: No notes
PB_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 8 | LP1 Data 1 | PWM0 Channel A Low Side | SMC0 Data 14 | TIMER0 Timer 4 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 9 | CAN1 Transmit | LP1 Data 2 | SMC0 Data 13 Notes: No notes
PB_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 10 | CAN1 Receive | LP1 Data 3 | SMC0 Data 12 | TIMER0 Timer 2 | TIMER0 Alternate Capture Input 4 Notes: No notes
PB_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 11 | LP1 Data 4 | PWM0 Channel D High Side | SMC0 Data 11 | CNT0 Count Zero Marker Notes: No notes
PB_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 12 | LP1 Data 5 | PWM0 Channel D Low Side | SMC0 Data 10 | CNT0 Count Up and Direction Notes: No notes
PB_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 13 | LP1 Data 6 | PWM0 Channel C High Side | SMC0 Data 9 Notes: No notes
PB_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 14 | LP1 Data 7 | PWM0 Channel C Low Side | SMC0 Data 8 | TIMER0 Timer 5 | CNT0 Count Down and Gate Notes: No notes
PB_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 15 | LP1 Acknowledge | PWM0 Shutdown Input 0 | SMC0 Write Enable | TIMER0 Timer 1 Notes: No notes
PCIE0_CLKM	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK - Notes: No notes
PCIE0_CLKP	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK + Notes: No notes
PCIE0_REF	a	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 Reference Notes: No notes
PCIE0_RXM	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX - Notes: No notes
PCIE0_RXP	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX + Notes: No notes
PCIE0_TXM	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX - Notes: No notes
PCIE0_TXP	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX + Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PD_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 8 | LP0 Data 6 | PWM1 Channel C Low Side | TRACE0 Trace Data 6 | TIMER0 Alternate Clock 1 Notes: No notes
PD_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 9 | LP0 Data 7 | PWM1 Channel D High Side | TRACE0 Trace Data 7 | TIMER0 Alternate Clock 2 Notes: No notes
PD_10	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTD Position 10 | LP0 Clock | PWM1 Channel D Low Side | TRACE0 Trace Clock Notes: No notes
PD_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 11 | LP0 Acknowledge | PWM1 PWMTMR Grouped Notes: No notes
PD_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 12 | EPPI0 Data 19|SMC0 Address 6|UART2 Transmit Notes: No notes
PD_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 13 | EPPI0 Data 18|SMC0 Address 5|UART2 Receive | TIMER0 Alternate Capture Input 2 Notes: No notes
PD_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 14 | EPPI0 Data 11 | MLB0 Single-Ended Clock Out | PWM2 Shutdown Input 0 | SMC0 Data 6 Notes: No notes
PD_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 15 | EPPI0 Data 10 | PWM2 Channel C High Side | SMC0 Data 5 Notes: No notes
PE_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 0 | EPPI0 Data 9 | PWM2 Channel C Low Side | SMC0 Data 4 Notes: No notes
PE_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 1 | EPPI0 Frame Sync 2 (VSYNC) | SPI0 Slave Select Output 5 | SHARC Core 1 Flag Pin | UART1 Clear to Send Notes: No notes

Asynchronous Read

Table 45 and Figure 12 show asynchronous memory read timing, related to the SMC.

Table 45. Asynchronous Read

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	5.1		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0.7		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
t_{AMSARE}	ADDR/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK0} – 2		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	(RST + PREAT) × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	RHT × t_{SCLK0} –2		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	RAT × t_{SCLK0} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$, $\overline{SMC0\_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

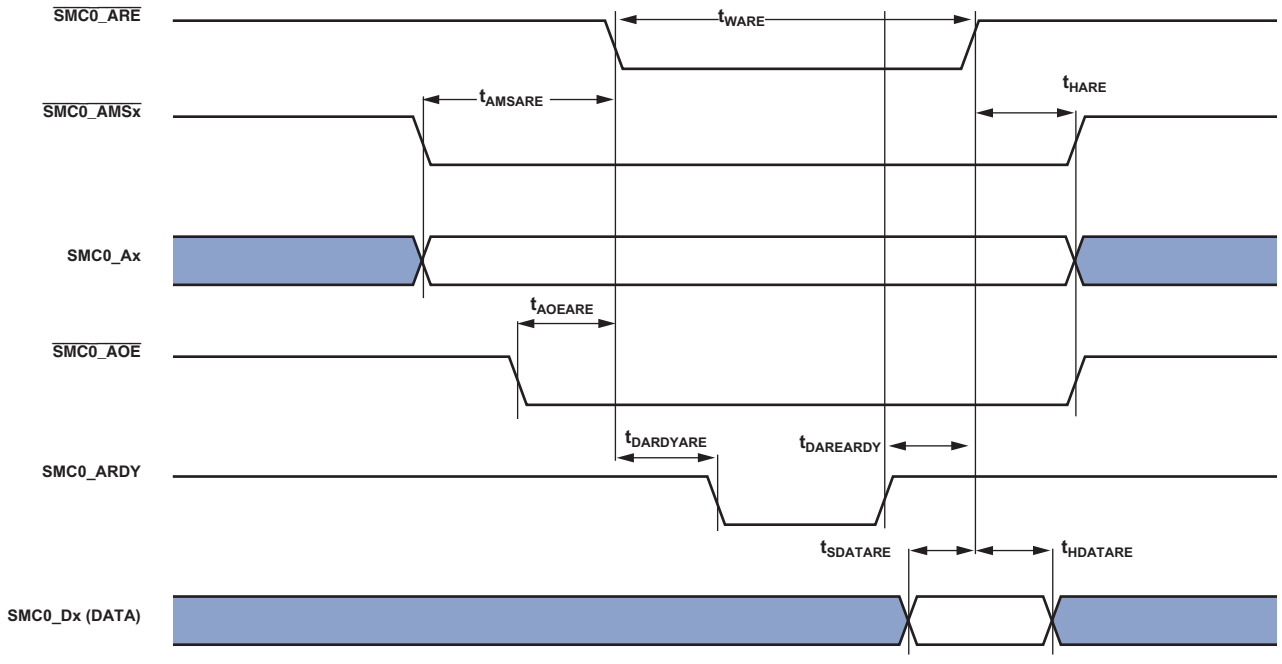

Figure 12. Asynchronous Read

SPI Port—Slave Timing

Table 72 and Figure 44 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 72. SPI Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLK} - 1$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

[1] All specifications apply to all three SPIs.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in Table 29.

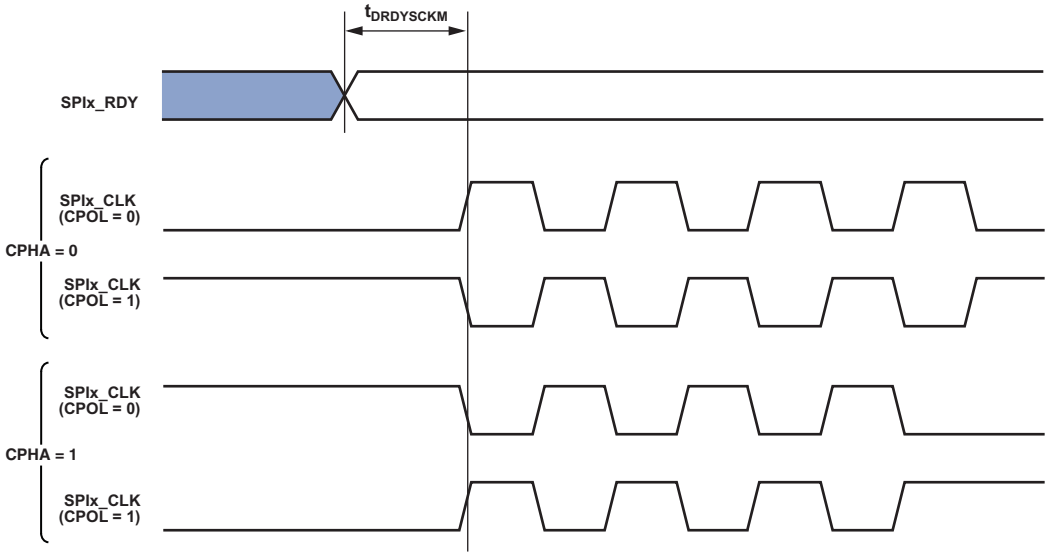

Figure 49. SPIx_CLK Switching Diagram After SPIx_RDY Assertion

Gigabit EMAC Timing (ETH0 Only)

Table 91 and Figure 62 describe the gigabit EMAC timing.

Table 91. Gigabit Ethernet MAC Controller (EMAC) Timing: RGMII [1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SETUPR}	Data to Clock Input Setup at Receiver	1		ns
t_{HOLDR}	Data to Clock Input Hold at Receiver	1		ns
$t_{GREFCLKF}$	RGMII Receive Clock Period	8		ns
$t_{GREFCLKW}$	RGMII Receive Clock Pulse Width	4		ns
Switching Characteristics				
t_{SKEWT}	Data to Clock Output Skew at Transmitter	–0.5	0.5	ns
t_{CYC}	Clock Cycle Duration	7.2	8.8	ns
t_{DUTY_G}	Duty Cycle for Gigabit Minimum	$t_{GREFCLKF} \times 45\%$	$t_{GREFCLKF} \times 55\%$	ns

[1] This specification is supported by ETH0 only (10/100/1000 EMAC controller).

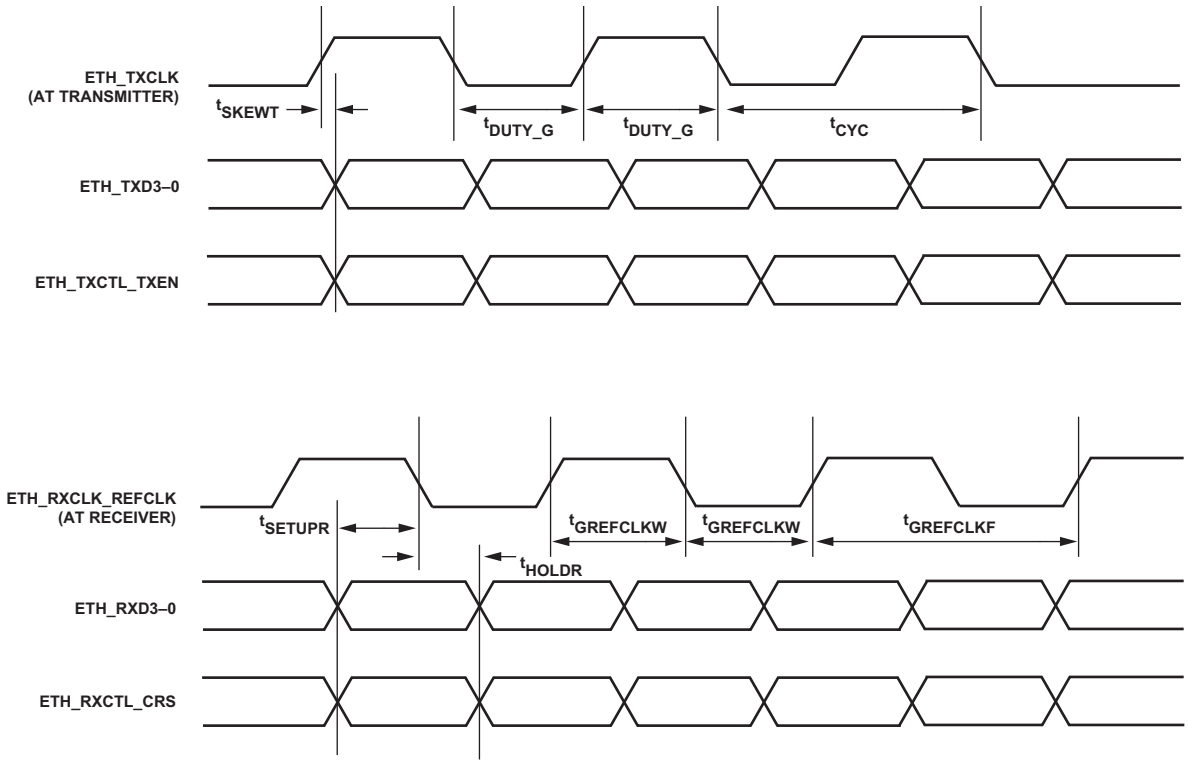

Figure 62. Gigabit EMAC Controller Timing—RGMII

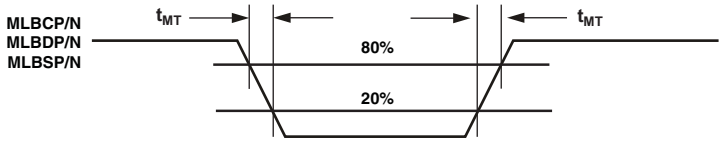

Figure 70. MLB 6-Pin Transition Time

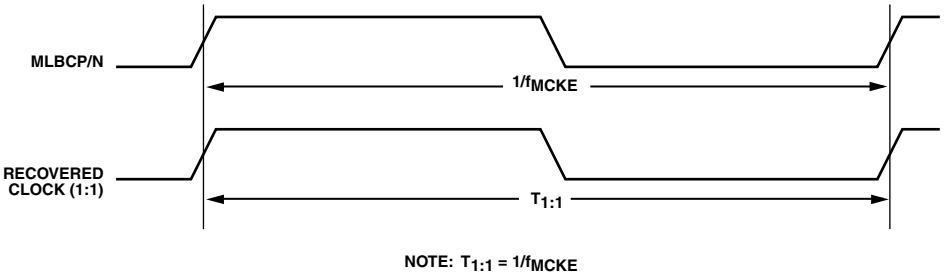

Figure 71. MLB 6-Pin Clock Definitions

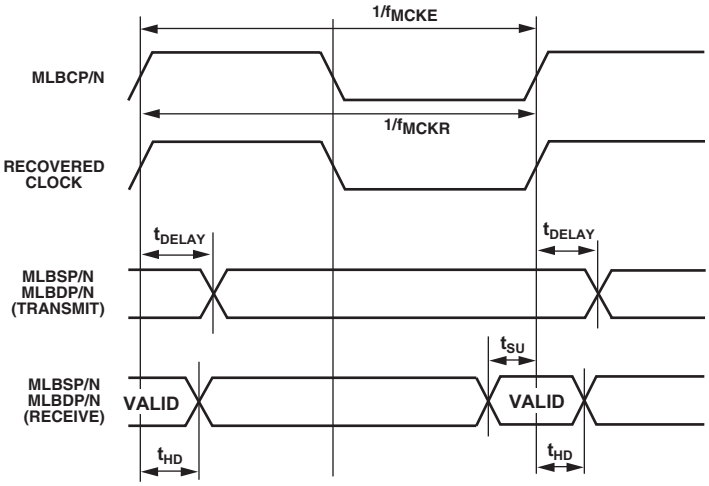

Figure 72. MLB 6-Pin Delay, Setup, and Hold Times

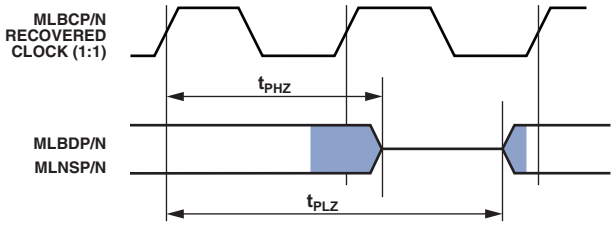

Figure 73. MLB 6-Pin Disable and Enable Turnaround Times

ORDERING GUIDE

Model[1]	Processor Instruction Rate (Max)	Temperature Range[2]	ARM Cores[3]	SHARC+ Cores	SHARC+ SRAM	PCIe Lanes[3]	Package Description	Package Option
ADSP-21583KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21587KBCZ-4B	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-21587BBCZ-4B	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC582KBCZ-4A	450 MHz	0°C to +70°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582BBCZ-4A	450 MHz	–40°C to +85°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582CBCZ-4A	450 MHz	–40°C to +95°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-3A	300 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-3A	300 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-3A	300 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-4A	450 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-4A	450 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-4A	450 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-3A	300 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-3A	300 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-3A	300 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-4A	450 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-4A	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-4A	450 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC587KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC587BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC589KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1
ADSP-SC589BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1

[1] Z =RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.

[3] N/A means not applicable.