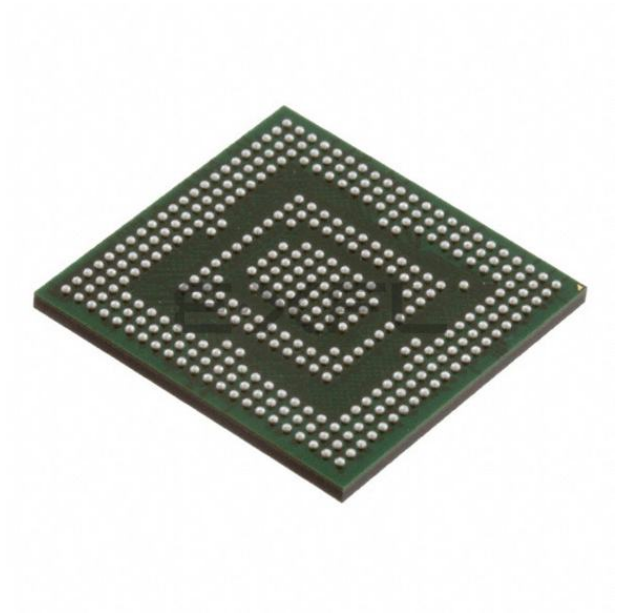

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsc584wcbcz3a10

Table 2. Comparison of ADSP-SC58x/ADSP-2158x Processor Features

Processor Feature		ADSP-SC582	ADSP-SC583	ADSP-SC584	ADSP-SC587	ADSP-SC589	ADSP-21583	ADSP-21584	ADSP-21587
ARM Cortex-A5 (MHz, Max)		450	450	450	450	450	N/A	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	32, 32	N/A	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	256	N/A	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	640	384	640	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1 Controller (16-bit)	1	1	1	2	2	1	1	2
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	1	N/A	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100/1000 /AVB EMAC + Timer IEEE 1588		1	1	1	1	1	N/A	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	1	N/A	N/A	N/A
RTC		N/A	N/A	N/A	1	1	N/A	N/A	1
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to G	Port A to E	Port A to E	Port A to G
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	102 + 40	80 + 28	80 + 28	102 + 40
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	529-BGA	349-BGA	349-BGA	529-BGA

Table 3. Comparison of ADSP-SC58x/ADSP-2158x Processor Features for Automotive

Processor Feature		ADSP-SC582W	ADSP-SC583W	ADSP-SC584W	ADSP-SC587W	ADSP-21583W	ADSP-21584W
ARM Cortex-A5 (MHz, Max)		450	450	450	450	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	384	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1 Controller (16-bit)	1	1	1	2	1	1
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	N/A	N/A
10/100/1000/AVB EMAC + Timer IEEE 1588		1	1	1	1	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	N/A	N/A
MLB 3-Pin/6-Pin		1	1	1	1	1	1
RTC		N/A	N/A	N/A	1	N/A	N/A
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to E	Port A to E
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	80 + 28	80 + 28
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	349-BGA	349-BGA

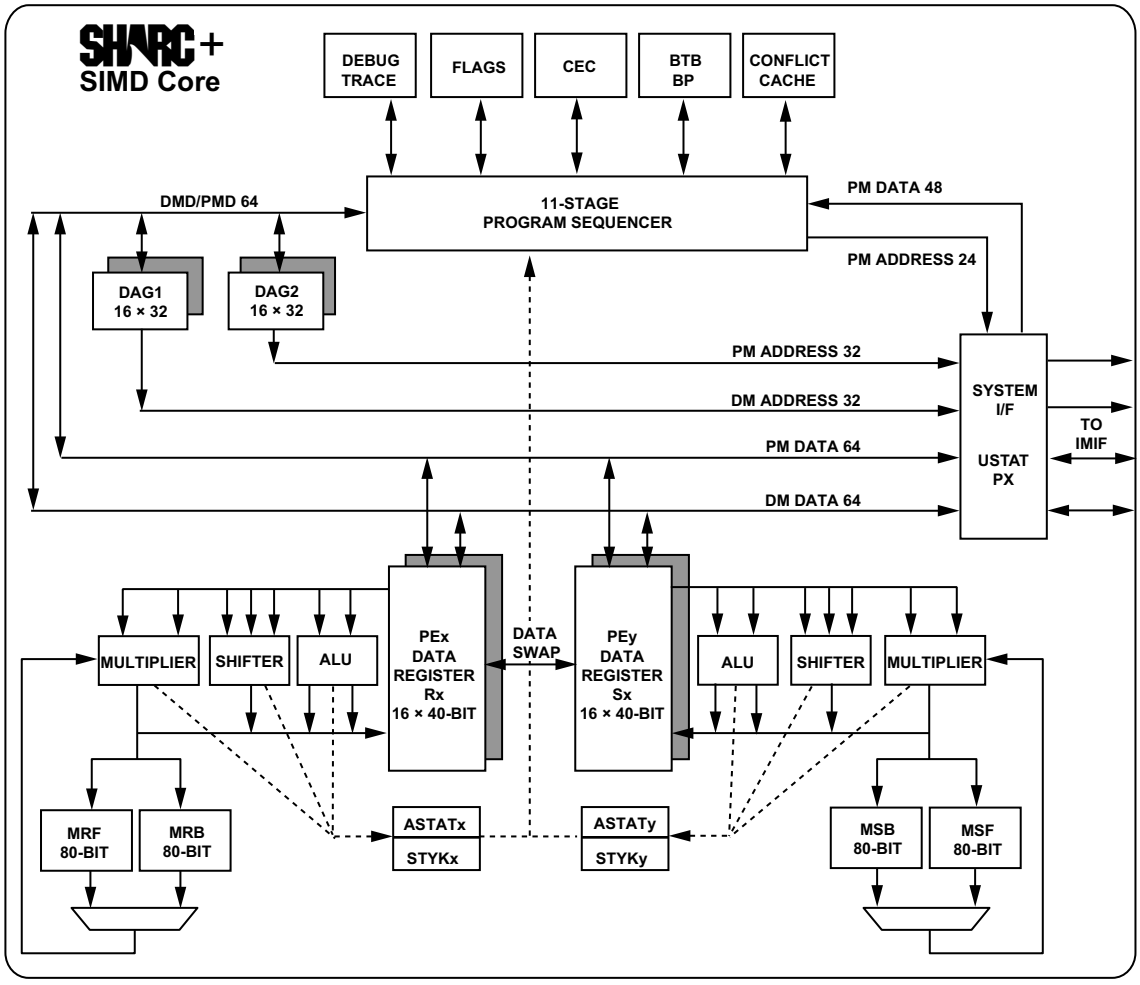

Figure 4. SHARC+ SIMD Core Block Diagram

L1 Memory

Figure 5 shows the ADSP-SC58x/ADSP-2158x memory map. Each SHARC+ core has a tightly coupled L1 SRAM of up to 5 Mb. Each SHARC+ core can access code and data in a single cycle from this memory space. The ARM Cortex-A5 core can also access this memory space with multicycle accesses.

In the SHARC+ core private address space, both cores have L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x 0000 0000 through 0x 0003 FFFF in Normal Word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1024 Kb can be configured for data memory (DM), program memory (PM), and instruction cache. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the DMA engine in a single cycle. The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 Kb DM, 128 Kb PM, and 128 Kb of instruction cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

- DMC (VDD_DMC)
- PCIe (VDD_PCIE, VDD_PCIE_TX and VDD_PCIE_RX)

All power supplies must meet the specifications provided in the Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 27.)

Table 10. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR3/DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
PCIe_TX	$V_{DD\_PCIE\_TX}$
PCIe_RX	$V_{DD\_PCIE\_RX}$
PCIe	V_{DD_PCIE}
All other I/O (includes SYS, JTAG, and port pins)	V_{DD_EXT}

The power dissipated by the processors is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

Debug Access Port (DAP)

Debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment (CrossCore® Embedded Studio), evaluation products, emulators, and a variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore Embedded Studio integrated development environment (IDE).

CrossCore Embedded Studio is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Various EZ-Extenders® are also available, which are daughter cards that deliver additional specialized functionality, including audio and video processing. For more information visit www.analog.com.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM2_DL	PWM2 Channel D Low Side	E	PE_10
PWM2_SYNC	PWM2 PWMTMR Grouped	E	PE_05
$\overline{\text{PWM2\_TRIP0}}$	PWM2 Shutdown Input 0	D	PD_14
GND	Ground	Not Muxed	GND
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
SINC0_CLK0	SINC0 Clock 0	B	PB_01
SINC0_D0	SINC0 Data 0	A	PA_14
SINC0_D1	SINC0 Data 1	A	PA_15
SINC0_D2	SINC0 Data 2	B	PB_00
SINC0_D3	SINC0 Data 3	B	PB_04
SMC0_A01	SMC0 Address 1	B	PB_05
SMC0_A02	SMC0 Address 2	B	PB_06
SMC0_A03	SMC0 Address 3	B	PB_03
SMC0_A04	SMC0 Address 4	B	PB_02
SMC0_A05	SMC0 Address 5	D	PD_13
SMC0_A06	SMC0 Address 6	D	PD_12
SMC0_A07	SMC0 Address 7	B	PB_01
SMC0_A08	SMC0 Address 8	B	PB_00
SMC0_A09	SMC0 Address 9	A	PA_15
SMC0_A10	SMC0 Address 10	A	PA_14
SMC0_A11	SMC0 Address 11	A	PA_09
SMC0_A12	SMC0 Address 12	A	PA_08
SMC0_A13	SMC0 Address 13	A	PA_13
SMC0_A14	SMC0 Address 14	A	PA_12
SMC0_A15	SMC0 Address 15	A	PA_11
SMC0_A16	SMC0 Address 16	A	PA_07
SMC0_A17	SMC0 Address 17	A	PA_06
SMC0_A18	SMC0 Address 18	A	PA_05
SMC0_A19	SMC0 Address 19	A	PA_04
SMC0_A20	SMC0 Address 20	A	PA_01
SMC0_A21	SMC0 Address 21	A	PA_00
SMC0_A22	SMC0 Address 22	A	PA_10
SMC0_A23	SMC0 Address 23	A	PA_03
SMC0_A24	SMC0 Address 24	A	PA_02
SMC0_A25	SMC0 Address 25	C	PC_12
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	E	PE_14
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	E	PE_15
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	C	PC_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	E	PE_13
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	C	PC_07
$\overline{\text{SMC0\_AMS3}}$	SMC0 Memory Select 3	C	PC_08
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	D	PD_01
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_04
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	C	PC_00
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_15
SMC0_D00	SMC0 Data 0	E	PE_12
SMC0_D01	SMC0 Data 1	E	PE_11

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART1_RTS	UART1 Request to Send	E	PE_02
UART1_RX	UART1 Receive	B	PB_03
UART1_TX	UART1 Transmit	B	PB_02
UART2_CTS	UART2 Clear to Send	E	PE_11
UART2_RTS	UART2 Request to Send	E	PE_10
UART2_RX	UART2 Receive	D	PD_13
UART2_TX	UART2 Transmit	D	PD_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Negative Data (–)	Not Muxed	USB0_DM
USB0_DP	USB0 Positive Data (+)	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
LP0_D7	LP0 Data 7	D	PD_09
LP1_ACK	LP1 Acknowledge	B	PB_15
LP1_CLK	LP1 Clock	C	PC_00
LP1_D0	LP1 Data 0	B	PB_07
LP1_D1	LP1 Data 1	B	PB_08
LP1_D2	LP1 Data 2	B	PB_09
LP1_D3	LP1 Data 3	B	PB_10
LP1_D4	LP1 Data 4	B	PB_11
LP1_D5	LP1 Data 5	B	PB_12
LP1_D6	LP1 Data 6	B	PB_13
LP1_D7	LP1 Data 7	B	PB_14
MLB0_CLKN	MLB0 Differential Clock (–)	Not Muxed	MLB0_CLKN
MLB0_CLKP	MLB0 Differential Clock (+)	Not Muxed	MLB0_CLKP
MLB0_DATN	MLB0 Differential Data (–)	Not Muxed	MLB0_DATN
MLB0_DATP	MLB0 Differential Data (+)	Not Muxed	MLB0_DATP
MLB0_SIGN	MLB0 Differential Signal (–)	Not Muxed	MLB0_SIGN
MLB0_SIGP	MLB0 Differential Signal (+)	Not Muxed	MLB0_SIGP
MLB0_CLK	MLB0 Single-Ended Clock	B	PB_04
MLB0_DAT	MLB0 Single-Ended Data	B	PB_06
MLB0_SIG	MLB0 Single-Ended Signal	B	PB_05
MLB0_CLKOUT	MLB0 Single-Ended Clock Out	D	PD_14
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	F	PF_12
MSI0_CLK	MSI0 Clock	F	PF_11
MSI0_CMD	MSI0 Command	F	PF_10
MSI0_D0	MSI0 Data 0	F	PF_02
MSI0_D1	MSI0 Data 1	F	PF_03
MSI0_D2	MSI0 Data 2	F	PF_04
MSI0_D3	MSI0 Data 3	F	PF_05
MSI0_D4	MSI0 Data 4	F	PF_06
MSI0_D5	MSI0 Data 5	F	PF_07
MSI0_D6	MSI0 Data 6	F	PF_08
MSI0_D7	MSI0 Data 7	F	PF_09
$\overline{\text{MSI0\_INT}}$	MSI0 eSDIO Interrupt Input	F	PF_13
PA_00-15	PORTA Position 00 through Position 15	A	PA_00-15
PB_00-15	PORTB Position 00 through Position 15	B	PB_00-15
PCIE0_CLKM	PCIE0 CLK -	Not Muxed	PCIE0_CLKM
PCIE0_CLKP	PCIE0 CLK +	Not Muxed	PCIE0_CLKP
PCIE0_REF	PCIE0 Reference	Not Muxed	PCIE0_REF
PCIE0_RXM	PCIE0 RX -	Not Muxed	PCIE0_RXM
PCIE0_RXP	PCIE0 RX +	Not Muxed	PCIE0_RXP
PCIE0_TXM	PCIE0 TX -	Not Muxed	PCIE0_TXM
PCIE0_TXP	PCIE0 TX +	Not Muxed	PCIE0_TXP
PC_00-15	PORTC Position 00 through Position 15	C	PC_00-15
PD_00-15	PORTD Position 00 through Position 15	D	PD_00-15
PE_00-15	PORTE Position 00 through Position 15	E	PE_00-15
PF_00-15	PORTF Position 00 through Position 15	F	PF_00-15
PG_00-5	PORTG Position 00 through Position 5	G	PG_00-5
PPI0_CLK	EPPI0 Clock	E	PE_03

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC0_DQ11	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes
DMC0_DQ12	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes
DMC0_DQ13	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes
DMC0_DQ14	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes
DMC0_DQ15	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes
DMC0_LDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes
$\overline{\text{DMC0\_LDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: No notes
DMC0_LDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: External weak pull-down required in LPDDR mode
DMC0_ODT	Output	B	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: No notes
$\overline{\text{DMC0\_RAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes
$\overline{\text{DMC0\_RESET}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Reset (DDR3 only) Notes: No notes
DMC0_RZQ	a	B	none	none	none	VDD_DMC	Desc: DMC0 External calibration resistor connection Notes: Applicable for DDR2 and DDR3 only. External pull-down of 34 ohms need to be added.
DMC0_UDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes
DMC0_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_00	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTC Position 0 | LP1 Clock | PWM0 Channel B Low Side | SMC0 Read Enable | SPI0 Slave Select Output 4 Notes: No notes
PC_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 1 | SPI2 Clock Notes: No notes
PC_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 2 | SPI2 Master In, Slave Out Notes: No notes
PC_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 3 | SPI2 Master Out, Slave In Notes: No notes
PC_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 4 | SPI2 Data 2 Notes: No notes
PC_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 5 | SPI2 Data 3 Notes: No notes
PC_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 6 | SPI2 Slave Select Output 1 | SPI2 Slave Select Input Notes: No notes
PC_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 7 | CAN0 Receive | SMC0 Memory Select 2 | SPI0 Slave Select Output 1 | TIMER0 Alternate Capture Input 3 Notes: No notes
PC_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 8 | CAN0 Transmit | SMC0 Memory Select 3 Notes: No notes
PC_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 9 | SPI0 Clock Notes: No notes
PC_10	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTC Position 10 | SPI0 Master In, Slave Out Notes: No notes
PC_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 11 | SPI0 Master Out, Slave In | TIMER0 Clock Notes: No notes
PC_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 12 | ACM0 External Trigger n | SMC0 Address 25 | SPI0 Ready | SPI0 Slave Select Output 3 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 13 | ACM0 ADC Control Signals | SPI1 Slave Select Output 1 | UART0 Transmit Notes: No notes
PC_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 14 | ACM0 ADC Control Signals | UART0 Receive | TIMER0 Alternate Capture Input 0 Notes: No notes
PC_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 15 | ACM0 ADC Control Signals | EPPI0 Frame Sync 3 (FIELD) | SMC0 Memory Select 0 | UART0 Request to Send Notes: No notes
PD_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 0 | ACM0 ADC Control Signals | EPPI0 Data 23 | SMC0 Data 7 | UART0 Clear to Send Notes: No notes
PD_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 1 | ACM0 ADC Control Signals | SMC0 Output Enable | SPI0 Slave Select Output 2 | SPI0 Slave Select Input Notes: No notes
PD_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 2 | LP0 Data 0 | PWM1 Shutdown Input 0 | TRACE0 Trace Data 0 Notes: No notes
PD_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 3 | LP0 Data 1 | PWM1 Channel A High Side | TRACE0 Trace Data 1 Notes: No notes
PD_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 4 | LP0 Data 2 | PWM1 Channel A Low Side | TRACE0 Trace Data 2 Notes: No notes
PD_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 5 | LP0 Data 3 | PWM1 Channel B High Side | TRACE0 Trace Data 3 Notes: No notes
PD_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 6 | LP0 Data 4 | PWM1 Channel B Low Side | TRACE0 Trace Data 4 Notes: No notes
PD_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 7 | LP0 Data 5 | PWM1 Channel C High Side | TRACE0 Trace Data 5 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 2 | EPPI0 Frame Sync 1 (HSYNC) | SPI0 Slave Select Output 6 | SHARC Core 2 Flag Pin | UART1 Request to Send Notes: No notes
PE_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 3 | EPPI0 Clock | SPI0 Slave Select Output 7 | SPI2 Slave Select Output 2 | SHARC Core 1 Flag Pin Notes: No notes
PE_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 4 | EPPI0 Data 8 | PWM2 Channel D High Side | SPI2 Slave Select Output 3 | SHARC Core 2 Flag Pin Notes: No notes
PE_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 5 | EPPI0 Data 7 | PWM2 PWMTMR Grouped | SPI2 Slave Select Output 4 | SHARC Core 1 Flag Pin Notes: No notes
PE_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 6 | EPPI0 Data 6 | SPI2 Slave Select Output 5 | SHARC Core 2 Flag Pin Notes: No notes
PE_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 7 | EPPI0 Data 5 | SPI1 Slave Select Output 2 | SHARC Core 1 Flag Pin Notes: No notes
PE_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 8 | EPPI0 Data 4 | SPI1 Ready | SPI1 Slave Select Output 5 | SHARC Core 2 Flag Pin Notes: No notes
PE_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 9 | EPPI0 Data 3 | PWM0 PWMTMR Grouped | SMC0 Data 3 | TIMER0 Timer 0 Notes: No notes
PE_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 10 | EPPI0 Data 2 | PWM2 Channel D Low Side | SMC0 Data 2 | UART2 Request to Send Notes: No notes
PE_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 11 | EPPI0 Data 1 | SMC0 Data 1 | SPI1 Slave Select Output 3 | UART2 Clear to Send | SPI1 Slave Select Input Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PF_08	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 8 | MSI0 Data 6 | PWM2 Channel B Low Side Notes: No notes
PF_09	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 9 | MSI0 Data 7 | PWM2 Channel B High Side Notes: No notes
PF_10	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 10 | MSI0 Command Notes: No notes
PF_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 11 | MSI0 Clock Notes: No notes
PF_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 12 | MSI0 Card Detect Notes: No notes
PF_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 13 | EMAC1 Carrier Sense/RMII Receive Data Valid | MSI0 eSDIO Interrupt Input | TRACE0 Trace Data | TRACE0 Trace Data 8 Notes: No notes
PF_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 14 | EMAC1 Management Channel Clock | TRACE0 Trace Data | TRACE0 Trace Data 9 Notes: No notes
PF_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 15 | EMAC1 Management Channel Serial Data | TRACE0 Trace Data | TRACE0 Trace Data 10 Notes: No notes
PG_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 0 | EMAC1 Reference Clock | TRACE0 Trace Clock Notes: No notes
PG_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 1 | EMAC1 Transmit Enable | TRACE0 Trace Data | TRACE0 Trace Data 11 Notes: No notes
PG_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 2 | EMAC1 Transmit Data 0 | TRACE0 Trace Data | TRACE0 Trace Data 12 Notes: No notes
PG_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 3 | EMAC1 Transmit Data 1 | TRACE0 Trace Data | TRACE0 Trace Data 13 Notes: No notes

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.1	1.15	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_RTC}	RTC Voltage		2.0	3.3	3.60	V
$V_{DD\_PCIE\_TX}$	PCIe Core Transmit Voltage		1.05	1.1	1.15	V
$V_{DD\_PCIE\_RX}$	PCIe Core Receive Voltage		1.05	1.1	1.15	V
V_{DD_PCIE}	PCIe Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = maximum	2.0			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.8	V
$V_{IL\_DDR2/3}$[5]	Low Level Input Voltage	V_{DD_DMC} = minimum			V_{REF} – 0.25	V
$V_{IH\_DDR2/3}$[5]	High Level Input Voltage	V_{DD_DMC} = maximum	V_{REF} + 0.25			V
V_{IL_LPDDR}[6]	Low Level Input Voltage	V_{DD_DMC} = minimum			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[6]	High Level Input Voltage	V_{DD_DMC} = maximum	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		100	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+110	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +95°C	–40		+125	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		110	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+125	°C
AUTOMOTIVE USE ONLY						
T_J	Junction Temperature 349-Lead CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ –40°C to +105°C	–40		+133[7]	°C

[1] Applies to DDR2/DDR3/LPDDR signals.
[2] If not used, V_{DD_USB} must be connected to 3.3V.
[3] V_{HADC_VREF} must always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional pins except the TWI, DMC, USB, PCIe, and MLB pins.
[5] This parameter applies to all DMC0/1 signals in DDR2/DDR3 mode. V_{REF} is the voltage applied to the V_{REF_DMC} pin, nominally $V_{DD\_DMC/2}$.
[6] This parameter applies to DMC0/1 signals in LPDDR mode.
[7] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Table 28. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_VSEL Selections	V_{DD_EXT} Nominal	V_{BUSTWI}			Unit
		Min	Nominal	Max	
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Parameter		Conditions	450 MHz Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 450 MHz ASF_{SHARC1} = 0.31 ASF_{SHARC2} = 0.31 ASF_{A5} = 0.29 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 1.1 V		495		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 450 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.73 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) FFT accelerator operating at $f_{SYSCLK/4}$ DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.1 V		1112		mA
I_{DD_INT}[11]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, PCIe, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups including JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals JTAG_TRST, USB0_VBUS, USB1_VBUS.
[9] Applies to signals PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-15, PG0-5, DAI0_PINx, DAI1_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USBx_DM, USBx_DP, and USBx_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC58x/2158x SHARC+ Processors" (EE-392) for further information.

DDR2 SDRAM Clock and Control Cycle Timing

Table 51 and Figure 17 show DDR2 SDRAM clock and control cycle timing, related to the DMC.

Table 51. DDR2 SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		400 MHz[2] Min	400 MHz[2] Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.5		ns
$t_{CH\ (abs)}$[3]	Minimum Clock Pulse Width	0.44	0.56	t_{CK}
$t_{CL\ (abs)}$[3]	Maximum Clock Pulse Width	0.44	0.56	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	175		ps
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	250		ps

[1] Specifications apply to both DMC0 and DMC1.
[2] In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-2E definition.

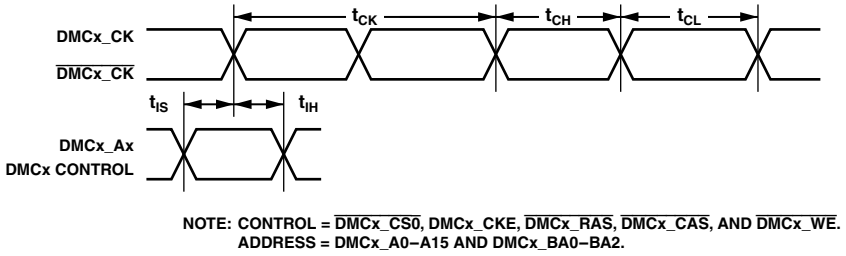

Figure 17. DDR2 SDRAM Clock and Control Cycle Timing

DDR3 SDRAM Write Cycle Timing

Table 59 and Figure 25 show mobile DDR3 SDRAM output ac timing, related to the DMC.

Table 59. DDR3 SDRAM Write Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Switching Characteristics				
t_{DQSS}	DMCx_DQS Latching Rising Transitions to Associated Clock Edges[3]	–0.25	0.25	t_{CK}
t_{DS}	Last Data Valid to DMCx_DQS Delay (Slew > 1 V/ns)	0.125		ns
t_{DH}	DMCx_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.150		ns
t_{DSS}	DMCx_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMCx_DQS Falling Edge Hold Time From DMCx_CK	0.2		t_{CK}
t_{DQSH}	DMCx_DQS Input High Pulse Width	0.45	0.55	t_{CK}
t_{DQSL}	DMCx_DQS Input Low Pulse Width	0.45	0.55	t_{CK}
t_{WPRE}	Write Preamble	0.9		t_{CK}
t_{WPST}	Write Postamble	0.3		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.840		ns
t_{DIPW}	DMCx_DQ and DMCx_DM Output Pulse Width	0.550		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] Write command to first DMCx_DQS delay = WL × t_{CK} + t_{DQSS}.

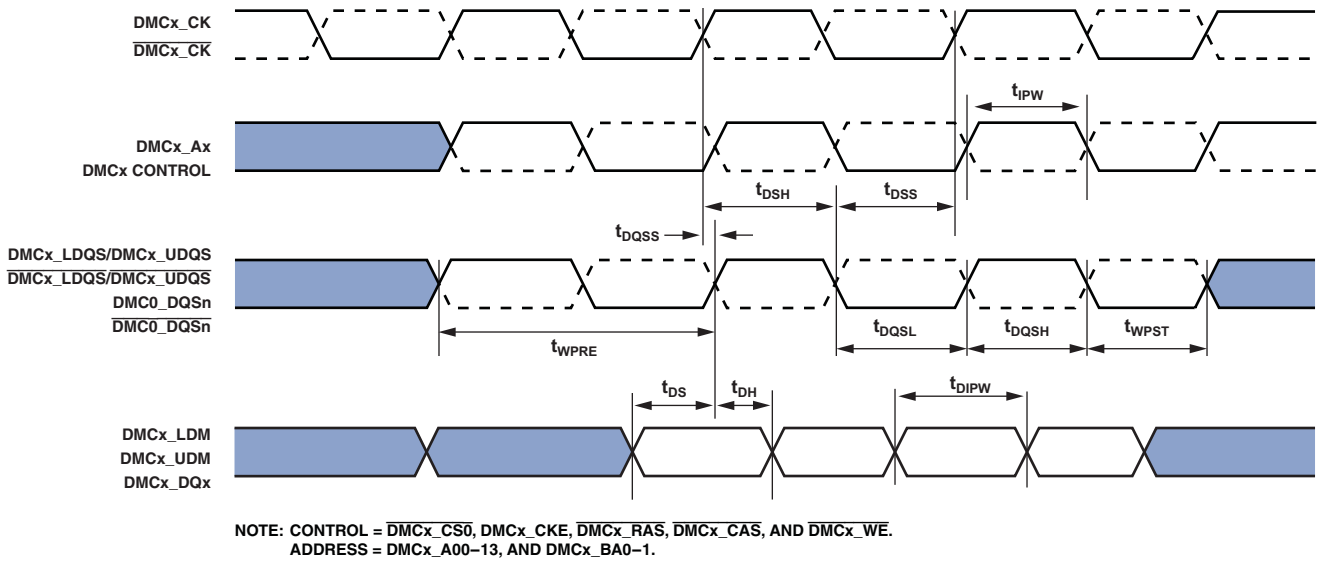

Figure 25. DDR3 SDRAM Controller Output AC Timing

SPI Port—Open Drain Mode (ODM) Timing

In Figure 46 and Figure 47 and Table 75 and Table 76, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3 depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 74. SPI Port ODM Master Mode Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance from Data Out Valid	–1		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid from High Impedance	–1	+6	ns

[1] All specifications apply to all three SPIs.

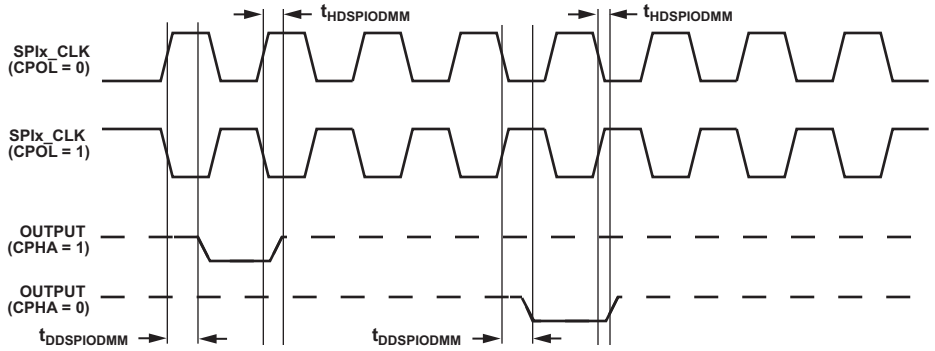

Figure 46. ODM Master Mode

Table 75. SPI Port—ODM Slave Mode[1]

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

[1] All specifications apply to all three SPIs.

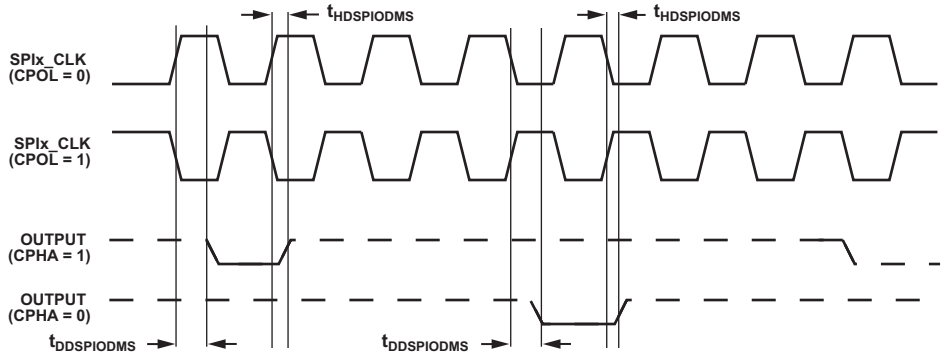

Figure 47. ODM Slave Mode

Sinus Cardinalis (SINC) Filter Timing

The programmed SINC filter clock ($f_{SINCLKPROG}$) frequency in MHz is set by the following equation where MDIV is a field in the CLK control register that can be set from 4 to 63:

$$f_{SINCLKPROG} = \frac{f_{SCLK}}{MDIV}$$

$$t_{SINCLKPROG} = \frac{1}{f_{SINCLKPROG}}$$

Table 92. SINC Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSINC}	SINC0_Dx Setup Before SINC0_CLKx Rise	13.5		ns
t_{HSINC}	SINC0_Dx Hold After SINC0_CLKx Rise	0		ns
Switching Characteristics				
t_{SINCLK}	SINC0_CLKx Period[1]	$t_{SINCLKPROG} - 2.5$		ns
$t_{SINCLKW}$	SINC0_CLKx Width[1]	$0.5 \times t_{SINCLKPROG} - 2.5$		ns

[1] See Table 29 for details on the minimum period that may be programmed for $t_{SINCLKPROG}$.

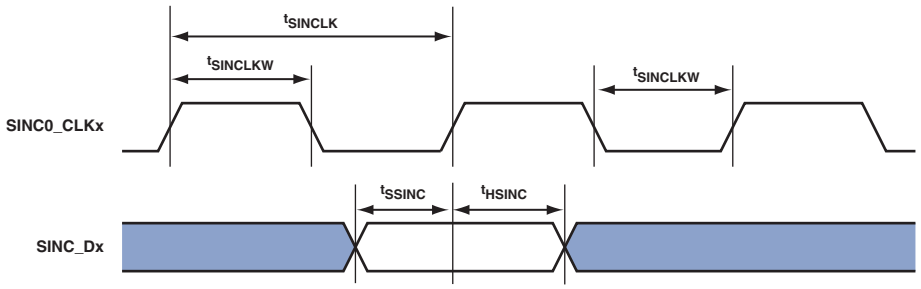

Figure 63. SINC Timing

CONFIGURATION OF THE 349-BALL CSP_BGA

Figure 98 shows an overview of signal placement on the 349-ball CSP_BGA.

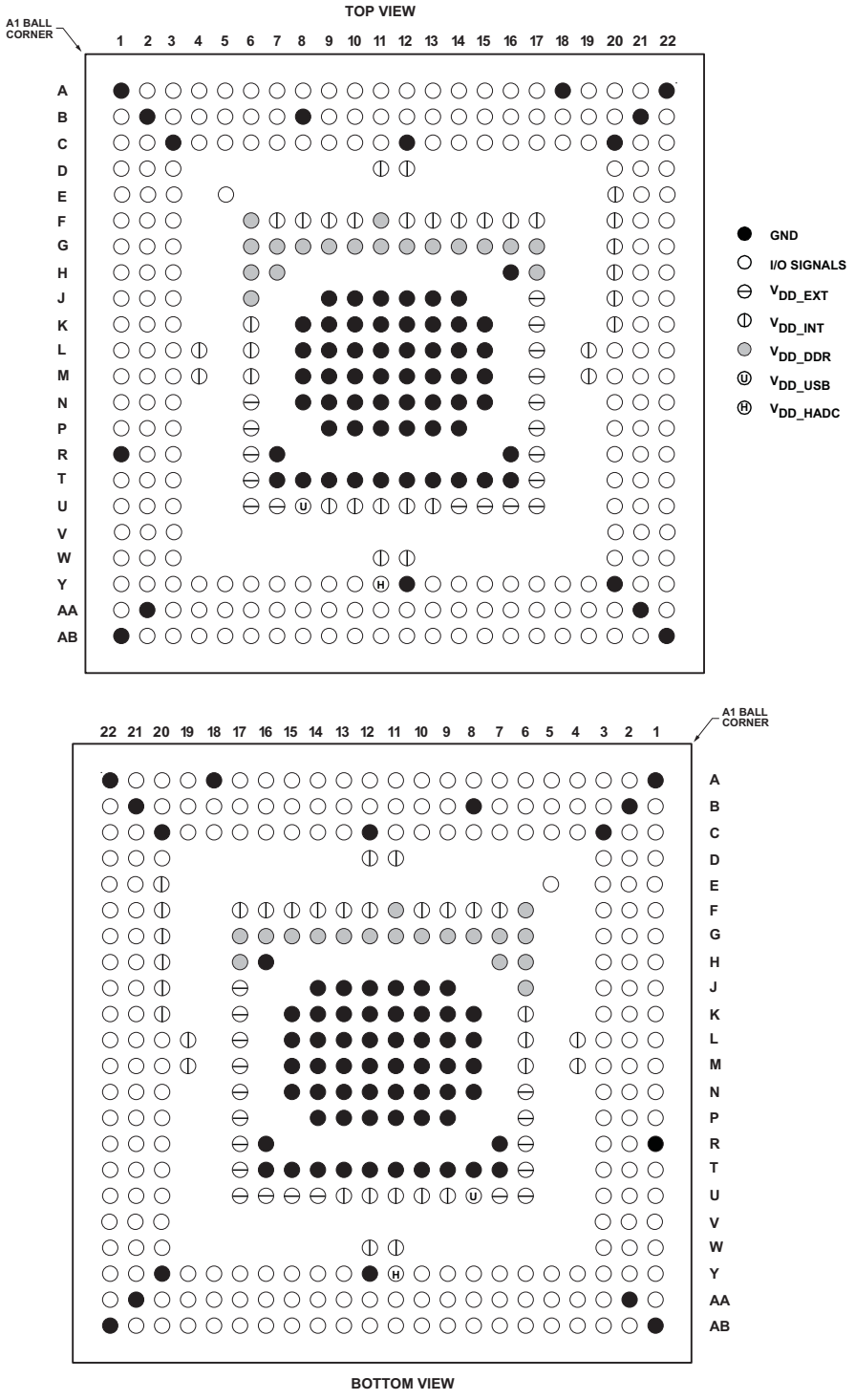

Figure 98. 349-Ball CSP_BGA Configuration

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
T08	GND	V10	VDD_EXT	Y12	HADC0_VIN0	AB14	HADC0_VIN3
T09	GND	V11	VDD_EXT	Y13	HADC0_VIN7	AB15	RTC0_XTAL
T10	GND	V12	HADC0_VIN4	Y14	GND	AB16	MLB0_SIGN
T11	GND	V13	VDD_EXT	Y15	PB_05	AB17	MLB0_DATN
T12	GND	V14	VDD_EXT	Y16	PA_14	AB18	MLB0_CLKN
T13	GND	V15	VDD_EXT	Y17	PA_13	AB19	PA_15
T14	GND	V16	VDD_EXT	Y18	PA_12	AB20	PA_11
T15	GND	V17	VDD_EXT	Y19	PA_10	AB21	PA_06
T16	GND	V18	VDD_EXT	Y20	PA_00	AB22	PA_04
T17	GND	V19	VDD_INT	Y21	DAI1_PIN14	AB23	PA_02
T18	VDD_EXT	V20	DAI1_PIN16	Y22	DAI1_PIN17	AC01	GND
T19	VDD_INT	V21	DAI1_PIN06	Y23	DAI1_PIN15	AC02	PCIE0_RXP
T20	DAI1_PIN03	V22	DAI1_PIN12	AA01	PB_08	AC03	PCIE0_RXM
T21	PG_03	V23	DAI1_PIN09	AA02	PB_07	AC04	PCIE0_CLKM
T22	PG_02	W01	PB_12	AA03	DAI0_PIN16	AC05	PCIE0_CLKP
T23	DAI1_PIN01	W02	PB_09	AA04	DAI0_PIN07	AC06	PCIE0_TXP
U01	SYS_XTAL0	W03	DAI0_PIN18	AA05	DAI0_PIN06	AC07	PCIE0_TXM
U02	$\overline{\text{SYS\_RESOUT}}$	W04	DAI0_PIN11	AA06	DAI0_PIN01	AC08	USB1_DM
U03	PC_00	W05	VDD_INT	AA07	PCIE0_REF	AC09	USB1_DP
U04	DAI0_PIN20	W06	VDD_INT	AA08	USB1_VBUS	AC10	USB0_DP
U05	VDD_INT	W07	VDD_PCIE	AA09	USB0_VBUS	AC11	USB0_DM
U06	VDD_EXT	W08	VDD_INT	AA10	TWI1_SCL	AC12	HADC0_VREFP
U07	GND	W09	VDD_INT	AA11	TWI1_SDA	AC13	VDD_HADC
U08	GND	W10	VDD_INT	AA12	HADC0_VIN1	AC14	GND
U09	GND	W11	VDD_INT	AA13	HADC0_VIN5	AC15	RTC0_CLKIN
U10	GND	W12	HADC0_VIN6	AA14	PB_06	AC16	MLB0_SIGP
U11	GND	W13	VDD_INT	AA15	PB_02	AC17	MLB0_DATP
U12	GND	W14	VDD_RTC	AA16	PB_04	AC18	MLB0_CLKP
U13	GND	W15	VDD_INT	AA17	PB_03	AC19	PB_01
U14	GND	W16	VDD_INT	AA18	PB_00	AC20	PA_07
U15	GND	W17	VDD_INT	AA19	PA_09	AC21	PA_08
U16	GND	W18	VDD_INT	AA20	PA_05	AC22	PA_03
U17	GND	W19	VDD_INT	AA21	PA_01	AC23	GND
U18	VDD_EXT	W20	DAI1_PIN20	AA22	DAI1_PIN19		
U19	DAI1_PIN08	W21	DAI1_PIN11	AA23	DAI1_PIN18		
U20	DAI1_PIN07	W22	DAI1_PIN10	AB01	DAI0_PIN15		
U21	DAI1_PIN04	W23	DAI1_PIN13	AB02	DAI0_PIN14		
U22	DAI1_PIN05	Y01	PB_11	AB03	DAI0_PIN09		
U23	DAI1_PIN02	Y02	PB_10	AB04	DAI0_PIN13		
V01	SYS_CLKIN0	Y03	DAI0_PIN17	AB05	DAI0_PIN04		
V02	PB_13	Y04	DAI0_PIN08	AB06	DAI0_PIN02		
V03	DAI0_PIN19	Y05	DAI0_PIN05	AB07	DAI0_PIN03		
V04	DAI0_PIN12	Y06	DAI0_PIN10	AB08	USB_XTAL		
V05	VDD_INT	Y07	USB0_ID	AB09	USB_CLKIN		
V06	VDD_EXT	Y08	VDD_USB	AB10	TWI2_SCL		
V07	VDD_PCIE_RX	Y09	USB0_VBC	AB11	TWI0_SDA		
V08	VDD_PCIE_TX	Y10	TWI0_SCL	AB12	HADC0_VREFN		
V09	VDD_EXT	Y11	TWI2_SDA	AB13	HADC0_VIN2		

D13317-0-10/16(0)