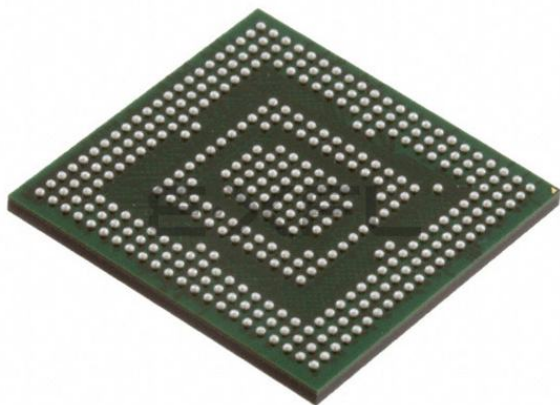




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I ² C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsc584wcbcz4a10

ADSP-SC582/SC583/SC584/SC587/SC589/ADSP-21583/21584/21587

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REVISION HISTORY

10/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADSP-SC58x/ADSP-2158x processors are members of the SHARC® family of products. The ADSP-SC58x processor is based on the SHARC+ dual core and the ARM® Cortex®-A5 core. The ADSP-SC58x/ADSP-2158x SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI). New additions to the SHARC+ core include cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a set of industry leading system peripherals and memory (see [Table 1](#), [Table 2](#), and [Table 3](#)), the ARM Cortex-A5 and SHARC processor is the platform of choice for applications that require programmability similar to RISC (reduced instruction set computing), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, pro audio, and industrial-based applications that require high floating-point performance.

[Table 2](#) provides comparison information for features that vary across the standard processors. (N/A in the table means not applicable.)

[Table 3](#) provides comparison information for features that vary across the automotive processors. (N/A in the table means not applicable.)

Table 1. Common Product Features

Product Features	ADSP-SC58x/ADSP-2158x
DAI (includes SRU)	2
Full SPORTs	4 per DAI
S/PDIF receive/transmit	1 per DAI
ASRCs	4 pair per DAI
PCGs	2 per DAI
I ² C (TWI)	3
Quad-data bit SPI	1
Dual-data bit SPI	2
CAN2.0	2
UARTs	3
Link ports	2
Enhanced PPI	1
GP timer ¹	8
GP counter	1
Enhanced PWMs ²	3
Watchdog timers	2
ADC control module	Yes
Static memory controller	Yes
Hardware accelerators	
High performance FFT/IFFT	Yes
FIR/IIR	Yes
Harmonic analysis engine	Yes
SINC filter	Yes
Security cryptographic engine	Yes
Multichannel 12-bit ADC	8-channel

¹ Eight timers are available in the 529-BGA package only. The 349-BGA package does not include Timer 6 and 7.

² Three 3ePWMs are available in the 529-BGA package only. The 349-BGA package does not include PWM 2.

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Table 2. Comparison of ADSP-SC58x/ADSP-2158x Processor Features

Processor Feature		ADSP-SC582	ADSP-SC583	ADSP-SC584	ADSP-SC587	ADSP-SC589	ADSP-21583	ADSP-21584	ADSP-21587
ARM Cortex-A5 (MHz, Max)		450	450	450	450	450	N/A	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	32, 32	N/A	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	256	N/A	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	640	384	640	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1	1	1	1	2	2	1	1	2
	Controller (16-bit)								
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	1	N/A	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100/1000 /AVB EMAC + Timer IEEE 1588		1	1	1	1	1	N/A	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	1	N/A	N/A	N/A
RTC		N/A	N/A	N/A	1	1	N/A	N/A	1
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to G	Port A to E	Port A to E	Port A to G
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	102 + 40	80 + 28	80 + 28	102 + 40
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	529-BGA	349-BGA	349-BGA	529-BGA

Table 3. Comparison of ADSP-SC58x/ADSP-2158x Processor Features for Automotive

Processor Feature		ADSP-SC582W	ADSP-SC583W	ADSP-SC584W	ADSP-SC587W	ADSP-21583W	ADSP-21584W
ARM Cortex-A5 (MHz, Max)		450	450	450	450	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	384	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1	1	1	1	2	1	1
	Controller (16-bit)						
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	N/A	N/A
10/100/1000/AVB EMAC + Timer IEEE 1588		1	1	1	1	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	N/A	N/A
MLB 3-Pin/6-Pin		1	1	1	1	1	1
RTC		N/A	N/A	N/A	1	N/A	N/A
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to E	Port A to E
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	80 + 28	80 + 28
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	349-BGA	349-BGA

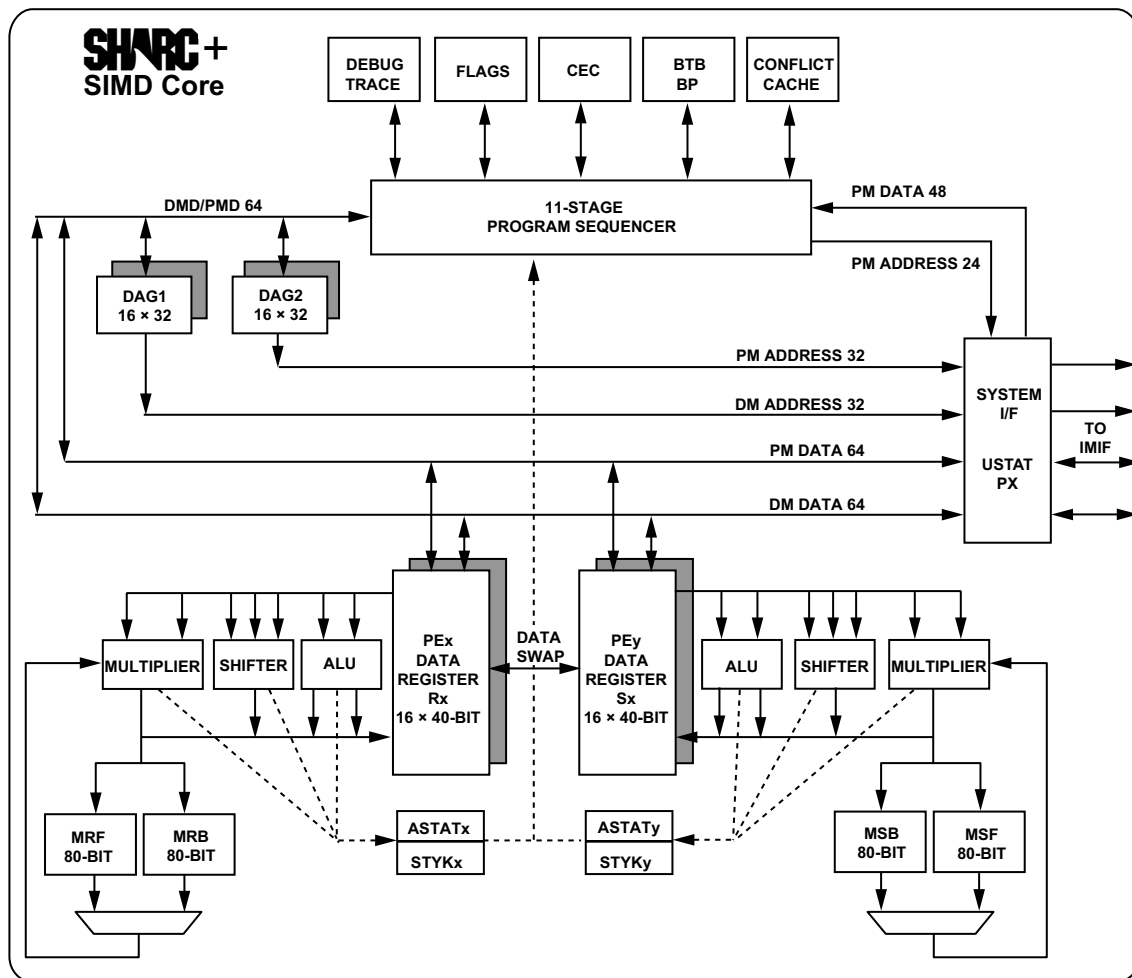


Figure 4. SHARC+ SIMD Core Block Diagram

L1 Memory

Figure 5 shows the ADSP-SC58x/ADSP-2158x memory map. Each SHARC+ core has a tightly coupled L1 SRAM of up to 5 Mb. Each SHARC+ core can access code and data in a single cycle from this memory space. The ARM Cortex-A5 core can also access this memory space with multicycle accesses.

In the SHARC+ core private address space, both cores have L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x 0000 0000 through 0x 0003 FFFF in Normal Word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1024 Kb can be configured for data memory (DM), program memory (PM), and instruction cache. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the DMA engine in a single cycle. The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit

instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 Kb DM, 128 Kb PM, and 128 Kb of instruction cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

ADSP-SC582/SC583/SC584/SC587/SC589/ADSP-21583/21584/21587

529-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown [Table 19](#) for the 529-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.

- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the [ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference](#) for complete information on the use of the DAIs and SRUs.

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	C	PC_13
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	D	PD_00
ACM0_A4	ACM0 ADC Control Signals	D	PD_01
ACM0_T0	ACM0 External Trigger n	C	PC_12
C1_FLG0	SHARC Core 1 Flag Pin	E	PE_01
C1_FLG1	SHARC Core 1 Flag Pin	E	PE_03
C1_FLG2	SHARC Core 1 Flag Pin	E	PE_05
C1_FLG3	SHARC Core 1 Flag Pin	E	PE_07
C2_FLG0	SHARC Core 2 Flag Pin	E	PE_02
C2_FLG1	SHARC Core 2 Flag Pin	E	PE_04
C2_FLG2	SHARC Core 2 Flag Pin	E	PE_06
C2_FLG3	SHARC Core 2 Flag Pin	E	PE_08
CAN0_RX	CAN0 Receive	C	PC_07
CAN0_TX	CAN0 Transmit	C	PC_08
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_09
CNT0_DG	CNT0 Count Down and Gate	B	PB_14
CNT0_UD	CNT0 Count Up and Direction	B	PB_12
CNT0_ZM	CNT0 Count Zero Marker	B	PB_11
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN13	DAI0 Pin 13	Not Muxed	DAI0_PIN13
DAI0_PIN14	DAI0 Pin 14	Not Muxed	DAI0_PIN14

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Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DAI0_PIN15	DAI0 Pin 15	Not Muxed	DAI0_PIN15
DAI0_PIN16	DAI0 Pin 16	Not Muxed	DAI0_PIN16
DAI0_PIN17	DAI0 Pin 17	Not Muxed	DAI0_PIN17
DAI0_PIN18	DAI0 Pin 18	Not Muxed	DAI0_PIN18
DAI0_PIN19	DAI0 Pin 19	Not Muxed	DAI0_PIN19
DAI0_PIN20	DAI0 Pin 20	Not Muxed	DAI0_PIN20
DAI1_PIN01	DAI1 Pin 1	Not Muxed	DAI1_PIN01
DAI1_PIN02	DAI1 Pin 2	Not Muxed	DAI1_PIN02
DAI1_PIN03	DAI1 Pin 3	Not Muxed	DAI1_PIN03
DAI1_PIN04	DAI1 Pin 4	Not Muxed	DAI1_PIN04
DAI1_PIN05	DAI1 Pin 5	Not Muxed	DAI1_PIN05
DAI1_PIN06	DAI1 Pin 6	Not Muxed	DAI1_PIN06
DAI1_PIN07	DAI1 Pin 7	Not Muxed	DAI1_PIN07
DAI1_PIN08	DAI1 Pin 8	Not Muxed	DAI1_PIN08
DAI1_PIN09	DAI1 Pin 9	Not Muxed	DAI1_PIN09
DAI1_PIN10	DAI1 Pin 10	Not Muxed	DAI1_PIN10
DAI1_PIN11	DAI1 Pin 11	Not Muxed	DAI1_PIN11
DAI1_PIN12	DAI1 Pin 12	Not Muxed	DAI1_PIN12
DAI1_PIN13	DAI1 Pin 13	Not Muxed	DAI1_PIN13
DAI1_PIN14	DAI1 Pin 14	Not Muxed	DAI1_PIN14
DAI1_PIN15	DAI1 Pin 15	Not Muxed	DAI1_PIN15
DAI1_PIN16	DAI1 Pin 16	Not Muxed	DAI1_PIN16
DAI1_PIN17	DAI1 Pin 17	Not Muxed	DAI1_PIN17
DAI1_PIN18	DAI1 Pin 18	Not Muxed	DAI1_PIN18
DAI1_PIN19	DAI1 Pin 19	Not Muxed	DAI1_PIN19
DAI1_PIN20	DAI1 Pin 20	Not Muxed	DAI1_PIN20
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_A14	DMC0 Address 14	Not Muxed	DMC0_A14
DMC0_A15	DMC0 Address 15	Not Muxed	DMC0_A15
DMC0_BA0	DMC0 Bank Address 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address 2	Not Muxed	DMC0_BA2
DMC0_CAS	DMC0 Column Address Strobe	Not Muxed	DMC0_CAS
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE

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Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
$\overline{\text{DMC0_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0_CK}}$
$\overline{\text{DMC0_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0_LDQS}}$
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0_RAS}}$	DMC0 Row Address Strobe	Not Muxed	$\overline{\text{DMC0_RAS}}$
$\overline{\text{DMC0_RESET}}$	DMC0 Reset (DDR3 only)	Not Muxed	$\overline{\text{DMC0_RESET}}$
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0_UDQS}}$	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0_UDQS}}$
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
$\overline{\text{DMC0_WE}}$	DMC0 Write Enable	Not Muxed	$\overline{\text{DMC0_WE}}$
DMC1_A00	DMC1 Address 0	Not Muxed	DMC1_A00
DMC1_A01	DMC1 Address 1	Not Muxed	DMC1_A01
DMC1_A02	DMC1 Address 2	Not Muxed	DMC1_A02
DMC1_A03	DMC1 Address 3	Not Muxed	DMC1_A03
DMC1_A04	DMC1 Address 4	Not Muxed	DMC1_A04
DMC1_A05	DMC1 Address 5	Not Muxed	DMC1_A05
DMC1_A06	DMC1 Address 6	Not Muxed	DMC1_A06
DMC1_A07	DMC1 Address 7	Not Muxed	DMC1_A07
DMC1_A08	DMC1 Address 8	Not Muxed	DMC1_A08
DMC1_A09	DMC1 Address 9	Not Muxed	DMC1_A09
DMC1_A10	DMC1 Address 10	Not Muxed	DMC1_A10
DMC1_A11	DMC1 Address 11	Not Muxed	DMC1_A11
DMC1_A12	DMC1 Address 12	Not Muxed	DMC1_A12
DMC1_A13	DMC1 Address 13	Not Muxed	DMC1_A13
DMC1_A14	DMC1 Address 14	Not Muxed	DMC1_A14
DMC1_A15	DMC1 Address 15	Not Muxed	DMC1_A15
DMC1_BA0	DMC1 Bank Address 0	Not Muxed	DMC1_BA0
DMC1_BA1	DMC1 Bank Address 1	Not Muxed	DMC1_BA1

ADSP-SC582/SC583/SC584/SC587/SC589/ADSP-21583/21584/21587

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_AMS2	SMC0 Memory Select 2	C	PC_07
SMC0_AMS3	SMC0 Memory Select 3	C	PC_08
SMC0_AOE	SMC0 Output Enable	D	PD_01
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_04
SMC0_ARE	SMC0 Read Enable	C	PC_00
SMC0_AWE	SMC0 Write Enable	B	PB_15
SMC0_D00	SMC0 Data 0	E	PE_12
SMC0_D01	SMC0 Data 1	E	PE_11
SMC0_D02	SMC0 Data 2	E	PE_10
SMC0_D03	SMC0 Data 3	E	PE_09
SMC0_D04	SMC0 Data 4	E	PE_00
SMC0_D05	SMC0 Data 5	D	PD_15
SMC0_D06	SMC0 Data 6	D	PD_14
SMC0_D07	SMC0 Data 7	D	PD_00
SMC0_D08	SMC0 Data 8	B	PB_14
SMC0_D09	SMC0 Data 9	B	PB_13
SMC0_D10	SMC0 Data 10	B	PB_12
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_10
SMC0_D13	SMC0 Data 13	B	PB_09
SMC0_D14	SMC0 Data 14	B	PB_08
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_10
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_11
SPI0_RDY	SPI0 Ready	C	PC_12
SPI0_SEL1	SPI0 Slave Select Output 1	C	PC_07
SPI0_SEL2	SPI0 Slave Select Output 2	D	PD_01
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_12
SPI0_SEL4	SPI0 Slave Select Output 4	C	PC_00
SPI0_SEL5	SPI0 Slave Select Output 5	E	PE_01
SPI0_SEL6	SPI0 Slave Select Output 6	E	PE_02
SPI0_SEL7	SPI0 Slave Select Output 7	E	PE_03
SPI0_SS	SPI0 Slave Select Input	D	PD_01
SPI1_CLK	SPI1 Clock	E	PE_13
SPI1_MISO	SPI1 Master In, Slave Out	E	PE_14
SPI1_MOSI	SPI1 Master Out, Slave In	E	PE_15
SPI1_RDY	SPI1 Ready	E	PE_08
SPI1_SEL1	SPI1 Slave Select Output 1	C	PC_13
SPI1_SEL2	SPI1 Slave Select Output 2	E	PE_07
SPI1_SEL3	SPI1 Slave Select Output 3	E	PE_11
SPI1_SEL4	SPI1 Slave Select Output 4	E	PE_12
SPI1_SEL5	SPI1 Slave Select Output 5	E	PE_08
SPI1_SEL6	SPI1 Slave Select Output 6	F	PF_00
SPI1_SEL7	SPI1 Slave Select Output 7	F	PF_01
SPI1_SS	SPI1 Slave Select Input	E	PE_11
SPI2_CLK	SPI2 Clock	C	PC_01
SPI2_D2	SPI2 Data 2	C	PC_04

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Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC0_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: No notes
DMC0_VREF	a		none	none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: No notes
DMC0_WE	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes
DMC1_A00	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 0 Notes: No notes
DMC1_A01	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 1 Notes: No notes
DMC1_A02	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 2 Notes: No notes
DMC1_A03	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 3 Notes: No notes
DMC1_A04	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 4 Notes: No notes
DMC1_A05	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 5 Notes: No notes
DMC1_A06	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 6 Notes: No notes
DMC1_A07	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 7 Notes: No notes
DMC1_A08	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 8 Notes: No notes
DMC1_A09	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 9 Notes: No notes
DMC1_A10	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 10 Notes: No notes
DMC1_A11	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 11 Notes: No notes
DMC1_A12	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 12 Notes: No notes
DMC1_A13	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 13 Notes: No notes
DMC1_A14	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 14 Notes: No notes
DMC1_A15	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 15 Notes: No notes
DMC1_BA0	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 0 Notes: No notes
DMC1_BA1	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 1 Notes: No notes

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Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PG_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 4 EMAC1 Receive Data 0 TRACE0 Trace Data TRACE0 Trace Data 14 Notes: No notes
PG_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 5 EMAC1 Receive Data 1 TRACE0 Trace Data TRACE0 Trace Data 15 Notes: No notes
RTC0_CLKIN	a	NA	none	none	none	VDD_RTC	Desc: RTC0 Crystal input / external oscillator connection Notes: Connect to GND if not used
RTC0_XTAL	a	NA	none	none	none	VDD_RTC	Desc: RTC0 Crystal output Notes: No notes
SYS_BMODE0	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_BMODE1	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_BMODE2	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_CLKIN0	a	NA	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: No notes
SYS_CLKIN1	a	NA	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: Connect to GND if not used
SYS_CLKOUT	a	A	none	none	none		Desc: Processor Clock Output Notes: No notes
SYS_FAULT	InOut	A	none	none	none		Desc: Active-High Fault Output Notes: External pull-down required to keep signal in de-asserted state
$\overline{\text{SYS_FAULT}}$	InOut	A	none	none	none		Desc: Active-Low Fault Output Notes: External pull-up required to keep signal in de-asserted state
$\overline{\text{SYS_HWRST}}$	Input	NA	none	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No notes
$\overline{\text{SYS_RESOUT}}$	Output	A	none	none	L	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	a	NA	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
SYS_XTAL1	a	NA	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.

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DDR2 SDRAM Read Cycle Timing

Table 52 and Figure 18 show DDR2 SDRAM read cycle timing, related to the DMC.

Table 52. DDR2 SDRAM Read Cycle Timing, $V_{DD_DMC_x}$ Nominal 1.8 V¹

Parameter		400 MHz ²		Unit
		Min	Max	
Timing Requirements				
t _{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQxx Signals		0.2	ns
t _{QH}	DMCx_DQxx, DMCx_DQS Output Hold Time From DMCx_DQS	0.9		ns
t _{RPRE}	Read Preamble	0.9		t _{CK}
t _{RPST}	Read Postamble	0.4		t _{CK}

¹Specifications apply to both DMC0 and DMC1.

²In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See “Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors” (EE-387).

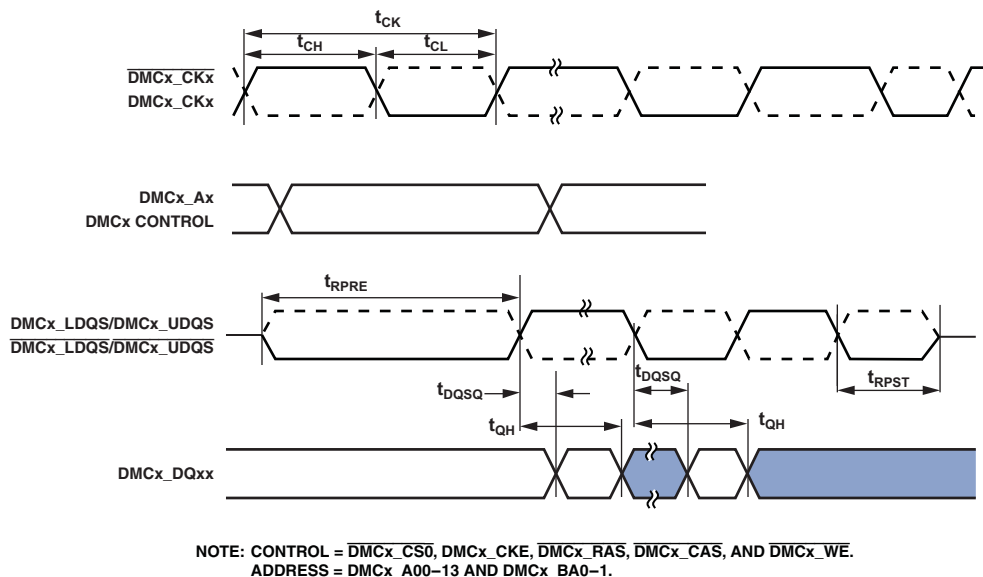


Figure 18. DDR2 SDRAM Controller Input AC Timing

ADSP-SC582/SC583/SC584/SC587/SC589/ADSP-21583/21584/21587

DDR2 SDRAM Write Cycle Timing

Table 53 and Figure 19 show DDR2 SDRAM write cycle timing, related to the DMC.

Table 53. DDR2 SDRAM Write Cycle Timing, $V_{DD_DMC_x}$ Nominal 1.8 V¹

Parameter		400 MHz ²		Unit
		Min	Max	
Switching Characteristics				
t _{DQSS}	DMC _x _DQS Latching Rising Transitions to Associated Clock Edges ³	−0.15	+0.15	t _{CK}
t _{DS}	Last Data Valid to DMC _x _DQS Delay	0.1		ns
t _{DH}	DMC _x _DQS to First Data Invalid Delay	0.15		ns
t _{DSS}	DMC _x _DQS Falling Edge to Clock Setup Time	0.2		t _{CK}
t _{DSH}	DMC _x _DQS Falling Edge Hold Time From DMC _x _CK	0.2		t _{CK}
t _{DQSH}	DMC _x _DQS Input High Pulse Width	0.35		t _{CK}
t _{DQSL}	DMC _x _DQS Input Low Pulse Width	0.35		t _{CK}
t _{WPRE}	Write Preamble	0.35		t _{CK}
t _{WPST}	Write Postamble	0.4		t _{CK}
t _{IPW}	Address and Control Output Pulse Width	0.6		t _{CK}
t _{DIPW}	DMC _x _DQ and DMC _x _DM Output Pulse Width	0.35		t _{CK}

¹Specifications apply to both DMC0 and DMC1.

²To ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See “Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors” (EE-387).

³Write command to first DMC_x_DQS delay = $WL \times t_{CK} + t_{DQSS}$.

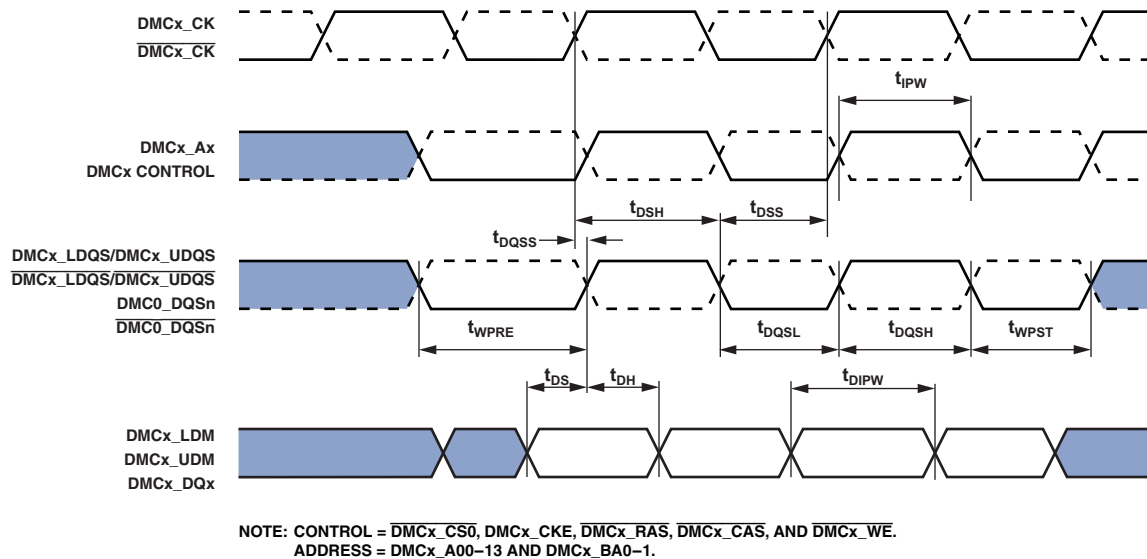


Figure 19. DDR2 SDRAM Controller Output AC Timing

ADSP-SC582/SC583/SC584/SC587/SC589/ADSP-21583/21584/21587

DDR3 SDRAM Write Cycle Timing

Table 59 and Figure 25 show mobile DDR3 SDRAM output ac timing, related to the DMC.

Table 59. DDR3 SDRAM Write Cycle Timing VDD_DMCx Nominal 1.5 V¹

Parameter		450 MHz ²		Unit
		Min	Max	
Switching Characteristics				
t _{DQSS}	DMC _x _DQS Latching Rising Transitions to Associated Clock Edges ³	−0.25	0.25	t _{CK}
t _{DS}	Last Data Valid to DMC _x _DQS Delay (Slew > 1 V/ns)	0.125		ns
t _{DH}	DMC _x _DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.150		ns
t _{DSS}	DMC _x _DQS Falling Edge to Clock Setup Time	0.2		t _{CK}
t _{DSH}	DMC _x _DQS Falling Edge Hold Time From DMC _x _CK	0.2		t _{CK}
t _{DQSH}	DMC _x _DQS Input High Pulse Width	0.45	0.55	t _{CK}
t _{DQSL}	DMC _x _DQS Input Low Pulse Width	0.45	0.55	t _{CK}
t _{WPRE}	Write Preamble	0.9		t _{CK}
t _{WPST}	Write Postamble	0.3		t _{CK}
t _{IPW}	Address and Control Output Pulse Width	0.840		ns
t _{DIPW}	DMC _x _DQ and DMC _x _DM Output Pulse Width	0.550		ns

¹Specifications apply to both DMC0 and DMC1.

²To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See “Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors” (EE-387).

³Write command to first DMCx_QDS delay = WL × t_{CK} + t_{DQSS}.

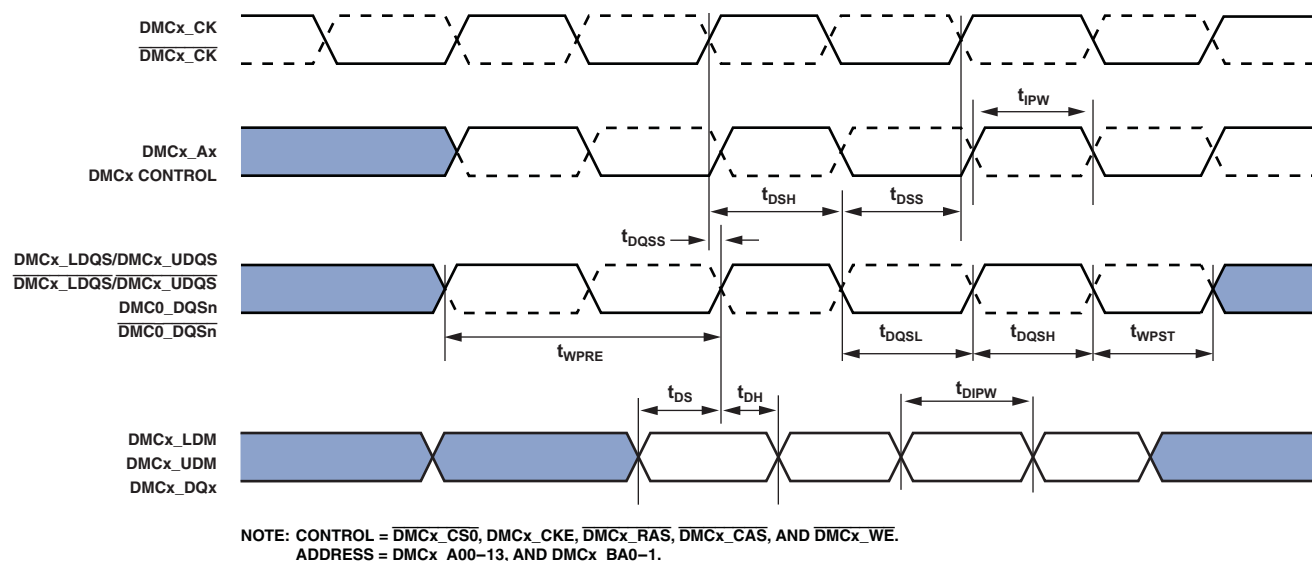


Figure 25. DDR3 SDRAM Controller Output AC Timing

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Link Ports (LP)

In LP receive mode, the link port clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by:

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In link port transmit mode, the programmed link port clock ($f_{LCLKTPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{CLKO8}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{CLKO8}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH} \min - t_{DLCH} - t_{SLDCL}$). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL} \min - t_{HLDCH} - t_{HLDCL}$).

Table 62. Link Ports—Receive¹

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$f_{LCLKREXT}$ LPx_CLK Frequency		150	MHz
t_{SLDCL} Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL} Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKW} LPx_CLK Period ²	$t_{LCLKREXT} - 0.42$		ns
$t_{LCLKRWL}$ LPx_CLK Width Low ²	$0.5 \times t_{LCLKREXT}$		ns
$t_{LCLKRWH}$ LPx_CLK Width High ²	$0.5 \times t_{LCLKREXT}$		ns
<i>Switching Characteristic</i>			
t_{DLALC} LPx_ACK Low Delay After LPx_CLK Low ³	$1.5 \times t_{CLKO8} + 4$	$2.5 \times t_{CLKO8} + 12$	ns

¹Specifications apply to LP0 and LP1.

²This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency see the $f_{LCLKTEXT}$ specification in Table 29.

³LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

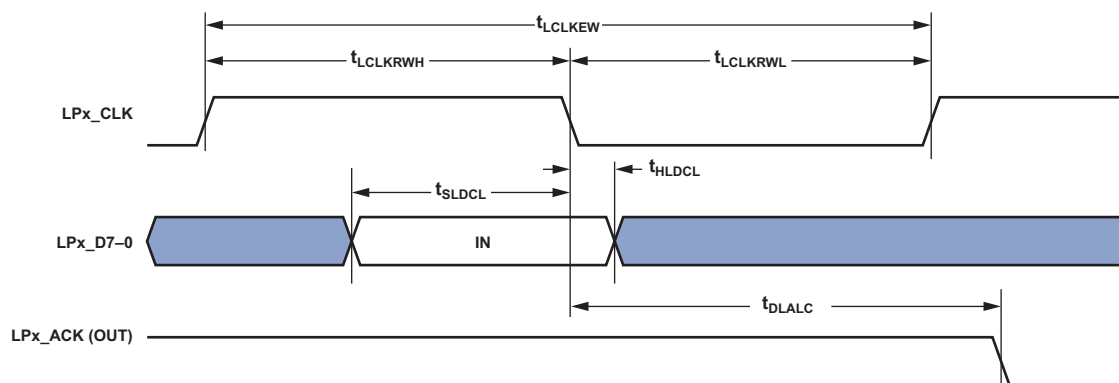


Figure 35. Link Ports—Receive

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SPI Port—Open Drain Mode (ODM) Timing

In Figure 46 and Figure 47 and Table 75 and Table 76, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3 depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 74. SPI Port ODM Master Mode Timing¹

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t_{HDSPIDMM} SPIx_CLK Edge to High Impedance from Data Out Valid	-1		ns
t_{DDSPIDMM} SPIx_CLK Edge to Data Out Valid from High Impedance	-1	+6	ns

¹ All specifications apply to all three SPIs.

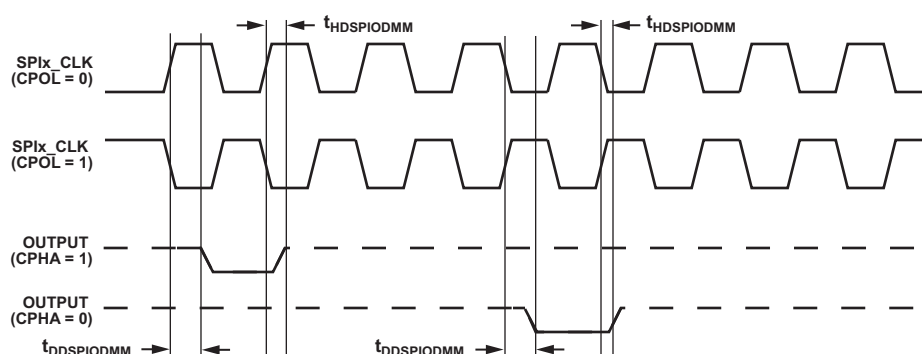


Figure 46. ODM Master Mode

Table 75. SPI Port—ODM Slave Mode¹

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{HDSPIDMS} SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
t_{DDSPIDMS} SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

¹ All specifications apply to all three SPIs.

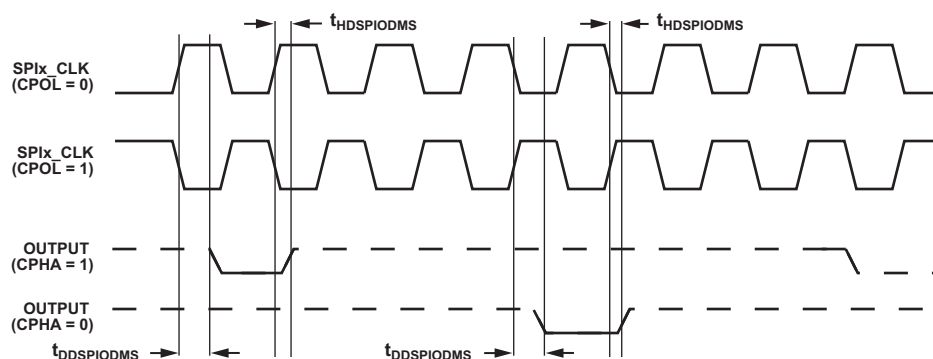


Figure 47. ODM Slave Mode

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General-Purpose I/O Port Timing

Table 78 and Figure 51 describe I/O timing, related to the general-purpose I/O port (PORT).

Table 78. General-Purpose Port Timing

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{WFI} General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

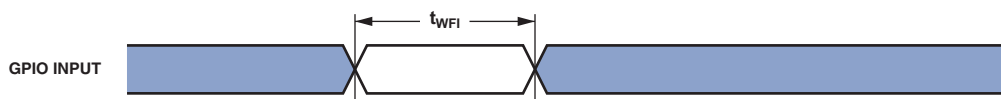


Figure 51. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 79, Table 80, and Figure 52 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of $f_{SCLK}/4$ MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 79. Timer Cycle Timing (Internal Mode)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{WL} Timer Pulse Width Input Low (Measured In SCLK Cycles) ¹	$2 \times t_{SCLK}$		ns
t_{WH} Timer Pulse Width Input High (Measured In SCLK Cycles) ¹	$2 \times t_{SCLK}$		ns
<i>Switching Characteristic</i>			
t_{HTO} Timer Pulse Width Output (Measured In SCLK Cycles) ²	$t_{SCLK} \times WIDTH - 1.5$	$t_{SCLK} \times WIDTH + 1.5$	ns

¹ The minimum pulse width applies for timer signals in width capture and external clock modes.

² WIDTH refers to the value in the $TMRx_WIDTH$ register (it can vary from 1 to $2^{32} - 1$).

Table 80. Timer Cycle Timing (External Mode)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{WL} Timer Pulse Width Input Low (Measured In EXT_CLK Cycles) ¹	$2 \times t_{EXT_CLK}$		ns
t_{WH} Timer Pulse Width Input High (Measured In EXT_CLK Cycles) ¹	$2 \times t_{EXT_CLK}$		ns
t_{EXT_CLK} Timer External Clock Period ²	$t_{TMRCLKEXT}$		ns
<i>Switching Characteristic</i>			
t_{HTO} Timer Pulse Width Output (Measured In EXT_CLK Cycles) ³	$t_{EXT_CLK} \times WIDTH - 1.5$	$t_{EXT_CLK} \times WIDTH + 1.5$	ns

¹ The minimum pulse width applies for timer signals in width capture and external clock modes.

² This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK . For the external TMR_CLK maximum frequency see the $f_{TMRCLKEXT}$ specification in Table 29.

³ WIDTH refers to the value in the $TMRx_WIDTH$ register (it can vary from 1 to $2^{32} - 1$).

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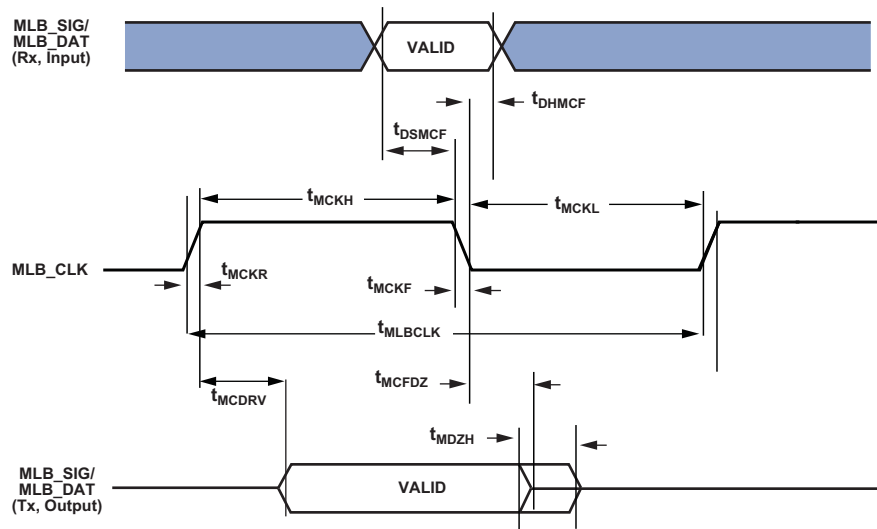


Figure 69. MLB Timing (3-Pin Interface)

The ac timing specifications of the 6-pin MLB interface is detailed in [Table 100](#). Refer to the *Media Local Bus Specification version 4.2* for more details.

Table 100. 6-Pin MLB Interface Specifications

Parameter	Conditions	Min	Typ	Max	Unit
t_{MT} Differential Transition Time at the Input Pin (See Figure 70)	20% to 80% V_{IN+}/V_{IN-} 80% to 20% V_{IN+}/V_{IN-}			1	ns
f_{MCKE} MLBCP/N External Clock Operating Frequency (See Figure 71) ¹	$2048 \times FS$ at 44.0 kHz $2048 \times FS$ at 50.0 kHz	90.112		102.4	MHz
f_{MCKR} Recovered Clock Operating Frequency (Internal, not Observable at Pins, Only for Timing References) (See Figure 71)	$2048 \times FS$ at 44.0 kHz $2048 \times FS$ at 50.0 kHz	90.112		102.4	MHz
t_{DELAY} Transmitter MLBSP/N (MLBDP/N) Output Valid From Transition of MLBCP/N (Low to High) (See Figure 72)	$f_{MCKR} = 2048 \times FS$	0.6		5	ns
t_{PHZ} Disable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 73)	$f_{MCKR} = 2048 \times FS$	0.6		7	ns
t_{PLZ} Enable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 73)	$f_{MCKR} = 2048 \times FS$	0.6		11.2	ns
t_{SU} MLBSP/N (MLBDP/N) Valid to Transition of MLBCP/N (Low to High) (See Figure 72)	$f_{MCKR} = 2048 \times FS$	1			ns
t_{HD} MLBSP/N (MLBDP/N) Hold From Transition of MLBCP/N (Low to High) (See Figure 72) ²		0.6			ns

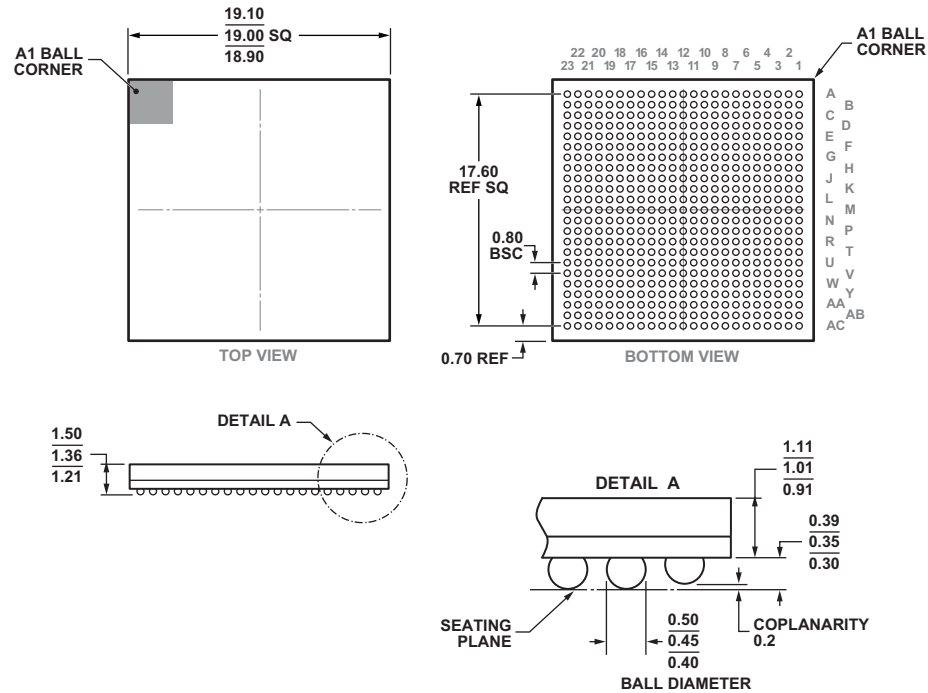
¹ f_{MCKE} (maximum) and f_{MCKR} (maximum) include maximum cycle to cycle system jitter (t_{JITTER}) of 600 ps for a bit error rate of 10E-9.

² Receivers must latch MLBSP/N (MLBDP/N) data within t_{HD} (min) of the rising edge of MLBCP/N.

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Dimensions for the 19 mm × 19 mm 529-ball CSP_BGA package in [Figure 101](#) are shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MO-275-RRAB-2.

Figure 101. 529-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-529-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

[Table 106](#) is an aid for PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 106. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-349-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter
BC-529-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter