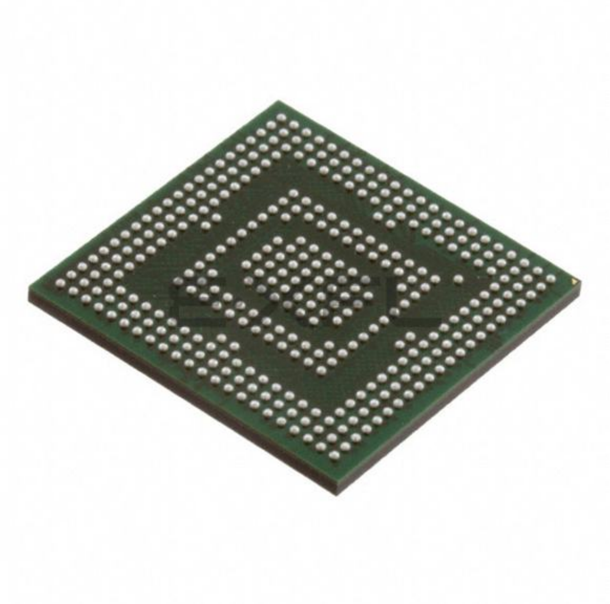

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21583kbcz-4a

GENERAL DESCRIPTION

The ADSP-SC58x/ADSP-2158x processors are members of the SHARC® family of products. The ADSP-SC58x processor is based on the SHARC+ dual core and the ARM® Cortex®-A5 core. The ADSP-SC58x/ADSP-2158x SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI). New additions to the SHARC+ core include cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a set of industry leading system peripherals and memory (see Table 1, Table 2, and Table 3), the ARM Cortex-A5 and SHARC processor is the platform of choice for applications that require programmability similar to RISC (reduced instruction set computing), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, pro audio, and industrial-based applications that require high floating-point performance.

Table 2 provides comparison information for features that vary across the standard processors. (N/A in the table means not applicable.)

Table 3 provides comparison information for features that vary across the automotive processors. (N/A in the table means not applicable.)

Table 1. Common Product Features

Product Features	ADSP-SC58x/ADSP-2158x
DAI (includes SRU)	2
Full SPORTs	4 per DAI
S/PDIF receive/transmit	1per DAI
ASRCs	4 pair per DAI
PCGs	2 per DAI
I^2C (TWI)	3
Quad-data bit SPI	1
Dual-data bit SPI	2
CAN2.0	2
UARTs	3
Link ports	2
Enhanced PPI	1
GP timer[1]	8
GP counter	1
Enhanced PWMs[2]	3
Watchdog timers	2
ADC control module	Yes
Static memory controller	Yes
Hardware accelerators	
High performance FFT/IFFT	Yes
FIR/IIR	Yes
Harmonic analysis engine	Yes
SINC filter	Yes
Security cryptographic engine	Yes
Multichannel 12-bit ADC	8-channel

[1] Eight timers are available in the 529-BGA package only. The 349-BGA package does not include Timer 6 and 7.

[2] Three 3ePWMs are available in the 529-BGA package only. The 349-BGA package does not include PWM 2.

Table 7. Memory Map of Mapped I/Os

	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	SHARC+ Core Instruction Fetch	
			VISA Space	ISA Space
SMC Bank 0 (64 MB)	0x40000000–0x43FFFFFF	0x01000000–0x01FFFFFF	0x00F00000–0x00F3FFFF	0x00700000–0x0073FFFF
SMC Bank 1 (64 MB)	0x44000000–0x47FFFFFF	Not applicable	Not applicable	Not applicable
SMC Bank 2 (64 MB)	0x48000000–0x4BFFFFFF	Not applicable	Not applicable	Not applicable
SMC Bank 3 (64 MB)	0x4C000000–0x4FFFFFFF	Not applicable	Not applicable	Not applicable
PCIe Data (256 MB)	0x50000000–0x5FFFFFFF	0x02000000–0x03FFFFFF	0x00F40000–0x00F7FFFF	0x00740000–0x0077FFFF
SPI2 Memory (512 MB)	0x60000000–0x7FFFFFFF	0x04000000–0x07FFFFFF	0x00F80000–0x00FFFFFF	0x00780000–0x007FFFFF

Table 8. DMC Memory Map

	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	SHARC+ Core Instruction Fetch	
			VISA Space	ISA Space
DMC0 (1 GB)	0x80000000–0xBFFFFFFF	0x10000000–0x17FFFFFF	0x00800000–0x00AFFFFF	0x00400000–0x004FFFFF
DMC1 (1 GB)	0xC0000000–0xFFFFFFFF	0x18000000–0x1FFFFFFF	0x00C00000–0x00EFFFFF	0x00600000–0x006FFFFF

System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch-fabric style for on-chip system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: one channel is the source channel and the second is the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based.

Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address
- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, RMII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Controller Area Network (CAN)

There are two controller area network (CAN) modules. A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to the capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on the first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- Interrupts, including transmit and receive complete, error, and global

An additional crystal is not required to supply the CAN clock because it is derived from a system clock through a programmable divider.

Timers

The processors include several timers that are described in the following sections.

General-Purpose (GP) Timers (TIMER)

There is one general-purpose (GP) timer unit, providing eight general-purpose programmable timers. Each timer has an external pin that can be configured either as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM_TMR[n] pins, an external TM_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and/or stopped by any TRU master without core intervention.

Watchdog Timer (WDT)

Two on-chip software watchdog timers (WDT) can be used by the ARM Cortex-A5 and/or SHARC+ cores. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

General-Purpose Counters (CNT)

A 32-bit counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

PCI Express (PCIe)

A PCI express interface (PCIe) is available on some product variants (see Table 2 and Table 3). This single, bidirectional lane can be configured to be either a root complex (RC) or end point (EP) system. The PCIe interface has the following features:

- Compliance with the *PCI Express Base Specification 3.0*
- Support for transfers at either 2.5 Gbps (Gen 1) or 5.0 Gbps (Gen 2) in each direction
- Support for 8b/10b encode and decode
- Lane reversal and lane polarity inversion
- Flow control of data in both the transmit and receive directions
- Support for removal of corrupted packets for error detection and recovery
- Maximum transaction payload of 256 bytes

Housekeeping Analog-to-Digital Converter (HADC)

The housekeeping analog-to-digital converter (HADC) provides a general-purpose, multichannel successive approximation ADC. It supports the following set of features:

- 12-bit ADC core (10-bit accuracy) with built in sample and hold.
- Eight single-ended input channels that can be extended to 15 channels by adding an external channel multiplexer.
- Throughput rates up to 1 MSPS.

- DMC (VDD_DMC)
- PCIe (VDD_PCIE, VDD_PCIE_TX and VDD_PCIE_RX)

All power supplies must meet the specifications provided in the Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 27.)

Table 10. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR3/DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
PCIe_TX	$V_{DD\_PCIE\_TX}$
PCIe_RX	$V_{DD\_PCIE\_RX}$
PCIe	V_{DD_PCIE}
All other I/O (includes SYS, JTAG, and port pins)	V_{DD_EXT}

The power dissipated by the processors is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

Debug Access Port (DAP)

Debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment (CrossCore® Embedded Studio), evaluation products, emulators, and a variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore Embedded Studio integrated development environment (IDE).

CrossCore Embedded Studio is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Various EZ-Extenders® are also available, which are daughter cards that deliver additional specialized functionality, including audio and video processing. For more information visit www.analog.com.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit.

Table 11. ADSP-SC58x/ADSP-2158x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SMC_ABE[n]	Output	**Byte Enable n.** Indicates whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1 = 0 and SMC_ABE0 = 1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1 = 1 and SMC_ABE0 = 0.
SMC_AMS[n]	Output	**Memory Select n.** Typically connects to the chip select of a memory device.
SMC_AOE	Output	**Output Enable.** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready.** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable.** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable.** Asserts for the duration of a write access period.
SMC_A[nn]	Output	**Address n.** Address bus.
SMC_D[nn]	InOut	**Data n.** Bidirectional data bus.
SPI_CLK	InOut	**Clock.** Input in slave mode, output in master mode.
SPI_D2	InOut	**Data 2.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_D3	InOut	**Data 3.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	InOut	**Ready.** Optional flow signal. Output in slave mode, input in master mode.
SPI_SEL[n]	Output	**Slave Select Output n.** Used in master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input.** Slave mode—acts as the slave select input. Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	InOut	**Channel A Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	InOut	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AD1	InOut	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AFS	InOut	**Channel A Frame Sync.** The frame sync pulse initiates shifting of the serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SPT_BCLK	InOut	**Channel B Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	InOut	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BD1	InOut	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BFS	InOut	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SYS_BMODE[n]	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN0	Input	**Clock/Crystal Input.**
SYS_CLKIN1	Input	**Clock/Crystal Input.**
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference for more details.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DAI1_PIN01	DAI1 Pin 1	Not Muxed	DAI1_PIN01
DAI1_PIN02	DAI1 Pin 2	Not Muxed	DAI1_PIN02
DAI1_PIN03	DAI1 Pin 3	Not Muxed	DAI1_PIN03
DAI1_PIN04	DAI1 Pin 4	Not Muxed	DAI1_PIN04
DAI1_PIN05	DAI1 Pin 5	Not Muxed	DAI1_PIN05
DAI1_PIN06	DAI1 Pin 6	Not Muxed	DAI1_PIN06
DAI1_PIN07	DAI1 Pin 7	Not Muxed	DAI1_PIN07
DAI1_PIN08	DAI1 Pin 8	Not Muxed	DAI1_PIN08
DAI1_PIN09	DAI1 Pin 9	Not Muxed	DAI1_PIN09
DAI1_PIN10	DAI1 Pin 10	Not Muxed	DAI1_PIN10
DAI1_PIN11	DAI1 Pin 11	Not Muxed	DAI1_PIN11
DAI1_PIN12	DAI1 Pin 12	Not Muxed	DAI1_PIN12
DAI1_PIN19	DAI1 Pin 19	Not Muxed	DAI1_PIN19
DAI1_PIN20	DAI1 Pin 20	Not Muxed	DAI1_PIN20
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_A14	DMC0 Address 14	Not Muxed	DMC0_A14
DMC0_A15	DMC0 Address 15	Not Muxed	DMC0_A15
DMC0_BA0	DMC0 Bank Address 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
$\overline{\text{DMC0\_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D02	EPPI0 Data 2	E	PE_10
PPI0_D03	EPPI0 Data 3	E	PE_09
PPI0_D04	EPPI0 Data 4	E	PE_08
PPI0_D05	EPPI0 Data 5	E	PE_07
PPI0_D06	EPPI0 Data 6	E	PE_06
PPI0_D07	EPPI0 Data 7	E	PE_05
PPI0_D08	EPPI0 Data 8	E	PE_04
PPI0_D09	EPPI0 Data 9	E	PE_00
PPI0_D10	EPPI0 Data 10	D	PD_15
PPI0_D11	EPPI0 Data 11	D	PD_14
PPI0_D12	EPPI0 Data 12	B	PB_04
PPI0_D13	EPPI0 Data 13	B	PB_05
PPI0_D14	EPPI0 Data 14	B	PB_00
PPI0_D15	EPPI0 Data 15	B	PB_01
PPI0_D16	EPPI0 Data 16	B	PB_02
PPI0_D17	EPPI0 Data 17	B	PB_03
PPI0_D18	EPPI0 Data 18	D	PD_13
PPI0_D19	EPPI0 Data 19	D	PD_12
PPI0_D20	EPPI0 Data 20	E	PE_13
PPI0_D21	EPPI0 Data 21	E	PE_14
PPI0_D22	EPPI0 Data 22	E	PE_15
PPI0_D23	EPPI0 Data 23	D	PD_00
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_02
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_01
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_15
PWM0_AH	PWM0 Channel A High Side	B	PB_07
PWM0_AL	PWM0 Channel A Low Side	B	PB_08
PWM0_BH	PWM0 Channel B High Side	B	PB_06
PWM0_BL	PWM0 Channel B Low Side	C	PC_00
PWM0_CH	PWM0 Channel C High Side	B	PB_13
PWM0_CL	PWM0 Channel C Low Side	B	PB_14
PWM0_DH	PWM0 Channel D High Side	B	PB_11
PWM0_DL	PWM0 Channel D Low Side	B	PB_12
PWM0_SYNC	PWM0 PWMTMR Grouped	E	PE_09
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	B	PB_15
PWM1_AH	PWM1 Channel A High Side	D	PD_03
PWM1_AL	PWM1 Channel A Low Side	D	PD_04
PWM1_BH	PWM1 Channel B High Side	D	PD_05
PWM1_BL	PWM1 Channel B Low Side	D	PD_06
PWM1_CH	PWM1 Channel C High Side	D	PD_07
PWM1_CL	PWM1 Channel C Low Side	D	PD_08
PWM1_DH	PWM1 Channel D High Side	D	PD_09
PWM1_DL	PWM1 Channel D Low Side	D	PD_10
PWM1_SYNC	PWM1 PWMTMR Grouped	D	PD_11
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	D	PD_02
PWM2_CH	PWM2 Channel C High Side	D	PD_15
PWM2_CL	PWM2 Channel C Low Side	E	PE_00
PWM2_DH	PWM2 Channel D High Side	E	PE_04

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_BMODE0	Boot Mode Control n	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control n	Not Muxed	SYS_BMODE1
SYS_BMODE2	Boot Mode Control n	Not Muxed	SYS_BMODE2
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKIN1	Clock/Crystal Input	Not Muxed	SYS_CLKIN1
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_FAULT	Active High Fault Output	Not Muxed	SYS_FAULT
$\overline{\text{SYS\_FAULT}}$	Active Low Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
SYS_XTAL1	Crystal Output	Not Muxed	SYS_XTAL1
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_14
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_03
TM0_ACI2	TIMER0 Alternate Capture Input 2	D	PD_13
TM0_ACI3	TIMER0 Alternate Capture Input 3	C	PC_07
TM0_ACI4	TIMER0 Alternate Capture Input 4	B	PB_10
TM0_ACLK1	TIMER0 Alternate Clock 1	D	PD_08
TM0_ACLK2	TIMER0 Alternate Clock 2	D	PD_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_01
TM0_CLK	TIMER0 Clock	C	PC_11
TM0_TMR0	TIMER0 Timer 0	E	PE_09
TM0_TMR1	TIMER0 Timer 1	B	PB_15
TM0_TMR2	TIMER0 Timer 2	B	PB_10
TM0_TMR3	TIMER0 Timer 3	B	PB_07
TM0_TMR4	TIMER0 Timer 4	B	PB_08
TM0_TMR5	TIMER0 Timer 5	B	PB_14
TRACE0_CLK	TRACE0 Trace Clock	D	PD_10
TRACE0_D00	TRACE0 Trace Data 0	D	PD_02
TRACE0_D01	TRACE0 Trace Data 1	D	PD_03
TRACE0_D02	TRACE0 Trace Data 2	D	PD_04
TRACE0_D03	TRACE0 Trace Data 3	D	PD_05
TRACE0_D04	TRACE0 Trace Data 4	D	PD_06
TRACE0_D05	TRACE0 Trace Data 5	D	PD_07
TRACE0_D06	TRACE0 Trace Data 6	D	PD_08
TRACE0_D07	TRACE0 Trace Data 7	D	PD_09
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_00
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	C	PC_15
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_14
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_13
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	E	PE_01

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM2_AL	PWM2 Channel A Low Side	F	PF_06
PWM2_BH	PWM2 Channel B High Side	F	PF_09
PWM2_BL	PWM2 Channel B Low Side	F	PF_08
PWM2_CH	PWM2 Channel C High Side	D	PD_15
PWM2_CL	PWM2 Channel C Low Side	E	PE_00
PWM2_DH	PWM2 Channel D High Side	E	PE_04
PWM2_DL	PWM2 Channel D Low Side	E	PE_10
PWM2_SYNC	PWM2 PWMTMR Grouped	E	PE_05
PWM2_TRIP0	PWM2 Shutdown Input 0	D	PD_14
GND	Ground	Not Muxed	GND
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
RTC0_CLKIN	RTC0 Crystal input / external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SINC0_CLK0	SINC0 Clock 0	B	PB_01
SINC0_D0	SINC0 Data 0	A	PA_14
SINC0_D1	SINC0 Data 1	A	PA_15
SINC0_D2	SINC0 Data 2	B	PB_00
SINC0_D3	SINC0 Data 3	B	PB_04
SMC0_A01	SMC0 Address 1	B	PB_05
SMC0_A02	SMC0 Address 2	B	PB_06
SMC0_A03	SMC0 Address 3	B	PB_03
SMC0_A04	SMC0 Address 4	B	PB_02
SMC0_A05	SMC0 Address 5	D	PD_13
SMC0_A06	SMC0 Address 6	D	PD_12
SMC0_A07	SMC0 Address 7	B	PB_01
SMC0_A08	SMC0 Address 8	B	PB_00
SMC0_A09	SMC0 Address 9	A	PA_15
SMC0_A10	SMC0 Address 10	A	PA_14
SMC0_A11	SMC0 Address 11	A	PA_09
SMC0_A12	SMC0 Address 12	A	PA_08
SMC0_A13	SMC0 Address 13	A	PA_13
SMC0_A14	SMC0 Address 14	A	PA_12
SMC0_A15	SMC0 Address 15	A	PA_11
SMC0_A16	SMC0 Address 16	A	PA_07
SMC0_A17	SMC0 Address 17	A	PA_06
SMC0_A18	SMC0 Address 18	A	PA_05
SMC0_A19	SMC0 Address 19	A	PA_04
SMC0_A20	SMC0 Address 20	A	PA_01
SMC0_A21	SMC0 Address 21	A	PA_00
SMC0_A22	SMC0 Address 22	A	PA_10
SMC0_A23	SMC0 Address 23	A	PA_03
SMC0_A24	SMC0 Address 24	A	PA_02
SMC0_A25	SMC0 Address 25	C	PC_12
SMC0_ABE0	SMC0 Byte Enable 0	E	PE_14
SMC0_ABE1	SMC0 Byte Enable 1	E	PE_15
SMC0_AMS0	SMC0 Memory Select 0	C	PC_15
SMC0_AMS1	SMC0 Memory Select 1	E	PE_13

Table 22. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	LP1_CLK	PWM0_BL	SPI0_SEL4	SMC0_ARE	
PC_01	SPI2_CLK				
PC_02	SPI2_MISO				
PC_03	SPI2_MOSI				
PC_04	SPI2_D2				
PC_05	SPI2_D3				
PC_06	SPI2_SEL1				SPI2_SS
PC_07	CAN0_RX	SPI0_SEL1		SMC0_AMS2	TM0_ACI3
PC_08	CAN0_TX			SMC0_AMS3	
PC_09	SPI0_CLK				
PC_10	SPI0_MISO				
PC_11	SPI0_MOSI				TM0_CLK
PC_12	SPI0_SEL3	SPI0_RDY	ACM0_T0	SMC0_A25	
PC_13	UART0_TX	SPI1_SEL1	ACM0_A0		
PC_14	UART0_RX		ACM0_A1		TM0_ACI0
PC_15	UART0_RTS	PPI0_FS3	ACM0_A2	SMC0_AMS0	

Table 23. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00	UART0_CTS	PPI0_D23	ACM0_A3	SMC0_D07	
PD_01	SPI0_SEL2		ACM0_A4	SMC0_AOE	SPI0_SS
PD_02	LP0_D0	PWM1_TRIP0	TRACE0_D00		
PD_03	LP0_D1	PWM1_AH	TRACE0_D01		
PD_04	LP0_D2	PWM1_AL	TRACE0_D02		
PD_05	LP0_D3	PWM1_BH	TRACE0_D03		
PD_06	LP0_D4	PWM1_BL	TRACE0_D04		
PD_07	LP0_D5	PWM1_CH	TRACE0_D05		
PD_08	LP0_D6	PWM1_CL	TRACE0_D06		TM0_ACLK1
PD_09	LP0_D7	PWM1_DH	TRACE0_D07		TM0_ACLK2
PD_10	LP0_CLK	PWM1_DL	TRACE0_CLK		
PD_11	LP0_ACK	PWM1_SYNC			
PD_12	UART2_TX		PPI0_D19	SMC0_A06	
PD_13	UART2_RX		PPI0_D18	SMC0_A05	TM0_ACI2
PD_14	PPI0_D11	PWM2_TRIP0	MLB0_CLKOUT	SMC0_D06	
PD_15	PPI0_D10	PWM2_CH		SMC0_D05	

Table 24. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	PPI0_D09	PWM2_CL		SMC0_D04	
PE_01	PPI0_FS2	SPI0_SEL5	UART1_CTS	C1_FLG0	
PE_02	PPI0_FS1	SPI0_SEL6	UART1_RTS	C2_FLG0	

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DAI1_PIN20	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 20 Notes: No notes
DMC0_A00	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 0 Notes: No notes
DMC0_A01	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 1 Notes: No notes
DMC0_A02	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 2 Notes: No notes
DMC0_A03	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 3 Notes: No notes
DMC0_A04	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 4 Notes: No notes
DMC0_A05	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 5 Notes: No notes
DMC0_A06	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 6 Notes: No notes
DMC0_A07	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 7 Notes: No notes
DMC0_A08	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 8 Notes: No notes
DMC0_A09	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 9 Notes: No notes
DMC0_A10	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 10 Notes: No notes
DMC0_A11	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 11 Notes: No notes
DMC0_A12	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 12 Notes: No notes
DMC0_A13	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 13 Notes: No notes
DMC0_A14	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 14 Notes: No notes
DMC0_A15	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Address 15 Notes: No notes
DMC0_BA0	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 0 Notes: No notes
DMC0_BA1	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 1 Notes: No notes
DMC0_BA2	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 2 Notes: No notes
$\overline{\text{DMC0\_CAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes
DMC0_CK	Output	C	none	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC0_DQ11	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes
DMC0_DQ12	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes
DMC0_DQ13	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes
DMC0_DQ14	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes
DMC0_DQ15	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes
DMC0_LDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes
$\overline{\text{DMC0\_LDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: No notes
DMC0_LDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: External weak pull-down required in LPDDR mode
DMC0_ODT	Output	B	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: No notes
$\overline{\text{DMC0\_RAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes
$\overline{\text{DMC0\_RESET}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Reset (DDR3 only) Notes: No notes
DMC0_RZQ	a	B	none	none	none	VDD_DMC	Desc: DMC0 External calibration resistor connection Notes: Applicable for DDR2 and DDR3 only. External pull-down of 34 ohms need to be added.
DMC0_UDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes
DMC0_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC1_UDM	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Data Mask for Upper Byte Notes: No notes
DMC1_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode
$\overline{\text{DMC1\_UDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Upper Byte (complement) Notes: No notes
DMC1_VREF	a		none	none	none	VDD_DMC	Desc: DMC1 Voltage Reference Notes: No notes
$\overline{\text{DMC1\_WE}}$	Output	B	none	none	none		Desc: DMC1 Write Enable Notes: No notes
GND	g	NA	none	none	none		Desc: Ground Notes: No notes
HADC0_VIN0	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If Input not used connect to GND
HADC0_VIN1	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If Input not used connect to GND
HADC0_VIN2	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If Input not used connect to GND
HADC0_VIN3	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If Input not used connect to GND
HADC0_VIN4	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 4 Notes: If Input not used connect to GND
HADC0_VIN5	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 5 Notes: If Input not used connect to GND
HADC0_VIN6	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 6 Notes: If Input not used connect to GND
HADC0_VIN7	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 7 Notes: If Input not used connect to GND

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 2 | EMAC0 Management Channel Clock | SMC0 Address 24 Notes: No notes
PA_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 3 | EMAC0 Management Channel Serial Data | SMC0 Address 23 Notes: No notes
PA_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 4 | EMAC0 Receive Data 0 | SMC0 Address 19 Notes: No notes
PA_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 5 | EMAC0 Receive Data 1 | SMC0 Address 18 Notes: No notes
PA_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 6 | EMAC0 RXCLK (GigE) or REFCLK (10/100) | SMC0 Address 17 Notes: No notes
PA_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 RXCTL (GigE) or CRS (10/100) | PORTA Position 7 | EMAC0 Carrier Sense/RMII Receive Data Valid | SMC0 Address 16 Notes: No notes
PA_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 8 | EMAC0 Receive Data 2 | SMC0 Address 12 Notes: No notes
PA_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 9 | EMAC0 Receive Data 3 | SMC0 Address 11 Notes: No notes
PA_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 TXCTL (GigE) or TXEN (10/100) | PORTA Position 10 | EMAC0 Transmit Enable | SMC0 Address 22 Notes: No notes
PA_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 11 | EMAC0 Transmit Clock | SMC0 Address 15 Notes: No notes
PA_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 12 | EMAC0 Transmit Data 2 | SMC0 Address 14 Notes: No notes
PA_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 13 | EMAC0 Transmit Data 3 | SMC0 Address 13 Notes: No notes
PA_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 14 | EMAC0 PTP Pulse-Per-Second Output 3 | SINC0 Data 0 | SMC0 Address 10 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 13 | ACM0 ADC Control Signals | SPI1 Slave Select Output 1 | UART0 Transmit Notes: No notes
PC_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 14 | ACM0 ADC Control Signals | UART0 Receive | TIMER0 Alternate Capture Input 0 Notes: No notes
PC_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 15 | ACM0 ADC Control Signals | EPPI0 Frame Sync 3 (FIELD) | SMC0 Memory Select 0 | UART0 Request to Send Notes: No notes
PD_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 0 | ACM0 ADC Control Signals | EPPI0 Data 23 | SMC0 Data 7 | UART0 Clear to Send Notes: No notes
PD_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 1 | ACM0 ADC Control Signals | SMC0 Output Enable | SPI0 Slave Select Output 2 | SPI0 Slave Select Input Notes: No notes
PD_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 2 | LP0 Data 0 | PWM1 Shutdown Input 0 | TRACE0 Trace Data 0 Notes: No notes
PD_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 3 | LP0 Data 1 | PWM1 Channel A High Side | TRACE0 Trace Data 1 Notes: No notes
PD_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 4 | LP0 Data 2 | PWM1 Channel A Low Side | TRACE0 Trace Data 2 Notes: No notes
PD_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 5 | LP0 Data 3 | PWM1 Channel B High Side | TRACE0 Trace Data 3 Notes: No notes
PD_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 6 | LP0 Data 4 | PWM1 Channel B Low Side | TRACE0 Trace Data 4 Notes: No notes
PD_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 7 | LP0 Data 5 | PWM1 Channel C High Side | TRACE0 Trace Data 5 Notes: No notes

Clock Related Operating Conditions

Table 29 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the table applies to all speed grades except where noted.

Table 29. Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$			450	MHz
f_{SYSCLK}	SYSCLK Frequency				225	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$	30		112.5	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			112.5	MHz
f_{DCLK}	LPDDR Clock Frequency				200	MHz
f_{DCLK}	DDR2 Clock Frequency				400	MHz
f_{DCLK}	DDR3 Clock Frequency				450	MHz
f_{OCLK}	Output Clock Frequency[2]				225	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[3, 4]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				75	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				45	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[5]	$f_{PCLKEXT} \leq f_{SCLK1}$			75	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[5, 6]	$f_{PCLKEXT} \leq f_{SCLK1}$			45	MHz
$f_{LCLKTPROG}$	Programmed Link Port Transmit Clock				150	MHz
$f_{LCLKREXT}$	External Link Port Receive Clock[5, 6]	$f_{LCLKEXT} \leq f_{CLKO8}$			150	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				56.25	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				28.125	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[5, 6]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			56.25	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[5, 6]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			28.125	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				75	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				75	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[5, 6]	$f_{SPICLKEXT} \leq f_{SCLK1}$			75	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[5, 6]	$f_{SPICLKEXT} \leq f_{SCLK1}$			45	MHz
$f_{ACLKPROG}$	Programmed ACM Clock				56.25	MHz

[1] The minimum frequency for SCLK0 applies only when using the USB.
[2] f_{OCLK} must not exceed f_{SCLK0} when selected as SYS_CLKOUT.
[3] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors, the measured jitter may be higher or lower than this typical specification for each end application.
[4] The typical value is the percentage of the SYS_CLKOUT period.
[5] The maximum achievable frequency for any peripheral in external clock mode is dependent on the ability to meet the setup and hold times in the ac timing specifications section for that peripheral.
[6] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} (f_{SCLK0} or f_{SCLK1}) that clocks the peripheral.

Asynchronous Read

Table 45 and Figure 12 show asynchronous memory read timing, related to the SMC.

Table 45. Asynchronous Read

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	5.1		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0.7		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		$(RAT – 2.5) \times t_{SCLK0} – 17.5$	ns
Switching Characteristics				
t_{AMSARE}	ADDR/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	$(PREST + RST + PREAT) \times t_{SCLK0} – 2$		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	$(RST + PREAT) \times t_{SCLK0} – 2$		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	$RHT \times t_{SCLK0} –2$		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	$RAT \times t_{SCLK0} – 2$		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	$2.5 \times t_{SCLK0}$	$3.5 \times t_{SCLK0} + 17.5$	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$, $\overline{SMC0\_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

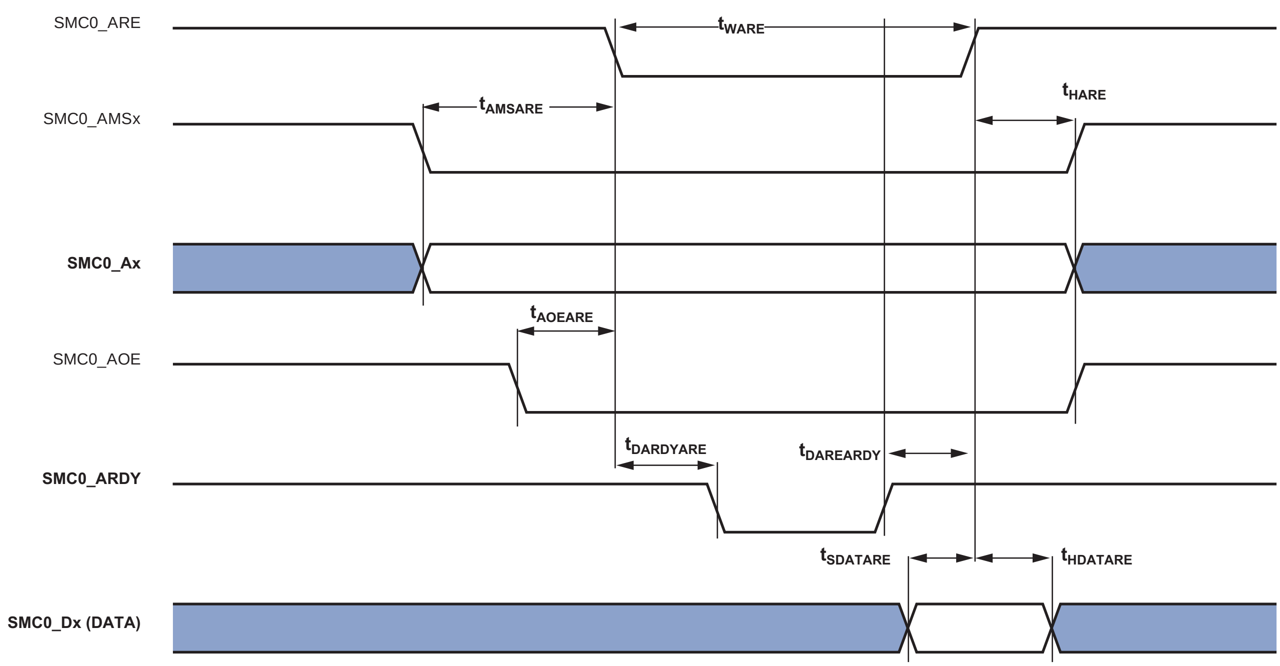

Figure 12. Asynchronous Read

Enhanced Parallel Peripheral Interface (EPPI) Timing

Table 60 and Table 61 and Figure 26 through Figure 34 describe enhanced parallel peripheral interface (EPPI) timing operations. In Figure 26 through Figure 34, POLC[1:0] represents the setting of the EPPI_CTL register, which sets the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated, the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 60. Enhanced Parallel Peripheral Interface (EPPI)—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	0		ns
Switching Characteristics				
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 1.5$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 1.5$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		3.5	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	0.5		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		3.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	0.5		ns

[1] See Table 29 for details on the minimum period that can be programmed for $t_{PCLKPROG}$.

Link Ports (LP)

In LP receive mode, the link port clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by:

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In link port transmit mode, the programmed link port clock ($f_{LCLKTPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{CLKO8}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{CLKO8}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}).

Table 62. Link Ports—Receive[1]

Parameter		Min	Max	Unit
Timing Requirements				
$f_{LCLKREXT}$	LPx_CLK Frequency		150	MHz
t_{SLDCL}	Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL}	Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKEW}	LPx_CLK Period[2]	$t_{LCLKREXT}$ – 0.42		ns
$t_{LCLKRWL}$	LPx_CLK Width Low[2]	0.5 × $t_{LCLKREXT}$		ns
$t_{LCLKRWH}$	LPx_CLK Width High[2]	0.5 × $t_{LCLKREXT}$		ns
Switching Characteristic				
t_{DLALC}	LPx_ACK Low Delay After LPx_CLK Low[3]	1.5 × t_{CLKO8} + 4	2.5 × t_{CLKO8} + 12	ns

[1] Specifications apply to LP0 and LP1.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency see the $f_{LCLKTEXT}$ specification in Table 29.

[3] LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.