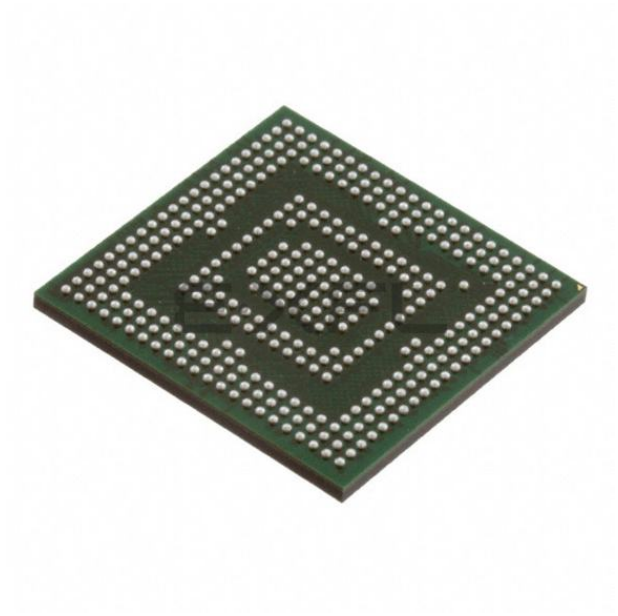

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21584bbcz-4a

GENERAL DESCRIPTION

The ADSP-SC58x/ADSP-2158x processors are members of the SHARC® family of products. The ADSP-SC58x processor is based on the SHARC+ dual core and the ARM® Cortex®-A5 core. The ADSP-SC58x/ADSP-2158x SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI). New additions to the SHARC+ core include cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a set of industry leading system peripherals and memory (see Table 1, Table 2, and Table 3), the ARM Cortex-A5 and SHARC processor is the platform of choice for applications that require programmability similar to RISC (reduced instruction set computing), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, pro audio, and industrial-based applications that require high floating-point performance.

Table 2 provides comparison information for features that vary across the standard processors. (N/A in the table means not applicable.)

Table 3 provides comparison information for features that vary across the automotive processors. (N/A in the table means not applicable.)

Table 1. Common Product Features

Product Features	ADSP-SC58x/ADSP-2158x
DAI (includes SRU)	2
Full SPORTs	4 per DAI
S/PDIF receive/transmit	1per DAI
ASRCs	4 pair per DAI
PCGs	2 per DAI
I^2C (TWI)	3
Quad-data bit SPI	1
Dual-data bit SPI	2
CAN2.0	2
UARTs	3
Link ports	2
Enhanced PPI	1
GP timer[1]	8
GP counter	1
Enhanced PWMs[2]	3
Watchdog timers	2
ADC control module	Yes
Static memory controller	Yes
Hardware accelerators	
High performance FFT/IFFT	Yes
FIR/IIR	Yes
Harmonic analysis engine	Yes
SINC filter	Yes
Security cryptographic engine	Yes
Multichannel 12-bit ADC	8-channel

[1] Eight timers are available in the 529-BGA package only. The 349-BGA package does not include Timer 6 and 7.

[2] Three 3ePWMs are available in the 529-BGA package only. The 349-BGA package does not include PWM 2.

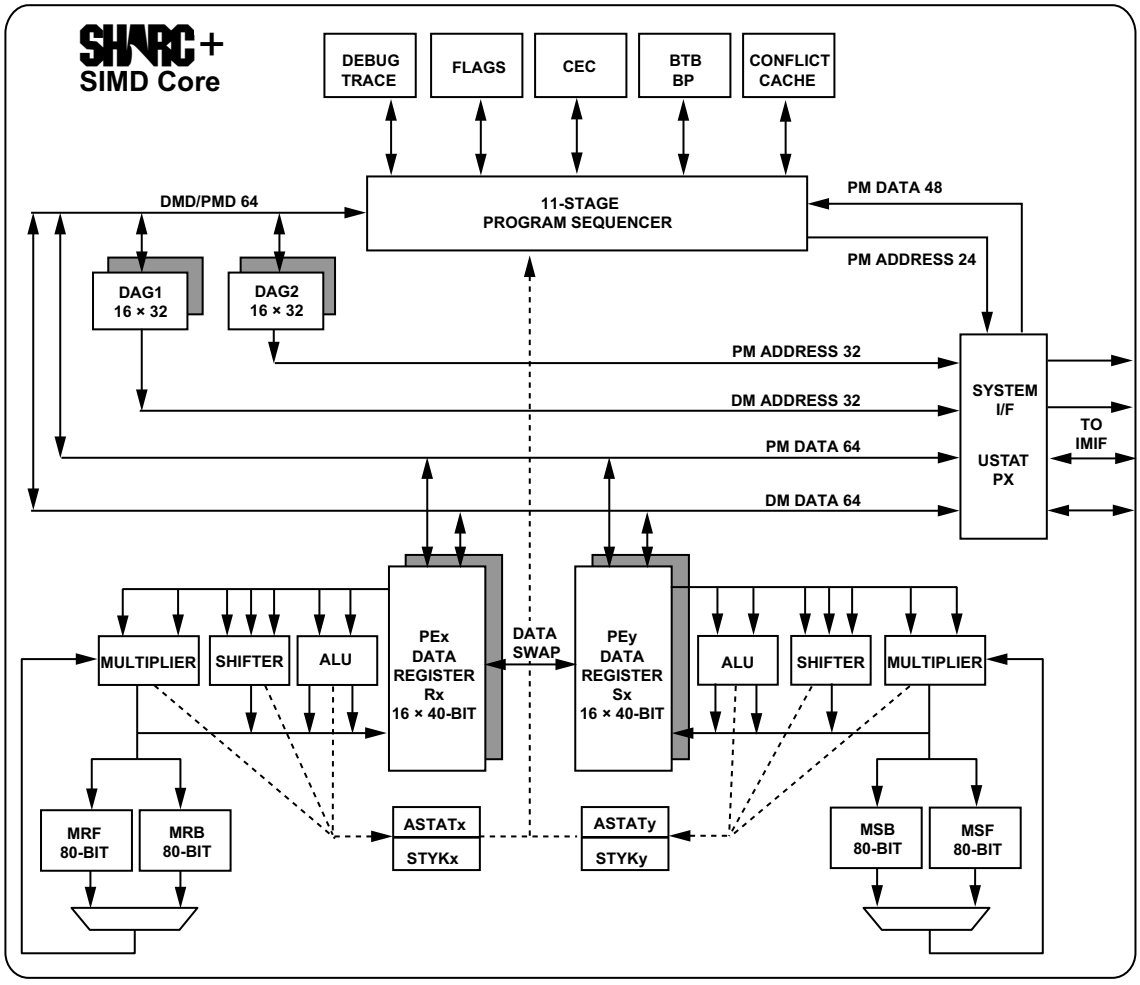


Figure 4. SHARC+ SIMD Core Block Diagram

L1 Memory

Figure 5 shows the ADSP-SC58x/ADSP-2158x memory map. Each SHARC+ core has a tightly coupled L1 SRAM of up to 5 Mb. Each SHARC+ core can access code and data in a single cycle from this memory space. The ARM Cortex-A5 core can also access this memory space with multicycle accesses.

In the SHARC+ core private address space, both cores have L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x 0000 0000 through 0x 0003 FFFF in Normal Word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1024 Kb can be configured for data memory (DM), program memory (PM), and instruction cache. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the DMA engine in a single cycle. The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 Kb DM, 128 Kb PM, and 128 Kb of instruction cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

SYSTEM MEMORY MAP

Table 4. L1 Block 0, Block 1, Block 2, and Block 3 SHARC+ Addressing Memory Map (Private Address Space)

Memory	Long Word (64 Bits)	Extended Precision/ ISA Code (48 Bits)	Normal Word (32 Bits)	Short Word/ VISA Code (16 Bits)	Byte Access (8 Bits)
L1 Block 0 SRAM (1.5 Mb)	0x00048000–0x0004DFFF	0x00090000–0x00097FFF	0x00090000–0x0009BFFF	0x00120000–0x00137FFF	0x00240000–0x0026FFFF
L1 Block 1 SRAM (1.5 Mb)	0x00058000–0x0005DFFF	0x000B0000–0x000B7FFF	0x000B0000–0x000BBFFF	0x00160000–0x00177FFF	0x002C0000–0x002EFFFF
L1 Block 2 SRAM (1 Mb)	0x00060000–0x00063FFF	0x000C0000–0x000C5554	0x000C0000–0x000C7FFF	0x00180000–0x0018FFFF	0x00300000–0x0031FFFF
L1 Block 3 SRAM (1 Mb)	0x00070000–0x00073FFF	0x000E0000–0x000E5554	0x000E0000–0x000E7FFF	0x001C0000–0x001CFFFF	0x00380000–0x0039FFFF

Table 5. L2 Memory Addressing Map

Memory[1]	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	Instruction Fetch VISA Address Space SHARC+	Instruction Fetch ISA Address Space SHARC+
L2 Boot ROM0[2]	ARM: 0x00000000–0x00007FFF SHARC+/DMA: 0x20000000–0x20007FFF	0x08000000–0x08001FFF	0x00B80000–0x00B83FFF	0x00580000–0x00581555
L2 RAM (2 Mb)	0x20080000–0x200BFFFF	0x08020000–0x0802FFFF	0x00BA0000–0x00BBFFFF	0x005A0000–0x005AAAAF
L2 Boot ROM1	0x20100000–0x20107FFF	0x08040000–0x08041FFF	0x00B00000–0x00B03FFF	0x00500000–0x00501555
L2 ROM1	0x20180000–0x201BFFFF	0x08060000–0x0806FFFF	0x00B20000–0x00B3FFFF	0x00520000–0x0052AAAF
L2 Boot ROM2[3]	0x20200000–0x20207FFF	0x08080000–0x08081FFF	0x00B40000–0x00B43FFF	0x00540000–0x00541555
L2 ROM2	0x20280000–0x202BFFFF	0x080A0000–0x080AFFFF	0x00B60000–0x00B7FFFF	0x00560000–0x0056AAAF

[1] All L2 RAM/ROM blocks are subdivided into eight banks.
[2] For ADSP-SC58x products, the L2 Boot ROM0 byte address space is 0x 0000 0000–0x 0000 7FFF.
[3] L2 Boot ROM address for ADSP-2158x products.

Table 6. SHARC+ L1 Memory in Multiprocessor Space

		Memory Block	Byte Address Space for ARM Cortex-A5 and SHARC+	Normal Word Address Space for SHARC+
L1 memory of SHARC1 in multiprocessor space	Address via Slave1 Port	Block 0	0x28240000–0x2826FFFF	0x0A090000–0xA09BFFF
		Block 1	0x282C0000–0x282EFFFF	0x0A0B0000–0xA0BBFFF
		Block 2	0x28300000–0x2831FFFF	0x0A0C0000–0x0A0C7FFF
		Block 3	0x28380000–0x2839FFFF	0x0A0E0000–0x0A0E7FFF
	Address via Slave2 Port	Block 0	0x28640000–0x2866FFFF	0x0A190000–0x0A19BFFF
		Block 1	0x286C0000–0x286EFFFF	0x0A1B0000–0x0A1BBFFF
		Block 2	0x28700000–0x2871FFFF	0x0A1C0000–0x0A1C7FFF
		Block 3	0x28780000–0x2879FFFF	0x0A1E0000–0x0A1E7FFF
L1 memory of SHARC2 in multiprocessor space	Address via Slave1 Port	Block 0	0x28A40000–0x28A6FFFF	0x0A290000–0x0A29BFFF
		Block 1	0x28AC0000–0x28AEFFFF	0x0A2B0000–0x0A2BBFFF
		Block 2	0x28B00000–0x28B1FFFF	0x0A2C0000–0x0A2C7FFF
		Block 3	0x28B80000–0x28B9FFFF	0x0A2E0000–0x0A2E7FFF
	Address via Slave2 Port	Block 0	0x28E40000–0x28E6FFFF	0x0A390000–0x0A39BFFF
		Block 1	0x28EC0000–0x28EEFFFF	0x0A3B0000–0x0A3BBFFF
		Block 2	0x28F00000–0x28F1FFFF	0x0A3C0000–0x0A3C7FFF
		Block 3	0x28F80000–0x28F9FFFF	0x0A3E0000–0x0A3E7FFF

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART1_RTS	UART1 Request to Send	E	PE_02
UART1_RX	UART1 Receive	B	PB_03
UART1_TX	UART1 Transmit	B	PB_02
UART2_CTS	UART2 Clear to Send	E	PE_11
UART2_RTS	UART2 Request to Send	E	PE_10
UART2_RX	UART2 Receive	D	PD_13
UART2_TX	UART2 Transmit	D	PD_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Negative Data (–)	Not Muxed	USB0_DM
USB0_DP	USB0 Positive Data (+)	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_CK	DMC0 Clock (complement)	Not Muxed	DMC0_CK
DMC0_CS0	DMC0 Chip Select 0	Not Muxed	DMC0_CS0
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
DMC0_LDQS	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	DMC0_LDQS
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
DMC0_RAS	DMC0 Row Address Strobe	Not Muxed	DMC0_RAS
DMC0_RESET	DMC0 Reset (DDR3 only)	Not Muxed	DMC0_RESET
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
DMC0_UDQS	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	DMC0_UDQS
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
DMC0_WE	DMC0 Write Enable	Not Muxed	DMC0_WE
DMC1_A00	DMC1 Address 0	Not Muxed	DMC1_A00
DMC1_A01	DMC1 Address 1	Not Muxed	DMC1_A01
DMC1_A02	DMC1 Address 2	Not Muxed	DMC1_A02
DMC1_A03	DMC1 Address 3	Not Muxed	DMC1_A03
DMC1_A04	DMC1 Address 4	Not Muxed	DMC1_A04
DMC1_A05	DMC1 Address 5	Not Muxed	DMC1_A05
DMC1_A06	DMC1 Address 6	Not Muxed	DMC1_A06
DMC1_A07	DMC1 Address 7	Not Muxed	DMC1_A07
DMC1_A08	DMC1 Address 8	Not Muxed	DMC1_A08
DMC1_A09	DMC1 Address 9	Not Muxed	DMC1_A09
DMC1_A10	DMC1 Address 10	Not Muxed	DMC1_A10
DMC1_A11	DMC1 Address 11	Not Muxed	DMC1_A11
DMC1_A12	DMC1 Address 12	Not Muxed	DMC1_A12
DMC1_A13	DMC1 Address 13	Not Muxed	DMC1_A13
DMC1_A14	DMC1 Address 14	Not Muxed	DMC1_A14
DMC1_A15	DMC1 Address 15	Not Muxed	DMC1_A15
DMC1_BA0	DMC1 Bank Address 0	Not Muxed	DMC1_BA0
DMC1_BA1	DMC1 Bank Address 1	Not Muxed	DMC1_BA1

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
ETH0_RXD0	ETH0 Receive Data 0	A	PA_04
ETH0_RXD1	ETH0 Receive Data 1	A	PA_05
ETH0_RXD2	ETH0 Receive Data 2	A	PA_08
ETH0_RXD3	ETH0 Receive Data 3	A	PA_09
ETH0_TXCLK	ETH0 Transmit Clock	A	PA_11
ETH0_TXCTL_TXEN	ETH0 TXCTL (GigE) or TXEN (10/100)	A	PA_10
ETH0_TXD0	ETH0 Transmit Data 0	A	PA_00
ETH0_TXD1	ETH0 Transmit Data 1	A	PA_01
ETH0_TXD2	ETH0 Transmit Data 2	A	PA_12
ETH0_TXD3	ETH0 Transmit Data 3	A	PA_13
ETH0_TXEN	ETH0 Transmit Enable	A	PA_10
ETH1_CRS	ETH1 Carrier Sense/RMII Receive Data Valid	F	PF_13
ETH1_MDC	ETH1 Management Channel Clock	F	PF_14
ETH1_MDIO	ETH1 Management Channel Serial Data	F	PF_15
ETH1_REFCLK	ETH1 Reference Clock	G	PG_00
ETH1_RXD0	ETH1 Receive Data 0	G	PG_04
ETH1_RXD1	ETH1 Receive Data 1	G	PG_05
ETH1_TXD0	ETH1 Transmit Data 0	G	PG_02
ETH1_TXD1	ETH1 Transmit Data 1	G	PG_03
ETH1_TXEN	ETH1 Transmit Enable	G	PG_01
HADC0_EOC_DOUT	HADC0 End of Conversion / Serial Data Out	F	PF_02
HADC0_MUX0	HADC0 Controls to external multiplexer	F	PF_05
HADC0_MUX1	HADC0 Controls to external multiplexer	F	PF_04
HADC0_MUX2	HADC0 Controls to external multiplexer	F	PF_03
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VIN4	HADC0 Analog Input at channel 4	Not Muxed	HADC0_VIN4
HADC0_VIN5	HADC0 Analog Input at channel 5	Not Muxed	HADC0_VIN5
HADC0_VIN6	HADC0 Analog Input at channel 6	Not Muxed	HADC0_VIN6
HADC0_VIN7	HADC0 Analog Input at channel 7	Not Muxed	HADC0_VIN7
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_TCK	TAPC JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	TAPC JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC JTAG Serial Data Out	Not Muxed	JTG_TDO
JTG_TMS	TAPC JTAG Mode Select	Not Muxed	JTG_TMS
$\overline{\text{JTG\_TRST}}$	TAPC JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LP0_ACK	LP0 Acknowledge	D	PD_11
LP0_CLK	LP0 Clock	D	PD_10
LP0_D0	LP0 Data 0	D	PD_02
LP0_D1	LP0 Data 1	D	PD_03
LP0_D2	LP0 Data 2	D	PD_04
LP0_D3	LP0 Data 3	D	PD_05
LP0_D4	LP0 Data 4	D	PD_06
LP0_D5	LP0 Data 5	D	PD_07
LP0_D6	LP0 Data 6	D	PD_08

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
LP0_D7	LP0 Data 7	D	PD_09
LP1_ACK	LP1 Acknowledge	B	PB_15
LP1_CLK	LP1 Clock	C	PC_00
LP1_D0	LP1 Data 0	B	PB_07
LP1_D1	LP1 Data 1	B	PB_08
LP1_D2	LP1 Data 2	B	PB_09
LP1_D3	LP1 Data 3	B	PB_10
LP1_D4	LP1 Data 4	B	PB_11
LP1_D5	LP1 Data 5	B	PB_12
LP1_D6	LP1 Data 6	B	PB_13
LP1_D7	LP1 Data 7	B	PB_14
MLB0_CLKN	MLB0 Differential Clock (–)	Not Muxed	MLB0_CLKN
MLB0_CLKP	MLB0 Differential Clock (+)	Not Muxed	MLB0_CLKP
MLB0_DATN	MLB0 Differential Data (–)	Not Muxed	MLB0_DATN
MLB0_DATP	MLB0 Differential Data (+)	Not Muxed	MLB0_DATP
MLB0_SIGN	MLB0 Differential Signal (–)	Not Muxed	MLB0_SIGN
MLB0_SIGP	MLB0 Differential Signal (+)	Not Muxed	MLB0_SIGP
MLB0_CLK	MLB0 Single-Ended Clock	B	PB_04
MLB0_DAT	MLB0 Single-Ended Data	B	PB_06
MLB0_SIG	MLB0 Single-Ended Signal	B	PB_05
MLB0_CLKOUT	MLB0 Single-Ended Clock Out	D	PD_14
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	F	PF_12
MSI0_CLK	MSI0 Clock	F	PF_11
MSI0_CMD	MSI0 Command	F	PF_10
MSI0_D0	MSI0 Data 0	F	PF_02
MSI0_D1	MSI0 Data 1	F	PF_03
MSI0_D2	MSI0 Data 2	F	PF_04
MSI0_D3	MSI0 Data 3	F	PF_05
MSI0_D4	MSI0 Data 4	F	PF_06
MSI0_D5	MSI0 Data 5	F	PF_07
MSI0_D6	MSI0 Data 6	F	PF_08
MSI0_D7	MSI0 Data 7	F	PF_09
$\overline{\text{MSI0\_INT}}$	MSI0 eSDIO Interrupt Input	F	PF_13
PA_00-15	PORTA Position 00 through Position 15	A	PA_00-15
PB_00-15	PORTB Position 00 through Position 15	B	PB_00-15
PCIE0_CLKM	PCIE0 CLK -	Not Muxed	PCIE0_CLKM
PCIE0_CLKP	PCIE0 CLK +	Not Muxed	PCIE0_CLKP
PCIE0_REF	PCIE0 Reference	Not Muxed	PCIE0_REF
PCIE0_RXM	PCIE0 RX -	Not Muxed	PCIE0_RXM
PCIE0_RXP	PCIE0 RX +	Not Muxed	PCIE0_RXP
PCIE0_TXM	PCIE0 TX -	Not Muxed	PCIE0_TXM
PCIE0_TXP	PCIE0 TX +	Not Muxed	PCIE0_TXP
PC_00-15	PORTC Position 00 through Position 15	C	PC_00-15
PD_00-15	PORTD Position 00 through Position 15	D	PD_00-15
PE_00-15	PORTE Position 00 through Position 15	E	PE_00-15
PF_00-15	PORTF Position 00 through Position 15	F	PF_00-15
PG_00-5	PORTG Position 00 through Position 5	G	PG_00-5
PPI0_CLK	EPPI0 Clock	E	PE_03

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.1	1.15	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_RTC}	RTC Voltage		2.0	3.3	3.60	V
$V_{DD\_PCIE\_TX}$	PCIe Core Transmit Voltage		1.05	1.1	1.15	V
$V_{DD\_PCIE\_RX}$	PCIe Core Receive Voltage		1.05	1.1	1.15	V
V_{DD_PCIE}	PCIe Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = maximum	2.0			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.8	V
$V_{IL\_DDR2/3}$[5]	Low Level Input Voltage	V_{DD_DMC} = minimum			V_{REF} – 0.25	V
$V_{IH\_DDR2/3}$[5]	High Level Input Voltage	V_{DD_DMC} = maximum	V_{REF} + 0.25			V
V_{IL_LPDDR}[6]	Low Level Input Voltage	V_{DD_DMC} = minimum			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[6]	High Level Input Voltage	V_{DD_DMC} = maximum	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		100	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+110	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +95°C	–40		+125	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		110	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+125	°C
AUTOMOTIVE USE ONLY						
T_J	Junction Temperature 349-Lead CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ –40°C to +105°C	–40		+133[7]	°C

[1] Applies to DDR2/DDR3/LPDDR signals.
[2] If not used, V_{DD_USB} must be connected to 3.3V.
[3] V_{HADC_VREF} must always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional pins except the TWI, DMC, USB, PCIe, and MLB pins.
[5] This parameter applies to all DMC0/1 signals in DDR2/DDR3 mode. V_{REF} is the voltage applied to the V_{REF_DMC} pin, nominally $V_{DD\_DMC/2}$.
[6] This parameter applies to DMC0/1 signals in LPDDR mode.
[7] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Table 28. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_VSEL Selections	V_{DD_EXT} Nominal	V_{BUSTWI}			Unit
		Min	Nominal	Max	
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	450 MHz Min	450 MHz Typ	450 MHz Max	Unit
V_{OH}[1]	High Level Output Voltage	At V_{DD_EXT} = minimum, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	At V_{DD_EXT} = minimum, I_{OL} = 1.0 mA[2]			0.4	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_LPDDR}[5]	High Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OH} = –6.0 mA	1.38			V
V_{OL_LPDDR}[5]	Low Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OL} = 6.0 mA			0.32	V
I_{IH}[6, 7]	High Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			10	µA
I_{IL}[6]	Low Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = 0 V			10	µA
I_{IL_PU}[7]	Low Level Input Current Pull-up	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{IH_PD}[8]	High Level Input Current Pull-down	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{OZH}[9]	Three-State Leakage Current	At V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = V_{DD_EXT}/V_{DD_DDR} maximum			10	µA
I_{OZL}[9]	Three-State Leakage Current	at V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = 0 V			10	µA
C_{IN}[10]	Input Capacitance	T_{CASE} = 25°C			5	pF

Clock and Reset Timing

Table 44 and Figure 11 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLK, DCLK, and OCLK timing specifications in Table 29, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 44. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKINx Frequency (Crystal)[1, 2, 3]	20	50	MHz
	SYS_CLKINx Frequency (External CLKIN)[1, 2, 3]	20	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 11) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 43 and Figure 10 for power-up reset timing.

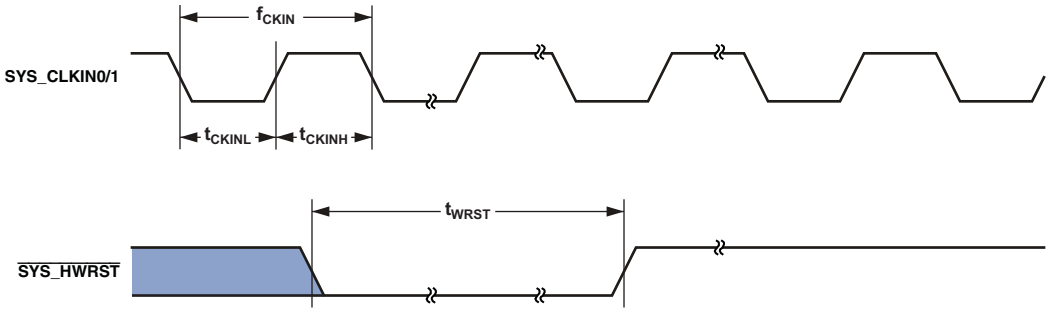


Figure 11. Clock and Reset Timing

DDR2 SDRAM Read Cycle Timing

Table 52 and Figure 18 show DDR2 SDRAM read cycle timing, related to the DMC.

Table 52. DDR2 SDRAM Read Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		400 MHz[2] Min	400 MHz[2] Max	Unit
Timing Requirements				
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQxx Signals		0.2	ns
t_{QH}	DMCx_DQxx, DMCx_DQS Output Hold Time From DMCx_DQS	0.9		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

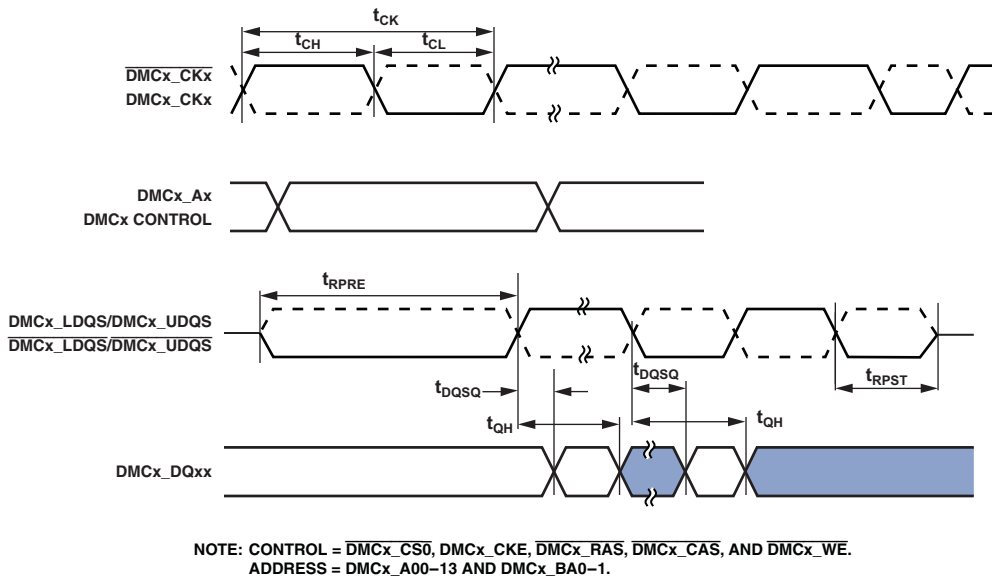


Figure 18. DDR2 SDRAM Controller Input AC Timing

DDR3 SDRAM Clock and Control Cycle Timing

Table 57 and Figure 23 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 57. DDR3 SDRAM Clock and Control Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[3]	Minimum Clock Pulse Width	0.43	0.57	t_{CK}
$t_{CL(abs)}$[3]	Maximum Clock Pulse Width	0.43	0.57	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	0.275		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-3F definition.

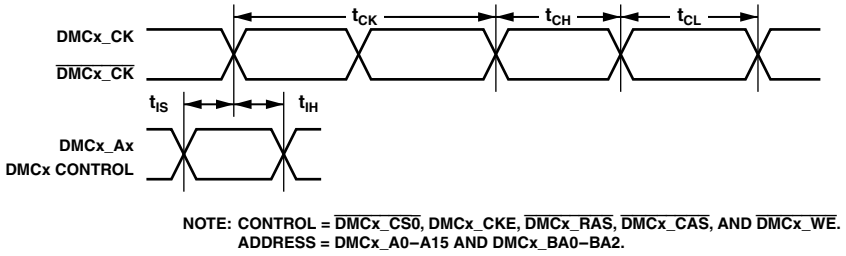


Figure 23. DDR3 SDRAM Clock and Control Cycle Timing

DDR3 SDRAM Read Cycle Timing

Table 58 and Figure 24 show mobile DDR3 SDRAM read cycle timing, related to the DMC.

Table 58. DDR3 SDRAM Read Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	Max	Unit
Timing Requirements				
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQ Signals		0.2	ns
t_{QH}	DMCx_DQ, DMCx_DQS Output Hold Time From DMCx_DQS	0.38		t_{CK}
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.3		t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

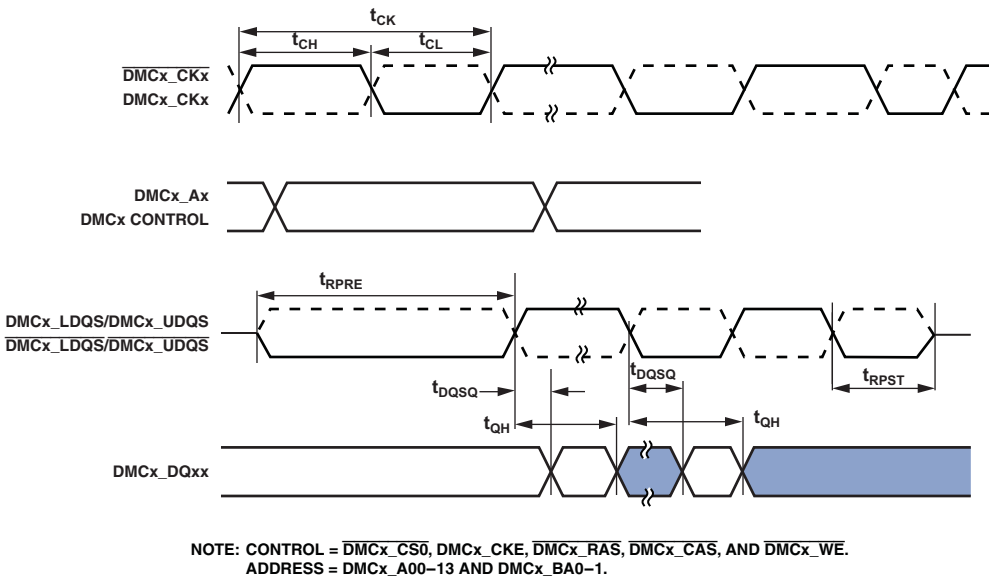


Figure 24. DDR3 SDRAM Controller Input AC Timing

SPI Port—Slave Timing

Table 72 and Figure 44 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 72. SPI Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLK} - 1$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

[1] All specifications apply to all three SPIs.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in Table 29.

SPI Port—Open Drain Mode (ODM) Timing

In Figure 46 and Figure 47 and Table 75 and Table 76, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3 depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 74. SPI Port ODM Master Mode Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance from Data Out Valid	–1		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid from High Impedance	–1	+6	ns

[1] All specifications apply to all three SPIs.

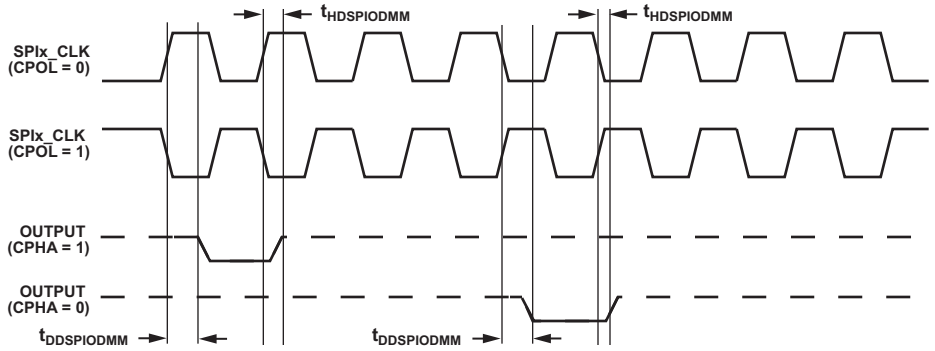


Figure 46. ODM Master Mode

Table 75. SPI Port—ODM Slave Mode[1]

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

[1] All specifications apply to all three SPIs.

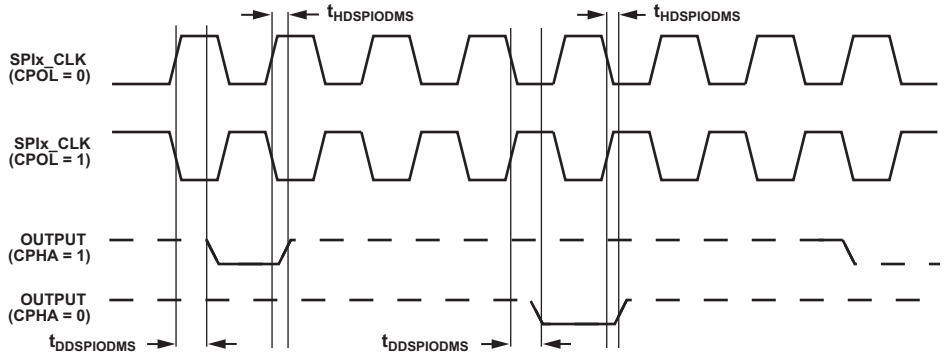


Figure 47. ODM Slave Mode

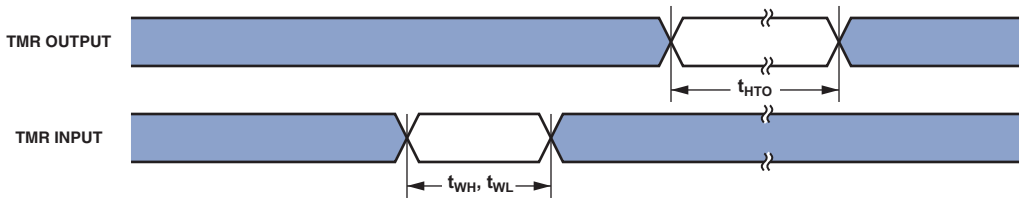


Figure 52. Timer Cycle Timing

DAIx Pin to DAIx Pin Direct Routing (DAI0 Block and DAI1 Block)

Table 81 and Figure 53 describe I/O timing related to the digital audio interface (DAI) for direct pin connections only (for example, DAIx_PB01_I to DAIx_PB02_O).

Table 81. DAI Pin to DAI Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	12	ns

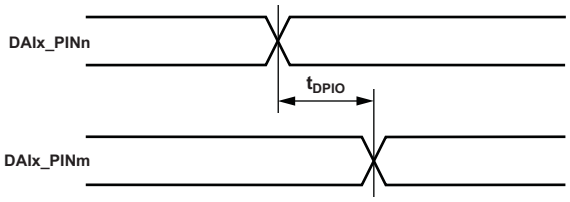


Figure 53. DAI Pin to DAI Pin Direct Routing

Up/Down Counter/Rotary Encoder Timing

Table 82 and Figure 54 describe timing related to the general-purpose counter (CNT).

Table 82. Up/Down Counter/Rotary Encoder Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		ns

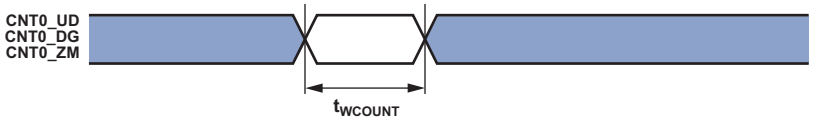


Figure 54. Up/Down Counter/Rotary Encoder Timing

Mobile Storage Interface (MSI) Controller Timing

Table 101 and Figure 74 show I/O timing related to the MSI.

Table 101. MSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	4.8		ns
t_{IH}	Input Hold Time	–0.5		ns
Switching Characteristics				
f_{PP}	Clock Frequency Data Transfer Mode[1]		50	MHz
t_{WL}	Clock Low Time	8		ns
t_{WH}	Clock High Time	8		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		2	ns
t_{OH}	Output Hold Time	–1.8		ns

[1] $t_{PP} = 1/f_{PP}$.

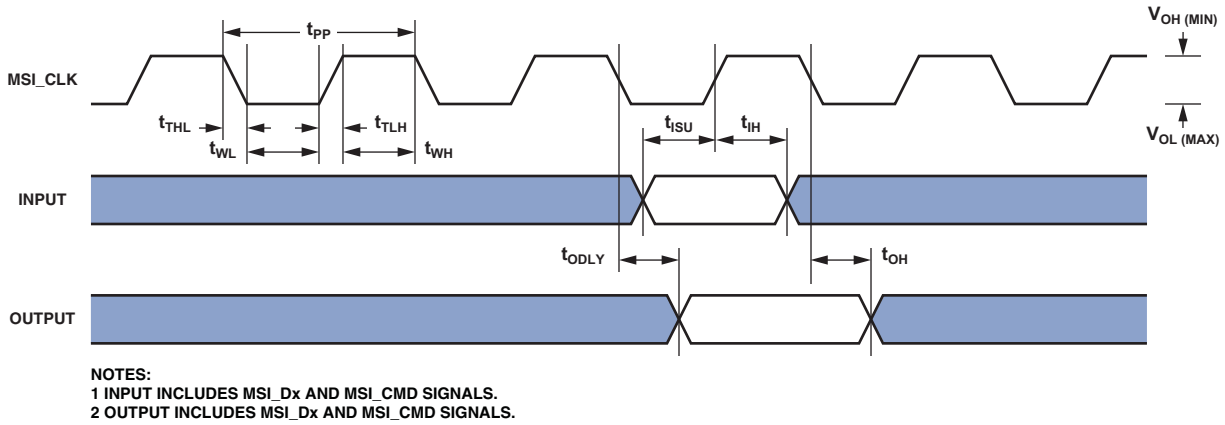


Figure 74. MSI Controller Timing

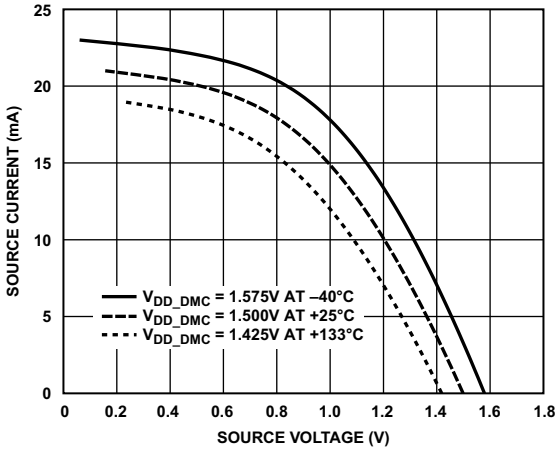


Figure 82. Driver Type B and Driver Type C (DDR3 Drive Strength 40 Ω)

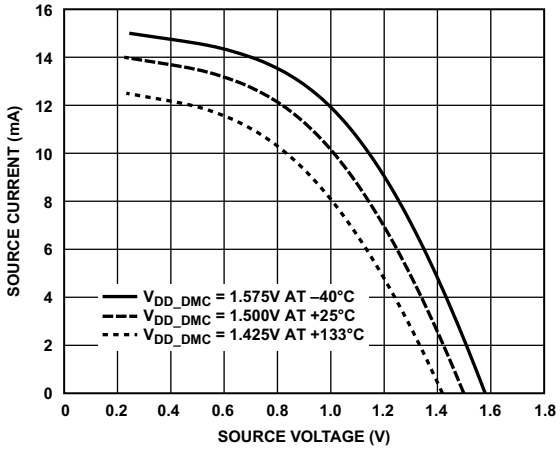


Figure 83. Driver Type B and Driver Type C (DDR3 Drive Strength 60 Ω)

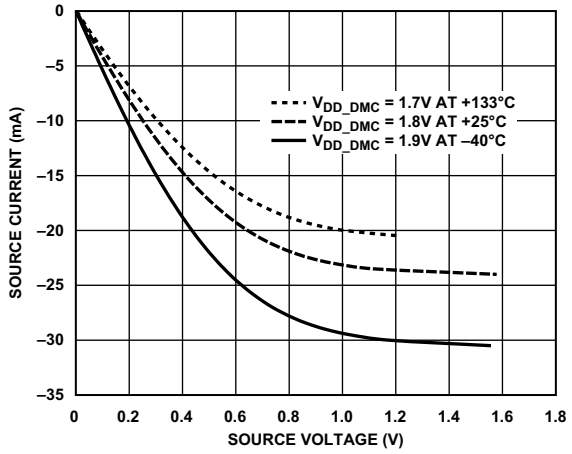


Figure 84. Driver Type B and Driver Type C (DDR2 Drive Strength 40 Ω)

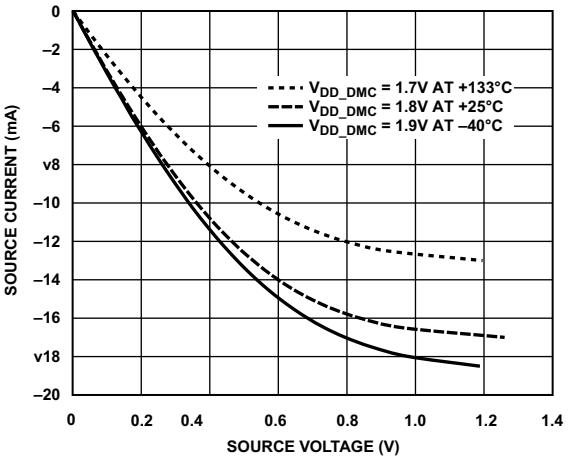


Figure 85. Driver Type B and Driver Type C (DDR2 Drive Strength 60Ω)

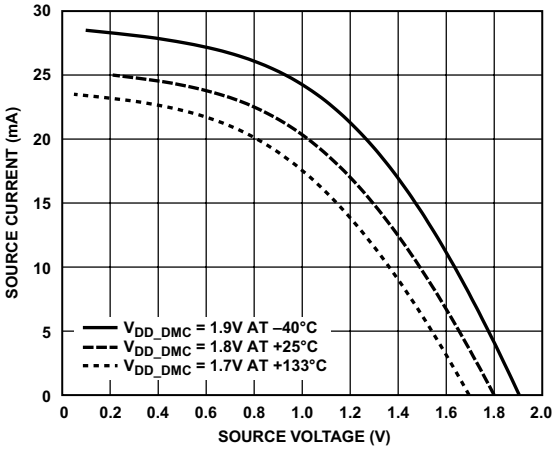


Figure 86. Driver Type B and Driver Type C (DDR2 Drive Strength 40Ω)

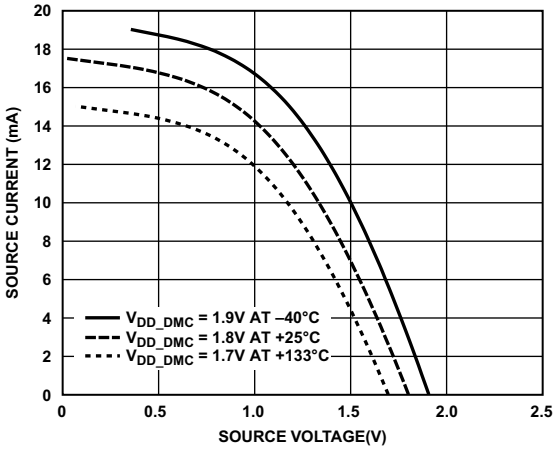


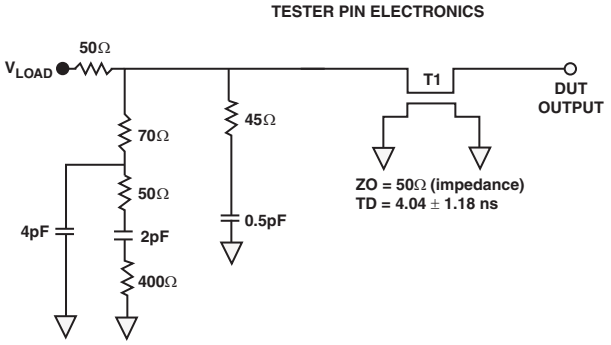
Figure 87. Driver Type B and Driver Type C (DDR2 Drive Strength 60 Ω)

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the output voltage of the processor and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line) and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications section.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 92). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 93 through Figure 97 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 92. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

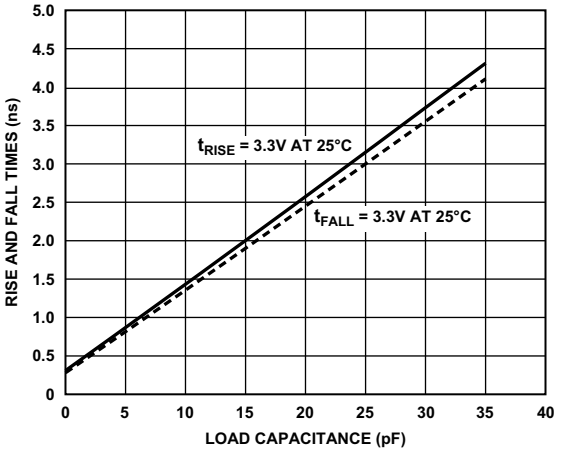


Figure 93. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

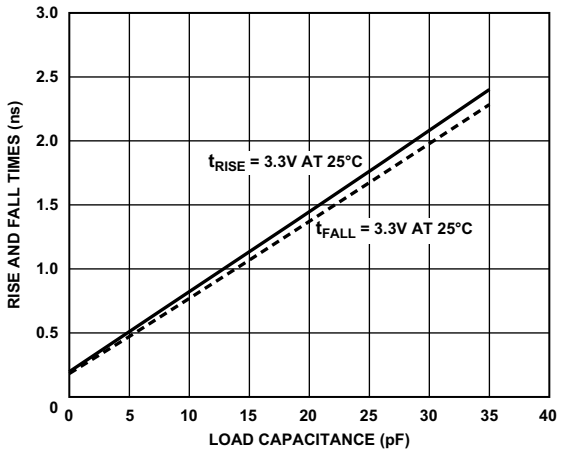


Figure 94. Driver Type H Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

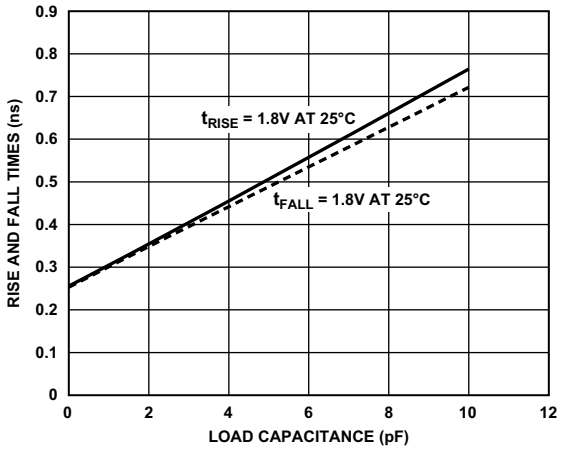


Figure 95. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for LPDDR

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
H04	DMC0_A00	K05	VDD_INT	M06	VDD_DMC	P07	GND
H05	VDD_INT	K06	VDD_DMC	M07	GND	P08	GND
H06	VDD_DMC	K07	GND	M08	GND	P09	GND
H07	VDD_DMC	K08	GND	M09	GND	P10	GND
H08	VDD_DMC	K09	GND	M10	GND	P11	GND
H09	VDD_DMC	K10	GND	M11	GND	P12	GND
H10	VDD_DMC	K11	GND	M12	GND	P13	GND
H11	VDD_DMC	K12	GND	M13	GND	P14	GND
H12	VDD_DMC	K13	GND	M14	GND	P15	GND
H13	VDD_DMC	K14	GND	M15	GND	P16	GND
H14	VDD_DMC	K15	GND	M16	GND	P17	GND
H15	VDD_DMC	K16	GND	M17	GND	P18	VDD_EXT
H16	VDD_DMC	K17	GND	M18	VDD_EXT	P19	PF_10
H17	VDD_DMC	K18	VDD_EXT	M19	PE_08	P20	PF_08
H18	VDD_DMC	K19	VDD_INT	M20	PE_11	P21	PF_15
H19	VDD_INT	K20	PD_15	M21	PF_03	P22	PF_12
H20	SYS_CLKOUT	K21	PF_11	M22	PF_00	P23	PG_00
H21	PE_12	K22	PF_06	M23	PF_02	R01	SYS_XTAL1
H22	PE_05	K23	PE_10	N01	JTG_TMS	R02	SYS_BMODE1
H23	PE_02	L01	PC_04	N02	$\overline{\text{JTG\_TRST}}$	R03	SYS_BMODE2
J01	DMC0_A15	L02	PC_12	N03	$\overline{\text{SYS\_HWRST}}$	R04	SYS_BMODE0
J02	DMC0_A10	L03	PC_07	N04	PC_03	R05	VDD_INT
J03	DMC0_A08	L04	PC_10	N05	VDD_INT	R06	VDD_EXT
J04	PC_08	L05	VDD_INT	N06	VDD_EXT	R07	GND
J05	VDD_INT	L06	VDD_DMC	N07	GND	R08	GND
J06	VDD_DMC	L07	GND	N08	GND	R09	GND
J07	GND	L08	GND	N09	GND	R10	GND
J08	GND	L09	GND	N10	GND	R11	GND
J09	GND	L10	GND	N11	GND	R12	GND
J10	GND	L11	GND	N12	GND	R13	GND
J11	GND	L12	GND	N13	GND	R14	GND
J12	GND	L13	GND	N14	GND	R15	GND
J13	GND	L14	GND	N15	GND	R16	GND
J14	GND	L15	GND	N16	GND	R17	GND
J15	GND	L16	GND	N17	GND	R18	VDD_EXT
J16	GND	L17	GND	N18	VDD_EXT	R19	VDD_INT
J17	GND	L18	VDD_EXT	N19	VDD_INT	R20	PG_01
J18	VDD_EXT	L19	VDD_INT	N20	PE_15	R21	PG_05
J19	PD_03	L20	PE_03	N21	PF_04	R22	PG_04
J20	PD_07	L21	PF_09	N22	PF_05	R23	PF_13
J21	PF_14	L22	PE_09	N23	PF_07	T01	SYS_CLKIN1
J22	PF_01	L23	PE_14	P01	JTG_TDO	T02	PB_15
J23	PE_07	M01	PC_01	P02	JTG_TDI	T03	GND
K01	$\overline{\text{DMC0\_RESET}}$	M02	PC_05	P03	SYS_FAULT	T04	PB_14
K02	PC_11	M03	PC_02	P04	JTG_TCK	T05	VDD_INT
K03	PC_06	M04	$\overline{\text{SYS\_FAULT}}$	P05	VDD_INT	T06	VDD_EXT
K04	PC_09	M05	VDD_INT	P06	VDD_EXT	T07	GND