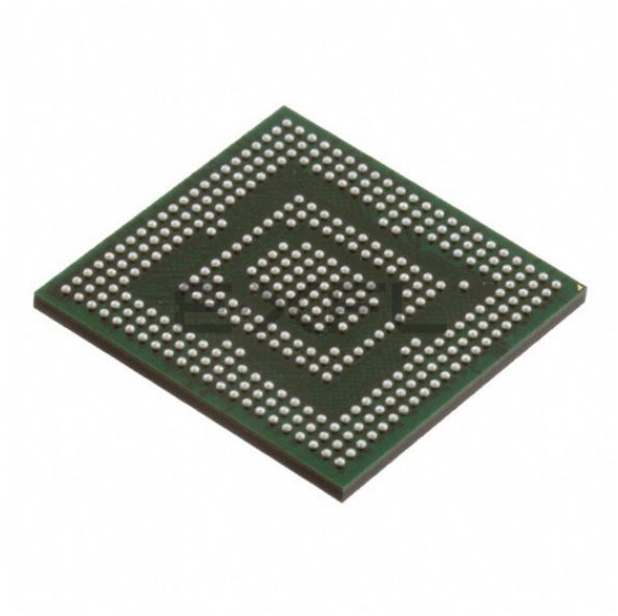

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21584kbcz-4a

The memory map in Table 4 gives the L1 memory address space and shows multiple L1 memory blocks offering a configurable mix of SRAM and cache.

L1 Master and Slave Ports

Each SHARC+ core has two master and two slave ports to and from the system fabric. One master port fetches instructions. The second master port drives data to the system world. Both slave ports allow conflict free core/direct memory access (DMA) streams to the individual memory blocks. For slave port addresses, refer to the L1 memory address map in Table 4.

L1 On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is realized using both the DMD and PMD buses.

Instruction and Data Cache

The ADSP-SC58x/ADSP-2158x processors also include a traditional instruction cache (I-cache) and two data caches (D-cache) (PM and DM caches). These caches support one instruction access and two data accesses over the DM and PM buses, per CCLK cycle. The cache controllers automatically manage the configured L1 memory. The system can configure part of the L1 memory for automatic management by the cache controllers. The sizes of these caches are independently configurable from 0 kB to a maximum of 128 kB each. The memory not managed by the cache controllers is directly addressable by the processors. The controllers ensure the data coherence between the two data caches. The caches provide user-controllable features such as full and partial locking, range-bound invalidation, and flushing.

System Event Controller (SEC) Input

The output of the system event controller (SEC) controller is forwarded to the core event controller (CEC) to respond directly to all unmasked system-based interrupts. The SEC also supports nesting including various SEC interrupt channel arbitration options. For all SEC channels, the processor automatically stacks the arithmetic status (ASTATx and ASTATy) registers and mode (MODE1) register in parallel with the interrupt servicing.

Core Memory-Mapped Registers (CMMR)

The core memory-mapped registers control the L1 instruction and data cache, BTB, L2 cache, parity error, system control, debug, and monitor functions.

SHARC+ CORE ARCHITECTURE

The ADSP-SC58x/ADSP-2158x processors are code compatible at the assembly level with the ADSP-2148x, ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-2116x, and with the first-generation ADSP-2106x SHARC processors.

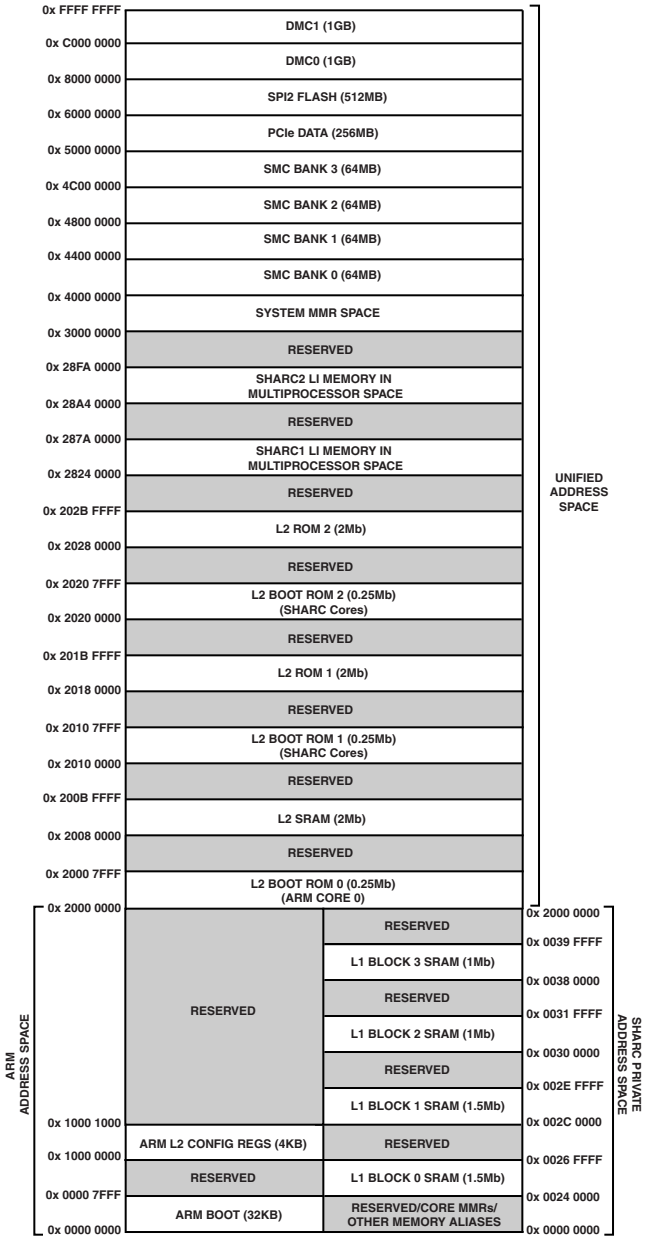


Figure 5. ADSP-SC58x/ADSP-2158x Memory Map

The ADSP-SC58x/ADSP-2158x processors share architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-214xx, and ADSP-2116x SIMD SHARC processors, shown in Figure 4 and detailed in the following sections.

SIMD Computational Engine

The SHARC+ core contains two computational processing elements that operate as a single-instruction, multiple data (SIMD) engine.

The reset target is defined as the following:

- System reset—all functional units except the RCU are set to default states.
- Hardware reset—all functional units are set to default states without exception. History is lost.
- Core only reset— affects the core only. When in reset state, the core is not accessed by any bus master.

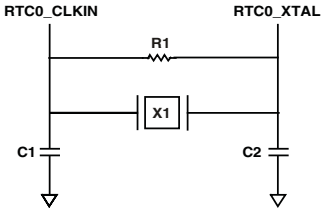
The reset source is defined as the following:

- System reset—can be triggered by software (writing to the RCU_CTL register) or by another functional unit such as the dynamic power management (DPM) unit or any of the SEC, TRU, or emulator inputs.
- Hardware reset—the $\overline{\text{SYS\_HWRST}}$ input signal asserts active (pulled down).
- Core only reset—affects only the core. The core is not accessed by any bus master when in reset state.
- Trigger request (peripheral).

Real-Time Clock (RTC)

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. Connect the RTC0_CLKIN and RTC0_XTAL pins with external components as shown in Figure 6.

The RTC peripheral has dedicated power supply pins so it can remain powered up and clocked even when the remainder of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks; interrupt on programmable stopwatch countdown; or interrupt at a programmed alarm time.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS.

Figure 6. External Components for RTC

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register (RTC_ALARM). There are two alarms: a time of day and a day and time of that day.

The stopwatch function counts down from a programmed value, with 1 sec resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

Clock Generation Unit (CGU)

The ADSP-SC58x/ADSP-2158x processors support two independent PLLs. Each PLL is part of a clock generation unit (CGU); see Figure 8. Each CGU can be either driven externally by the same clock source or each can be driven by separate sources. This provides flexibility in determining the internal clocking frequencies for each clock domain.

Frequencies generated by each CGU are derived from a common multiplier with different divider values available for each output.

The CGU generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency.

Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks, the DDR1/DDR2/DDR3 clock (DCLK), and the output clock (OCLK). For more information on clocking, see the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value and the PLL logic executes the changes so it transitions smoothly from the current conditions to the new conditions.

System Crystal Oscillator and USB Crystal Oscillator

The processor can be clocked by an external crystal (see Figure 7), a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If using an external clock, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the SYS_CLKINx pin and the USB_CLKIN pin of the processor. When using an external clock, the SYS_XTALx pin and the USB_XTAL pin must be left unconnected. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal can be used.

For fundamental frequency operation, use the circuit shown in Figure 7. A parallel resonant, fundamental frequency, microprocessor grade crystal is connected across the SYS_CLKINx pin and the SYS_XTALx pin. The on-chip resistance between the SYS_CLKINx pin and the SYS_XTALx pin is in the 500 kΩ range. Further parallel resistors are typically not recommended.

The two capacitors and the series resistor, shown in Figure 7, fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 7 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D02	EPPI0 Data 2	E	PE_10
PPI0_D03	EPPI0 Data 3	E	PE_09
PPI0_D04	EPPI0 Data 4	E	PE_08
PPI0_D05	EPPI0 Data 5	E	PE_07
PPI0_D06	EPPI0 Data 6	E	PE_06
PPI0_D07	EPPI0 Data 7	E	PE_05
PPI0_D08	EPPI0 Data 8	E	PE_04
PPI0_D09	EPPI0 Data 9	E	PE_00
PPI0_D10	EPPI0 Data 10	D	PD_15
PPI0_D11	EPPI0 Data 11	D	PD_14
PPI0_D12	EPPI0 Data 12	B	PB_04
PPI0_D13	EPPI0 Data 13	B	PB_05
PPI0_D14	EPPI0 Data 14	B	PB_00
PPI0_D15	EPPI0 Data 15	B	PB_01
PPI0_D16	EPPI0 Data 16	B	PB_02
PPI0_D17	EPPI0 Data 17	B	PB_03
PPI0_D18	EPPI0 Data 18	D	PD_13
PPI0_D19	EPPI0 Data 19	D	PD_12
PPI0_D20	EPPI0 Data 20	E	PE_13
PPI0_D21	EPPI0 Data 21	E	PE_14
PPI0_D22	EPPI0 Data 22	E	PE_15
PPI0_D23	EPPI0 Data 23	D	PD_00
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_02
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_01
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_15
PWM0_AH	PWM0 Channel A High Side	B	PB_07
PWM0_AL	PWM0 Channel A Low Side	B	PB_08
PWM0_BH	PWM0 Channel B High Side	B	PB_06
PWM0_BL	PWM0 Channel B Low Side	C	PC_00
PWM0_CH	PWM0 Channel C High Side	B	PB_13
PWM0_CL	PWM0 Channel C Low Side	B	PB_14
PWM0_DH	PWM0 Channel D High Side	B	PB_11
PWM0_DL	PWM0 Channel D Low Side	B	PB_12
PWM0_SYNC	PWM0 PWMTMR Grouped	E	PE_09
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	B	PB_15
PWM1_AH	PWM1 Channel A High Side	D	PD_03
PWM1_AL	PWM1 Channel A Low Side	D	PD_04
PWM1_BH	PWM1 Channel B High Side	D	PD_05
PWM1_BL	PWM1 Channel B Low Side	D	PD_06
PWM1_CH	PWM1 Channel C High Side	D	PD_07
PWM1_CL	PWM1 Channel C Low Side	D	PD_08
PWM1_DH	PWM1 Channel D High Side	D	PD_09
PWM1_DL	PWM1 Channel D Low Side	D	PD_10
PWM1_SYNC	PWM1 PWMTMR Grouped	D	PD_11
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	D	PD_02
PWM2_CH	PWM2 Channel C High Side	D	PD_15
PWM2_CL	PWM2 Channel C Low Side	E	PE_00
PWM2_DH	PWM2 Channel D High Side	E	PE_04

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
ETH0_RXD0	ETH0 Receive Data 0	A	PA_04
ETH0_RXD1	ETH0 Receive Data 1	A	PA_05
ETH0_RXD2	ETH0 Receive Data 2	A	PA_08
ETH0_RXD3	ETH0 Receive Data 3	A	PA_09
ETH0_TXCLK	ETH0 Transmit Clock	A	PA_11
ETH0_TXCTL_TXEN	ETH0 TXCTL (GigE) or TXEN (10/100)	A	PA_10
ETH0_TXD0	ETH0 Transmit Data 0	A	PA_00
ETH0_TXD1	ETH0 Transmit Data 1	A	PA_01
ETH0_TXD2	ETH0 Transmit Data 2	A	PA_12
ETH0_TXD3	ETH0 Transmit Data 3	A	PA_13
ETH0_TXEN	ETH0 Transmit Enable	A	PA_10
ETH1_CRS	ETH1 Carrier Sense/RMII Receive Data Valid	F	PF_13
ETH1_MDC	ETH1 Management Channel Clock	F	PF_14
ETH1_MDIO	ETH1 Management Channel Serial Data	F	PF_15
ETH1_REFCLK	ETH1 Reference Clock	G	PG_00
ETH1_RXD0	ETH1 Receive Data 0	G	PG_04
ETH1_RXD1	ETH1 Receive Data 1	G	PG_05
ETH1_TXD0	ETH1 Transmit Data 0	G	PG_02
ETH1_TXD1	ETH1 Transmit Data 1	G	PG_03
ETH1_TXEN	ETH1 Transmit Enable	G	PG_01
HADC0_EOC_DOUT	HADC0 End of Conversion / Serial Data Out	F	PF_02
HADC0_MUX0	HADC0 Controls to external multiplexer	F	PF_05
HADC0_MUX1	HADC0 Controls to external multiplexer	F	PF_04
HADC0_MUX2	HADC0 Controls to external multiplexer	F	PF_03
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VIN4	HADC0 Analog Input at channel 4	Not Muxed	HADC0_VIN4
HADC0_VIN5	HADC0 Analog Input at channel 5	Not Muxed	HADC0_VIN5
HADC0_VIN6	HADC0 Analog Input at channel 6	Not Muxed	HADC0_VIN6
HADC0_VIN7	HADC0 Analog Input at channel 7	Not Muxed	HADC0_VIN7
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_TCK	TAPC JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	TAPC JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC JTAG Serial Data Out	Not Muxed	JTG_TDO
JTG_TMS	TAPC JTAG Mode Select	Not Muxed	JTG_TMS
$\overline{\text{JTG\_TRST}}$	TAPC JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LP0_ACK	LP0 Acknowledge	D	PD_11
LP0_CLK	LP0 Clock	D	PD_10
LP0_D0	LP0 Data 0	D	PD_02
LP0_D1	LP0 Data 1	D	PD_03
LP0_D2	LP0 Data 2	D	PD_04
LP0_D3	LP0 Data 3	D	PD_05
LP0_D4	LP0 Data 4	D	PD_06
LP0_D5	LP0 Data 5	D	PD_07
LP0_D6	LP0 Data 6	D	PD_08

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D00	EPPI0 Data 0	E	PE_12
PPI0_D01	EPPI0 Data 1	E	PE_11
PPI0_D02	EPPI0 Data 2	E	PE_10
PPI0_D03	EPPI0 Data 3	E	PE_09
PPI0_D04	EPPI0 Data 4	E	PE_08
PPI0_D05	EPPI0 Data 5	E	PE_07
PPI0_D06	EPPI0 Data 6	E	PE_06
PPI0_D07	EPPI0 Data 7	E	PE_05
PPI0_D08	EPPI0 Data 8	E	PE_04
PPI0_D09	EPPI0 Data 9	E	PE_00
PPI0_D10	EPPI0 Data 10	D	PD_15
PPI0_D11	EPPI0 Data 11	D	PD_14
PPI0_D12	EPPI0 Data 12	B	PB_04
PPI0_D13	EPPI0 Data 13	B	PB_05
PPI0_D14	EPPI0 Data 14	B	PB_00
PPI0_D15	EPPI0 Data 15	B	PB_01
PPI0_D16	EPPI0 Data 16	B	PB_02
PPI0_D17	EPPI0 Data 17	B	PB_03
PPI0_D18	EPPI0 Data 18	D	PD_13
PPI0_D19	EPPI0 Data 19	D	PD_12
PPI0_D20	EPPI0 Data 20	E	PE_13
PPI0_D21	EPPI0 Data 21	E	PE_14
PPI0_D22	EPPI0 Data 22	E	PE_15
PPI0_D23	EPPI0 Data 23	D	PD_00
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_02
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_01
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_15
PWM0_AH	PWM0 Channel A High Side	B	PB_07
PWM0_AL	PWM0 Channel A Low Side	B	PB_08
PWM0_BH	PWM0 Channel B High Side	B	PB_06
PWM0_BL	PWM0 Channel B Low Side	C	PC_00
PWM0_CH	PWM0 Channel C High Side	B	PB_13
PWM0_CL	PWM0 Channel C Low Side	B	PB_14
PWM0_DH	PWM0 Channel D High Side	B	PB_11
PWM0_DL	PWM0 Channel D Low Side	B	PB_12
PWM0_SYNC	PWM0 PWMTMR Grouped	E	PE_09
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	B	PB_15
PWM1_AH	PWM1 Channel A High Side	D	PD_03
PWM1_AL	PWM1 Channel A Low Side	D	PD_04
PWM1_BH	PWM1 Channel B High Side	D	PD_05
PWM1_BL	PWM1 Channel B Low Side	D	PD_06
PWM1_CH	PWM1 Channel C High Side	D	PD_07
PWM1_CL	PWM1 Channel C Low Side	D	PD_08
PWM1_DH	PWM1 Channel D High Side	D	PD_09
PWM1_DL	PWM1 Channel D Low Side	D	PD_10
PWM1_SYNC	PWM1 PWMTMR Grouped	D	PD_11
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	D	PD_02
PWM2_AH	PWM2 Channel A High Side	F	PF_07

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 15 | EMAC0 PTP Pulse-Per-Second Output 2 | SINC0 Data 1 | SMC0 Address 9 Notes: No notes
PB_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 0 | EMAC0 PTP Pulse-Per-Second Output 1 | EPPI0 Data 14 | SINC0 Data 2 | SMC0 Address 8 | TIMER0 Alternate Clock 3 Notes: No notes
PB_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 1 | EMAC0 PTP Pulse-Per-Second Output 0 | EPPI0 Data 15 | SINC0 Clock 0 | SMC0 Address 7 | TIMER0 Alternate Clock 4 Notes: No notes
PB_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 2 | EMAC0 PTP Clock Input 0 | EPPI0 Data 16 | SMC0 Address 4 | UART1 Transmit Notes: No notes
PB_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 3 | EMAC0 PTP Auxiliary Trigger Input 0 | EPPI0 Data 17 | SMC0 Address 3 | UART1 Receive | TIMER0 Alternate Capture Input 1 Notes: No notes
PB_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 4 | EPPI0 Data 12 | MLB0 Single-Ended Clock | SINC0 Data 3 | SMC0 Asynchronous Ready | EMAC0 PTP Auxiliary Trigger Input 1 Notes: No notes
PB_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 5 | EPPI0 Data 13 | MLB0 Single-Ended Signal | SMC0 Address 1 | EMAC0 PTP Auxiliary Trigger Input 2 Notes: No notes
PB_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 6 | MLB0 Single-Ended Data | PWM0 Channel B High Side | SMC0 Address 2 | EMAC0 PTP Auxiliary Trigger Input 3 Notes: No notes
PB_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 7 | LP1 Data 0 | PWM0 Channel A High Side | SMC0 Data 15 | TIMER0 Timer 3 Notes: No notes
PB_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 8 | LP1 Data 1 | PWM0 Channel A Low Side | SMC0 Data 14 | TIMER0 Timer 4 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 12 | EPPI0 Data 0 | SMC0 Data 0 | SPI1 Slave Select Output 4 | SPI2 Ready Notes: No notes
PE_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 13 | EPPI0 Data 20 | SMC0 Memory Select 1 | SPI1 Clock Notes: No notes
PE_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 14 | EPPI0 Data 21 | SMC0 Byte Enable 0 | SPI1 Master In, Slave Out Notes: No notes
PE_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 15 | EPPI0 Data 22 | SMC0 Byte Enable 1 | SPI1 Master Out, Slave In Notes: No notes
PF_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 0 | SPI1 Slave Select Output 6 | TIMER0 Timer 6 Notes: No notes
PF_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 1 | SPI1 Slave Select Output 7 | TIMER0 Timer 7 Notes: No notes
PF_02	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 2 | HADC0 End of Conversion / Serial Data Out | MSI0 Data 0 Notes: No notes
PF_03	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 3 | HADC0 Controls to external multiplexer | MSI0 Data 1 Notes: No notes
PF_04	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 4 | HADC0 Controls to external multiplexer | MSI0 Data 2 Notes: No notes
PF_05	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 5 | HADC0 Controls to external multiplexer | MSI0 Data 3 Notes: No notes
PF_06	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 6 | MSI0 Data 4 | PWM2 Channel A Low Side Notes: No notes
PF_07	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 7 | MSI0 Data 5 | PWM2 Channel A High Side Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
USB_XTAL	a		none	none	none		Desc: USB0/USB1 Crystal Notes: Services both USB0 and USB1
VDD_DMC	s	NA	none	none	none		Desc: DMC VDD Notes: No notes
VDD_EXT	s	NA	none	none	none		Desc: External Voltage Domain Notes: No notes
VDD_HADC	s	NA	none	none	none		Desc: HADC VDD Notes: No notes
VDD_INT	s	NA	none	none	none		Desc: Internal Voltage Domain Notes: No notes
VDD_PCIE	s	NA	none	none	none		Desc: PCIE Supply Voltage Notes: Connect to GND if not used[1]
VDD_PCIE_RX	s	NA	none	none	none		Desc: PCIE RX Supply Voltage Notes: Connect to GND if not used[1]
VDD_PCIE_TX	s	NA	none	none	none		Desc: PCIE TX Supply Voltage Notes: Connect to GND if not used[1]
VDD_RTC	s	NA	none	none	none		Desc: RTC VDD Notes: No notes
VDD_USB	s	NA	none	none	none		Desc: USB VDD Notes: Connect to VDD_EXT when USB is not used

[1] Guidance also applies to models that do not feature the associated hardware block. See Table 2 or Table 3 for further information.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.1	1.15	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_RTC}	RTC Voltage		2.0	3.3	3.60	V
$V_{DD\_PCIE\_TX}$	PCIe Core Transmit Voltage		1.05	1.1	1.15	V
$V_{DD\_PCIE\_RX}$	PCIe Core Receive Voltage		1.05	1.1	1.15	V
V_{DD_PCIE}	PCIe Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = maximum	2.0			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.8	V
$V_{IL\_DDR2/3}$[5]	Low Level Input Voltage	V_{DD_DMC} = minimum			V_{REF} – 0.25	V
$V_{IH\_DDR2/3}$[5]	High Level Input Voltage	V_{DD_DMC} = maximum	V_{REF} + 0.25			V
V_{IL_LPDDR}[6]	Low Level Input Voltage	V_{DD_DMC} = minimum			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[6]	High Level Input Voltage	V_{DD_DMC} = maximum	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		100	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+110	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +95°C	–40		+125	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		110	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+125	°C
AUTOMOTIVE USE ONLY						
T_J	Junction Temperature 349-Lead CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ –40°C to +105°C	–40		+133[7]	°C

[1] Applies to DDR2/DDR3/LPDDR signals.
[2] If not used, V_{DD_USB} must be connected to 3.3V.
[3] V_{HADC_VREF} must always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional pins except the TWI, DMC, USB, PCIe, and MLB pins.
[5] This parameter applies to all DMC0/1 signals in DDR2/DDR3 mode. V_{REF} is the voltage applied to the V_{REF_DMC} pin, nominally $V_{DD\_DMC/2}$.
[6] This parameter applies to DMC0/1 signals in LPDDR mode.
[7] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Table 28. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_VSEL Selections	V_{DD_EXT} Nominal	V_{BUSTWI}			Unit
		Min	Nominal	Max	
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC1\_DYN} + I_{DD\_INT\_CCLK\_SHARC2\_DYN} + I_{DD\_INT\_CCLK\_A5\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_USB\_DYN} + I_{DD\_INT\_MLB\_DYN} + I_{DD\_INT\_GIGE\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN} + I_{DD\_INT\_PCIE\_DYN}$$

$I_{DD\_INT\_STATIC}$ is the sole contributor to the static power dissipation component and is specified as a function of voltage (V_{DD_INT}) and junction temperature (T_J) in Table 31.

Table 31. Static Current—$I_{DD\_INT\_STATIC}$ (mA)

	Voltage (V_{DD_INT})		
T_J (°C)	**1.05**	**1.10**	**1.15**
–40	7	8	10
–20	12	14	17
–10	16	19	23
0	21	25	30
10	28	33	39
25	42	49	58
40	63	73	84
55	92	106	122
70	133	152	175
85	190	216	247
100	269	305	346
105	302	342	387
115	376	425	480
125	466	525	592
133	552	621	700

The other 14 addends in the $I_{DD\_INT\_TOT}$ equation comprise the dynamic power dissipation component and fall into four broad categories: application-dependent currents, clock currents, currents from high-speed peripheral operation, and data transmission currents.

Application Dependent Current

The application dependent currents include the dynamic current in the core clock domain of the two SHARC+ cores and the ARM Cortex-A5 core, as well as the dynamic current in the accelerator block.

Dynamic current consumed by the core is subject to an activity scaling factor (ASF) that represents application code running on the processor cores (see Table 32 and Table 33). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent dynamic current data in Table 34 and Table 35, respectively, to calculate this portion of the total dynamic power dissipation component.

$I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ = Table 34 × ASF_{SHARC1}
$I_{DD\_INT\_CCLK\_SHARC2\_DYN}$ = Table 34 × ASF_{SHARC2}
$I_{DD\_INT\_CCLK\_A5\_DYN}$ = Table 35 × ASF_{A5}

Table 32. Activity Scaling Factors for the SHARC+ Core1 and Core2 (ASF_{SHARC1} and ASF_{SHARC2})

I_{DD_INT} Power Vector	**ASF**
$I_{DD\text{-}IDLE}$	0.31
$I_{DD\text{-}NOP}$	0.53
$I_{DD\text{-}TYP\_3070}$	0.74
$I_{DD\text{-}TYP\_5050}$	0.87
$I_{DD\text{-}TYP\_7030}$	1.00
$I_{DD\text{-}PEAK\_100}$	1.14

Table 33. Activity Scaling Factors for the ARM Cortex-A5 Core (ASF_{A5})

I_{DD_INT} Power Vector	**ASF**
$I_{DD\text{-}IDLE}$	0.29
$I_{DD\text{-}DHRYSTONE}$	0.73
$I_{DD\text{-}TYP\_2575}$	0.57
$I_{DD\text{-}TYP\_5050}$	0.80
$I_{DD\text{-}TYP\_7525}$	1.00
$I_{DD\text{-}PEAK\_100}$	1.21

Asynchronous Read

Table 45 and Figure 12 show asynchronous memory read timing, related to the SMC.

Table 45. Asynchronous Read

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	5.1		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0.7		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
t_{AMSARE}	ADDR/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK0} – 2		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	(RST + PREAT) × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	RHT × t_{SCLK0} –2		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	RAT × t_{SCLK0} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$, $\overline{SMC0\_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

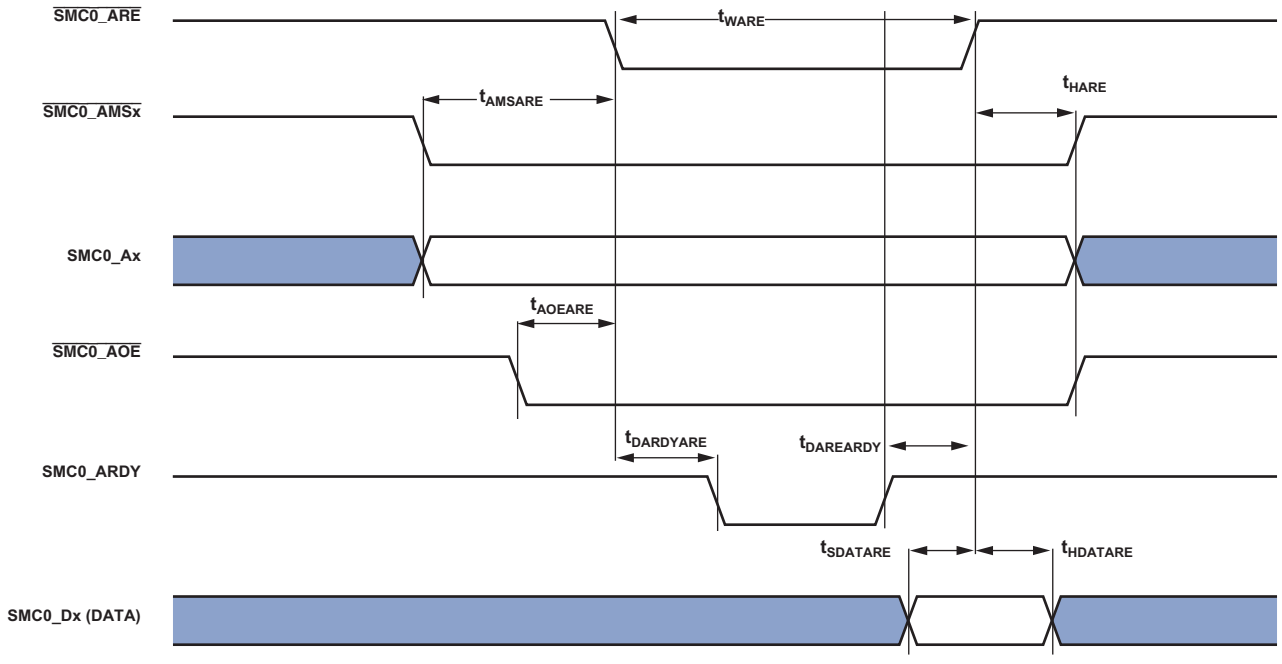


Figure 12. Asynchronous Read

Asynchronous Flash Read

Table 46 and Figure 13 show asynchronous flash memory read timing, related to the SMC.

Table 46. Asynchronous Flash Read

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before SMC0_NORDV Low[1]	PREST × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From SMC0_NORDV High[3]	PREAT × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$, $\overline{\text{SMC0\_AOE}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

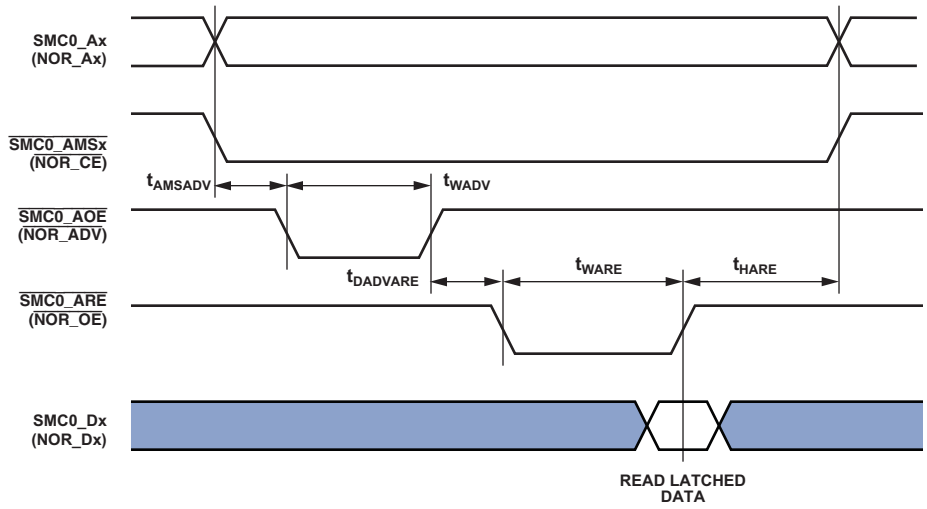


Figure 13. Asynchronous Flash Read

DDR2 SDRAM Clock and Control Cycle Timing

Table 51 and Figure 17 show DDR2 SDRAM clock and control cycle timing, related to the DMC.

Table 51. DDR2 SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		400 MHz[2] Min	400 MHz[2] Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.5		ns
$t_{CH\ (abs)}$[3]	Minimum Clock Pulse Width	0.44	0.56	t_{CK}
$t_{CL\ (abs)}$[3]	Maximum Clock Pulse Width	0.44	0.56	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	175		ps
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	250		ps

[1] Specifications apply to both DMC0 and DMC1.
[2] In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-2E definition.

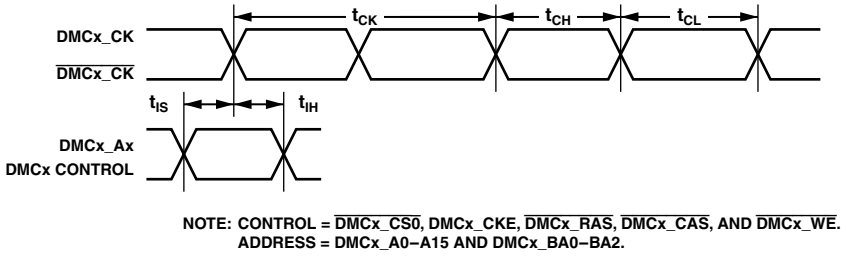


Figure 17. DDR2 SDRAM Clock and Control Cycle Timing

DDR2 SDRAM Read Cycle Timing

Table 52 and Figure 18 show DDR2 SDRAM read cycle timing, related to the DMC.

Table 52. DDR2 SDRAM Read Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		400 MHz[2] Min	400 MHz[2] Max	Unit
Timing Requirements				
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQxx Signals		0.2	ns
t_{QH}	DMCx_DQxx, DMCx_DQS Output Hold Time From DMCx_DQS	0.9		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

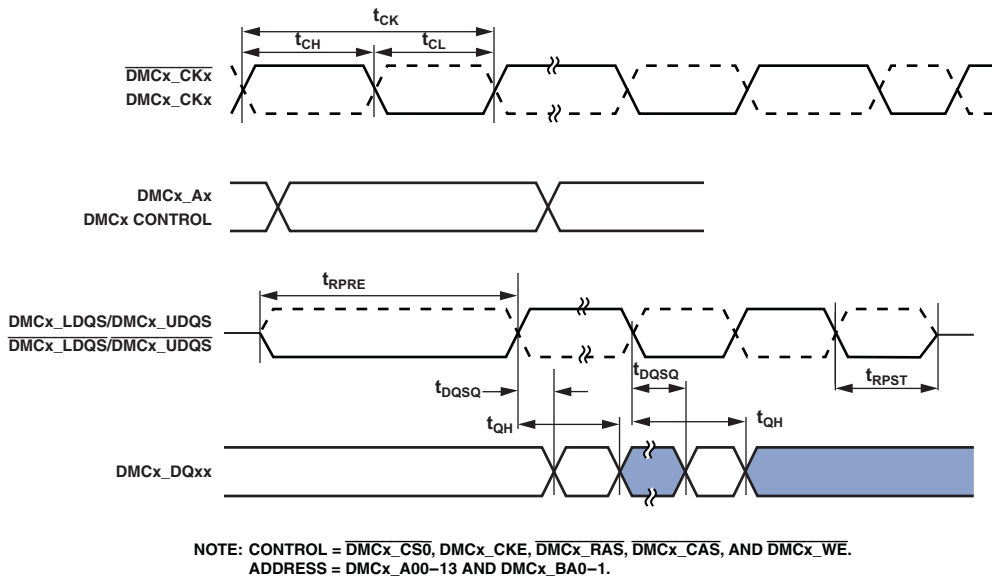


Figure 18. DDR2 SDRAM Controller Input AC Timing

DDR3 SDRAM Clock and Control Cycle Timing

Table 57 and Figure 23 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 57. DDR3 SDRAM Clock and Control Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[3]	Minimum Clock Pulse Width	0.43	0.57	t_{CK}
$t_{CL(abs)}$[3]	Maximum Clock Pulse Width	0.43	0.57	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	0.275		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-3F definition.

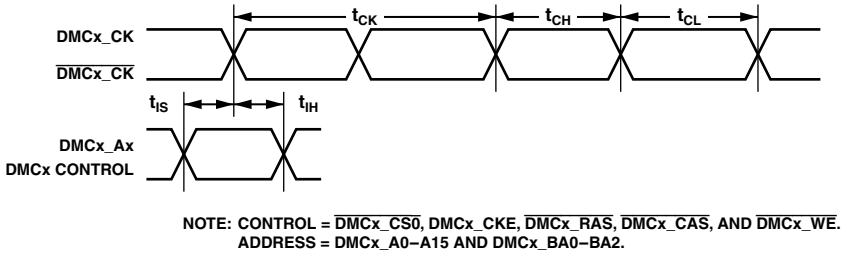


Figure 23. DDR3 SDRAM Clock and Control Cycle Timing

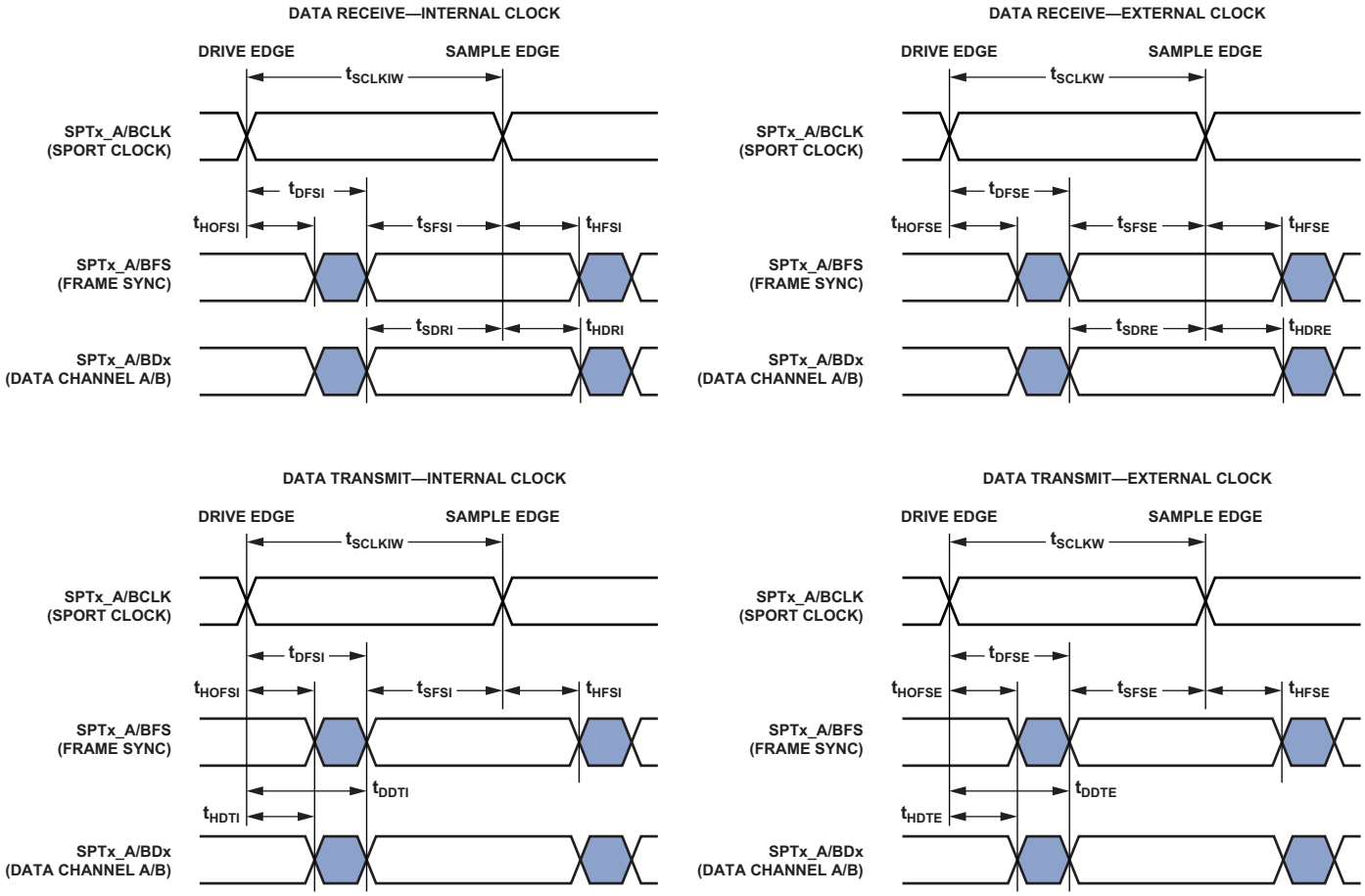


Figure 37. Serial Ports

Pulse Width Modulator (PWM) Timing

Table 83 and Figure 55 describe timing, related to the PWM.

Table 83. PWM Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{ES}	External Sync Pulse Width	$2 \times t_{SCLK0}$		ns
Switching Characteristics				
t_{DODIS}	Output Inactive (off) After Trip Input[2]		15	ns
t_{DOE}	Output Delay After External Sync[2, 3]	$2 \times t_{SCLK0} + 5.5$	$5 \times t_{SCLK0} + 14$	ns

[1] All specifications apply to all three PWMs.
[2] PWM outputs are PWMx_AH, PWMx_AL, PWMx_BH, PWMx_BL, PWMx_CH, and PWMx_CL.
[3] When the external sync signal is synchronous to the peripheral clock, it takes fewer clock cycles for the output to appear compared to when the external sync signal is asynchronous to the peripheral clock.

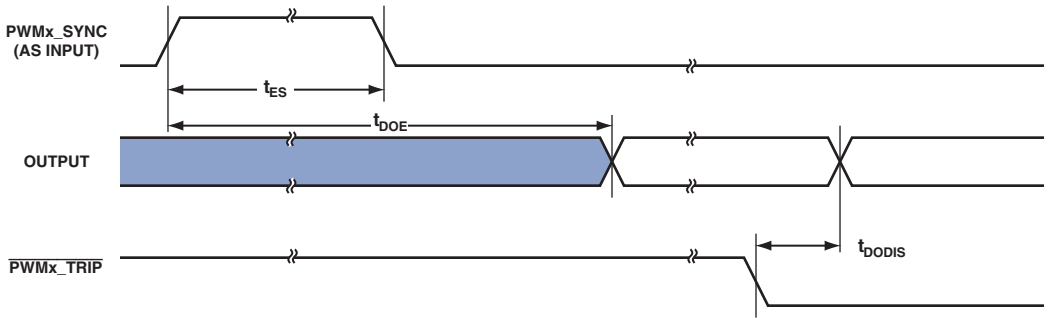


Figure 55. PWM Timing

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 96. Input signals are routed to the DAIx_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAIx_PINx pins.

Table 96. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

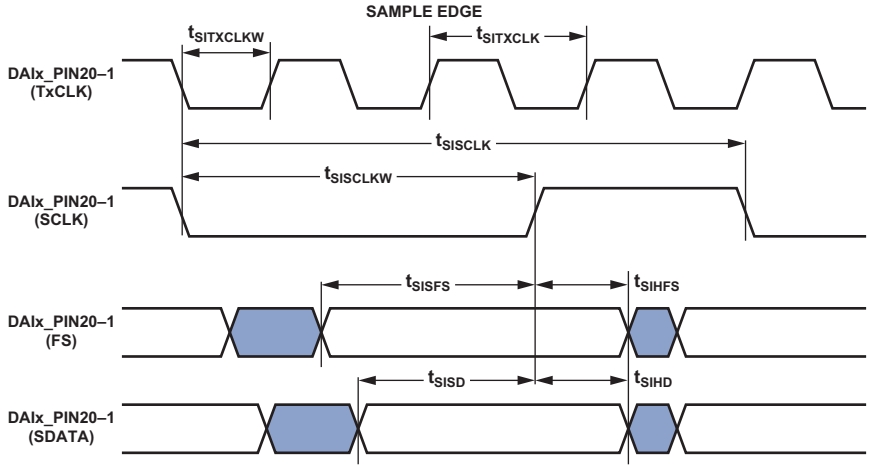


Figure 67. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 97. Oversampling Clock (TxCLK) Switching Characteristics

Parameter		Max	Unit
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

ADSP-SC58x/ADSP-2158x 529-BALL BGA BALL ASSIGNMENTS

The ADSP-SC58x/ADSP-2158x 529-Ball BGA Ball Assignments (Numerical by Ball Number) table lists the 529-ball BGA package by ball number.

The ADSP-SC58x/ADSP-2158x 529-Ball BGA Ball Assignments (Alphabetical by Pin Name) table lists the 529-ball BGA package by pin name.

ADSP-SC58x/ADSP-2158x 529-BALL BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	B19	DMC1_DQ11	D14	DMC1_BA2	F09	GND
A02	DMC0_UDQS	B20	DMC1_DQ12	D15	DMC1_CAS	F10	VDD_INT
A03	DMC0_CK	B21	DMC1_DQ14	D16	DMC1_RAS	F11	VDD_INT
A04	DMC0_CK	B22	PD_00	D17	DMC1_A09	F12	VDD_INT
A05	DMC0_DQ09	B23	PD_04	D18	DMC1_A15	F13	VDD_INT
A06	DMC0_LDQS	C01	DMC0_DQ14	D19	DMC1_A10	F14	VDD_INT
A07	DMC0_LDQS	C02	DMC0_DQ13	D20	DMC1_A11	F15	VDD_INT
A08	DMC0_DQ05	C03	DMC0_CS0	D21	PC_14	F16	GND
A09	DMC0_DQ03	C04	DMC0_CKE	D22	PD_10	F17	VDD_INT
A10	DMC0_DQ01	C05	DMC0_LDM	D23	PD_09	F18	VDD_INT
A11	DMC1_DQ03	C06	DMC1_RESET	E01	DMC0_A04	F19	VDD_INT
A12	DMC1_DQ00	C07	DMC1_A03	E02	DMC0_RAS	F20	PE_06
A13	DMC1_LDQS	C08	DMC1_A00	E03	DMC0_BA1	F21	PD_02
A14	DMC1_LDQS	C09	DMC1_A01	E04	DMC0_WE	F22	PD_13
A15	DMC1_VREF	C10	DMC1_A04	E05	DMC0_RZQ	F23	PD_12
A16	DMC1_CK	C11	DMC1_A06	E06	GND	G01	DMC0_A13
A17	DMC1_CK	C12	DMC1_BA1	E07	GND	G02	DMC0_A09
A18	DMC1_DQ09	C13	DMC1_ODT	E08	GND	G03	DMC0_A03
A19	DMC1_UDQS	C14	DMC1_CS0	E09	GND	G04	DMC0_A11
A20	DMC1_UDQS	C15	DMC1_LDM	E10	VDD_INT	G05	VDD_INT
A21	DMC1_DQ13	C16	DMC1_UDM	E11	VDD_INT	G06	VDD_DMC
A22	DMC1_DQ15	C17	DMC1_A14	E12	VDD_INT	G07	VDD_DMC
A23	GND	C18	DMC1_A12	E13	VDD_INT	G08	VDD_DMC
B01	DMC0_UDQS	C19	DMC1_A13	E14	VDD_INT	G09	VDD_DMC
B02	DMC0_DQ12	C20	PC_13	E15	VDD_INT	G10	VDD_DMC
B03	DMC0_DQ11	C21	PD_01	E16	VDD_INT	G11	VDD_DMC
B04	DMC0_DQ10	C22	PD_06	E17	VDD_INT	G12	VDD_DMC
B05	DMC0_DQ08	C23	PD_05	E18	VDD_INT	G13	VDD_DMC
B06	DMC0_DQ06	D01	DMC0_VREF	E19	DMC1_RZQ	G14	VDD_DMC
B07	DMC0_DQ07	D02	DMC0_DQ15	E20	PC_15	G15	VDD_DMC
B08	DMC0_DQ04	D03	DMC0_BA0	E21	PD_08	G16	VDD_DMC
B09	DMC0_DQ02	D04	DMC0_BA2	E22	PD_14	G17	VDD_DMC
B10	DMC0_DQ00	D05	DMC0_ODT	E23	PD_11	G18	VDD_DMC
B11	DMC1_DQ01	D06	DMC0_UDM	F01	DMC0_A01	G19	VDD_INT
B12	DMC1_DQ02	D07	DMC1_A05	F02	DMC0_A06	G20	PE_04
B13	DMC1_DQ04	D08	DMC1_WE	F03	DMC0_CAS	G21	PE_13
B14	DMC1_DQ05	D09	DMC1_A07	F04	DMC0_A02	G22	PE_01
B15	DMC1_DQ06	D10	DMC1_A02	F05	DMC0_A07	G23	PE_00
B16	DMC1_DQ07	D11	DMC1_BA0	F06	GND	H01	DMC0_A14
B17	DMC1_DQ08	D12	DMC1_A08	F07	VDD_INT	H02	DMC0_A12
B18	DMC1_DQ10	D13	DMC1_CKE	F08	VDD_INT	H03	DMC0_A05

CONFIGURATION OF THE 529-BALL CSP_BGA

Figure 99 shows an overview of signal placement on the 529-ball CSP_BGA.

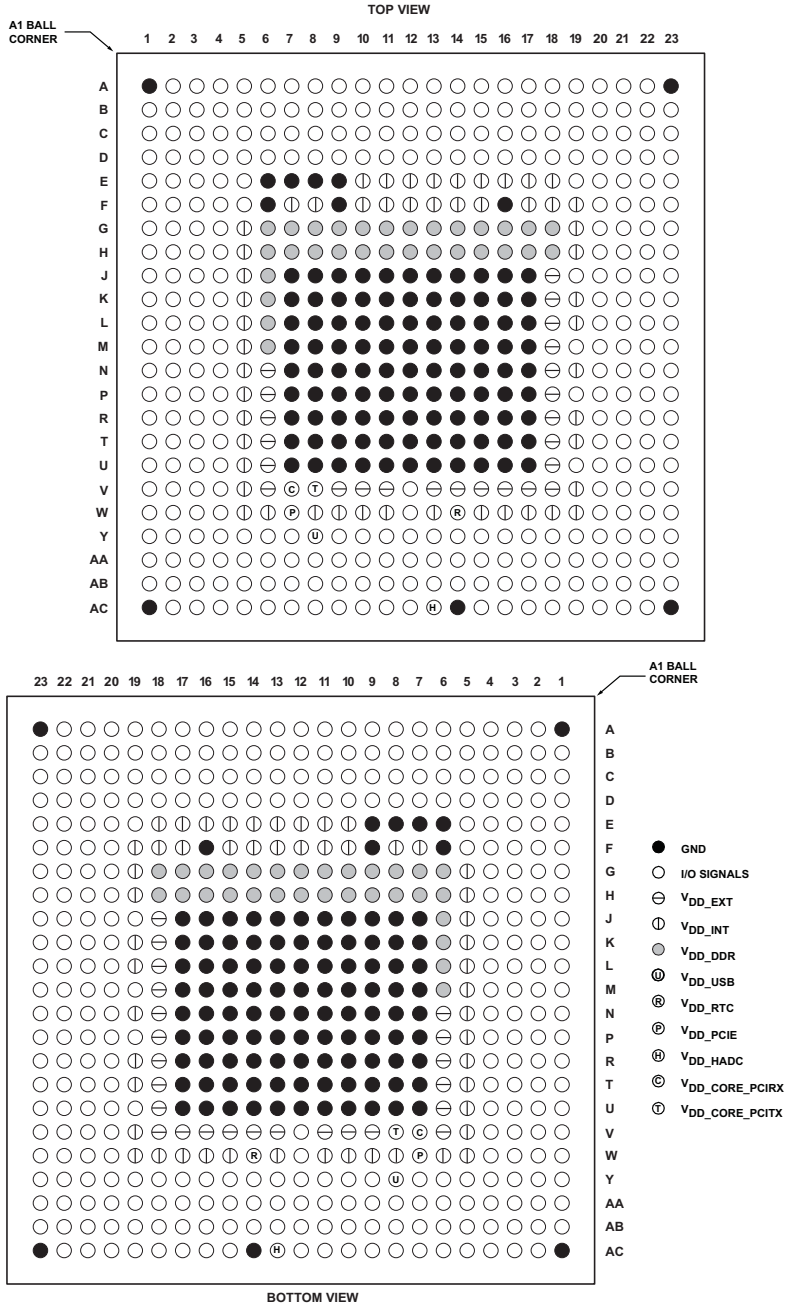


Figure 99. 529-Ball CSP_BGA Configuration