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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	896kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	529-LFBGA, CSPBGA
Supplier Device Package	529-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21587bbcz-4b

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REVISION HISTORY

10/2016—Revision 0: Initial Version

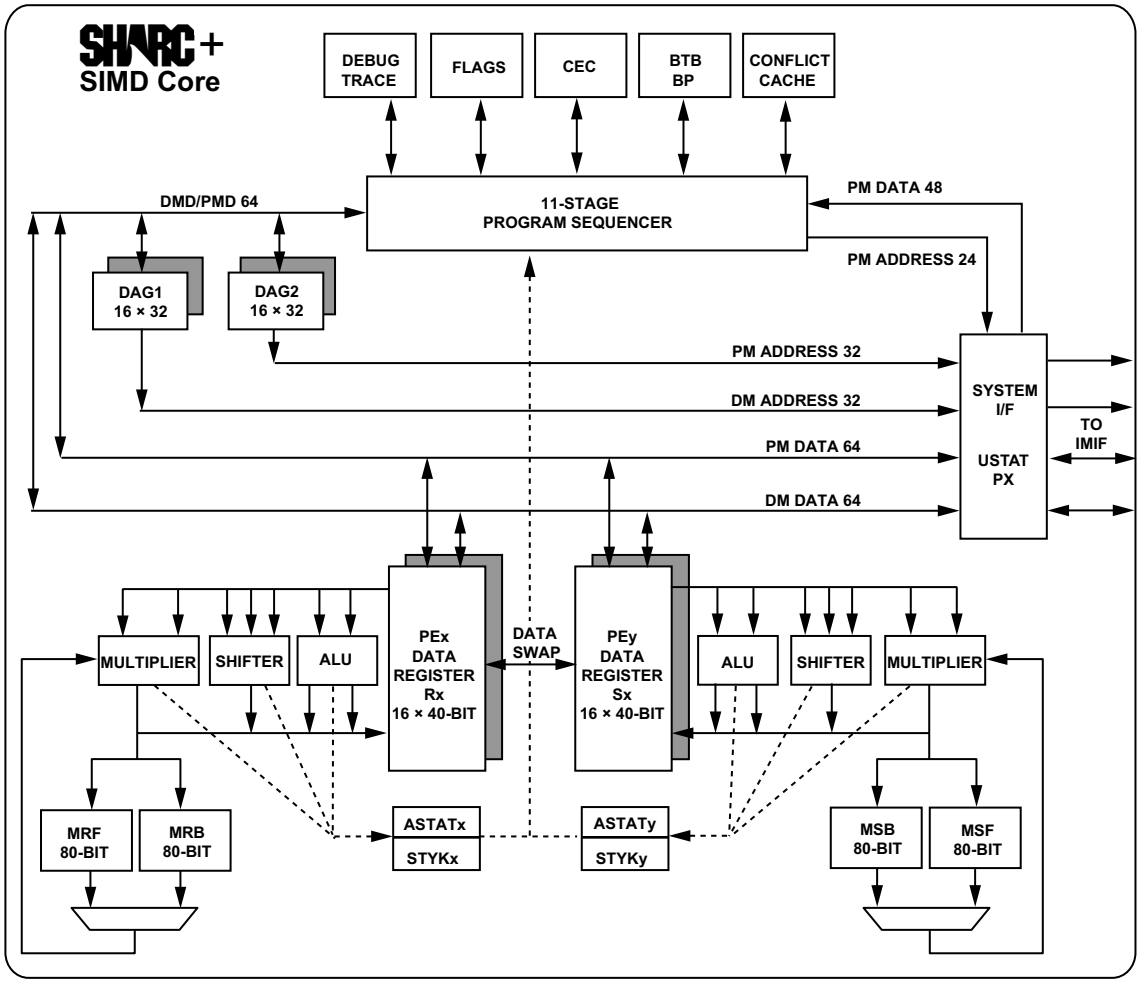


Figure 4. SHARC+ SIMD Core Block Diagram

L1 Memory

Figure 5 shows the ADSP-SC58x/ADSP-2158x memory map. Each SHARC+ core has a tightly coupled L1 SRAM of up to 5 Mb. Each SHARC+ core can access code and data in a single cycle from this memory space. The ARM Cortex-A5 core can also access this memory space with multicycle accesses.

In the SHARC+ core private address space, both cores have L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x 0000 0000 through 0x 0003 FFFF in Normal Word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1024 Kb can be configured for data memory (DM), program memory (PM), and instruction cache. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the DMA engine in a single cycle. The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 Kb DM, 128 Kb PM, and 128 Kb of instruction cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

Single-Cycle Fetch of Instructional Four Operands

The ADSP-SC58x/ADSP-2158x processors feature an enhanced Harvard architecture in which the DM bus transfers data and PM bus transfers both instructions and data.

With the separate program memory bus, data memory buses, and on-chip instruction conflict-cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction from the conflict cache, in a single cycle.

Core Event Controller (CEC)

The SHARC+ core generates various core interrupts (including arithmetic and circular buffer instruction flow exceptions) and SEC events (debug/monitor and software). The core only responds to unmasked interrupts (enabled in the IMASK register).

Instruction Conflict-Cache

The processors include a 32-entry instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions that require fetches conflict with the PM bus data accesses cache. This cache allows full speed execution of core, looped operations, such as digital filter multiply accumulates, and fast Fourier transforms (FFT) butterfly processing. The conflict cache serves for on-chip bus conflicts only.

Branch Target Buffer/Branch Predictor

Implementation of a hardware-based branch predictor (BP) and branch target buffer (BTB) reduce branch delay. The program sequencer supports efficient branching using the BTB for conditional and unconditional instructions.

Addressing Spaces

In addition to traditionally supported long word, normal word, extended precision word and short word addressing aliases, the processors support byte addressing for the data and instruction accesses. The enhanced ISA/VISA provides new instructions for accessing all sizes of data from byte space as well as converting word addresses to byte and byte to word addresses.

Additional Features

The enhanced ISA/VISA of the ADSP-SC58x/ADSP-2158x processors also provides a memory barrier instruction for data synchronization, exclusive data access support for multicore data sharing, and exclusive data access to enable multiprocessor programming. To enhance the reliability of the application, L1 data RAMs support parity error detection logic for every byte. Additionally, the processors detect illegal opcodes. Core interrupts flag both errors. Master ports of the core also detect for failed external accesses.

SYSTEM INFRASTRUCTURE

The following sections describe the system infrastructure of the ADSP-SC58x/ADSP-2158x processors.

System L2 Memory

A system L2 SRAM memory of 2 Mb (256 kB) and two ROM memories, each 2 Mb (256 kB), are available to both SHARC+ cores, the ARM Cortex-A5 core, and the system DMA channels (see Table 5). All L2 SRAM/ROM blocks are subdivided into eight banks to support concurrent access to the L2 memory ports. Memory accesses to the L2 memory space are multicycle accesses by both the ARM Cortex-A5 and SHARC+ cores.

The memory space is used for various cases including:

- ARM Cortex-A5 to SHARC+ core data sharing and inter-core communications
- Accelerator and peripheral sources and destination memory to avoid accessing data in the external memory
- A location for DMA descriptors
- Storage for additional data for either the ARM Cortex-A5 or SHARC+ cores to avoid external memory latencies and reduce external memory bandwidth
- Storage for incoming Ethernet traffic to improve performance
- Storage for data coefficient tables cached by the SHARC+ core

See the System Memory Protection Unit (SMPU) section for options in limiting access by specific cores and DMA masters.

The ARM Cortex-A5 core has an L1 instruction and data cache, each of which is 32 kB in size. The core also has an L2 cache controller of 256 kB. When enabling the caches, accesses to all other memory spaces (internal and external) go through the cache.

SHARC+ Core L1 Memory in Multiprocessor Space

The ARM Cortex-A5 core can access the L1 memory of the SHARC+ core. See Table 6 for the L1 memory address in multiprocessor space. The SHARC+ core can access the L1 memory of the other SHARC+ core in the multiprocessor space.

One Time Programmable Memory (OTP)

The processors feature 7 Kb of one time programmable (OTP) memory which is memory-map accessible. This memory stores a unique chip identification and supports secure boot and secure operation.

I/O Memory Space

The static memory controller (SMC) is programmed to control up to two blocks of external memories or memory-mapped devices, with flexible timing parameters. Each block occupies an 8 Kb segment regardless of the size of the device used. Mapped I/Os also include PCIe data and SPI2 memory address space (see Table 7).

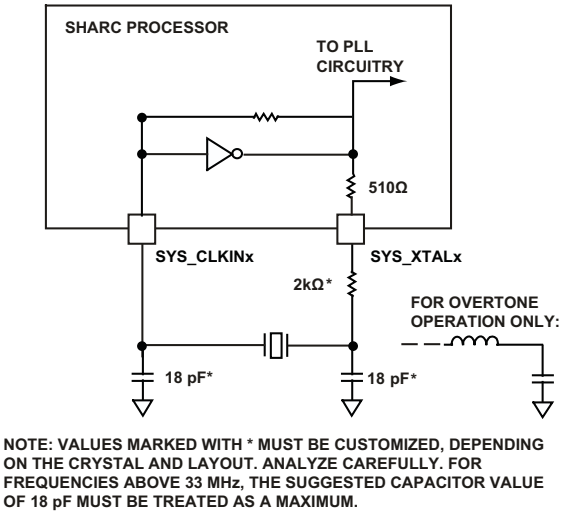


Figure 7. External Crystal Connection

A third overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit, shown in Figure 7. A design procedure for the third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168). The same recommendations can be used for the USB crystal oscillator.

Clock Distribution Unit (CDU)

The two CGUs each provide outputs which feed a clock distribution unit (CDU). The clock outputs CLKO0–CLKO9 are connected to various targets. For more information, refer to the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.

Power-Up

SYS_XTALx oscillations (SYS_CLKINx) start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ starts on-chip PLL locking (PLL lock counter). The deassertion must apply only if all voltage supplies and SYS_CLKINx oscillations are valid (refer to the Power-Up Reset Timing section).

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In master boot mode, the processors actively load data from serial memories. In slave boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 9. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

In the ADSP-SC58x processors, the ARM Cortex-A5 (Core 0) controls the boot process, including loading all internal and external memory. Likewise, in the ADSP-2158x processors, the SHARC+ (Core 1) controls the boot function. The option for secure boot is available on all models.

Table 9. Boot Modes

SYS_BMODE[n] Setting	Boot Mode
000	No boot
001	SPI2 master
010	SPI2 slave
011	Reserved
100	Reserved
101	Reserved
110	Link0 slave
111	UART0 slave

Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement which is important in applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Averaging feature available

Power Supplies

The processors have separate power supply connections for:

- Internal (VDD_INT)
- External (VDD_EXT)
- USB (VDD_USB)
- HADC (VDD_HADC)
- RTC (VDD_RTC)

Table 11. ADSP-SC58x/ADSP-2158x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SYS_FAULT	InOut	**Active-High Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_FAULT}}$	InOut	**Active-Low Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates the device is in the reset state.
SYS_XTAL0	Output	**Crystal Output.**
SYS_XTAL1	Output	**Crystal Output.**
TM_ACI[n]	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLK[n]	Input	**Alternate Clock n.** Provides an additional time base for an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for all GP timers.
TM_TMR[n]	InOut	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_D[nn]	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	InOut	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	InOut	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receives input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input.** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.
USB_DM	InOut	**Data –.** Bidirectional differential data line.
USB_DP	InOut	**Data +.** Bidirectional differential data line.
USB_ID	Input	**OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device).The input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. Can be configured as open-drain. Polarity is configurable as well.
USB_VBUS	InOut	**Bus Voltage.** Connects to bus voltage in host and device modes.
USB_XTAL	Output	**Crystal.** Drives an external crystal. Must be left unconnected if an external clock is driving USB_CLKIN.

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
VDD_PCIE	PCIE Supply Voltage	Not Muxed	VDD_PCIE
VDD_PCIE_RX	PCIE RX Supply Voltage	Not Muxed	VDD_PCIE_RX
VDD_PCIE_TX	PCIE TX Supply Voltage	Not Muxed	VDD_PCIE_TX
VDD_RTC	RTC VDD	Not Muxed	VDD_RTC
VDD_USB	USB VDD	Not Muxed	VDD_USB

ADSP-SC58X/ADSP-2158X DESIGNER QUICK REFERENCE

Table 27 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are a (analog), s (supply), g (ground) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The int term column specifies the termination present when the processor is not in the reset state.
- The reset term column specifies the termination present when the processor is in the reset state.
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 1 Notes: No notes
DAI0_PIN02	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 2 Notes: No notes
DAI0_PIN03	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 3 Notes: No notes
DAI0_PIN04	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 4 Notes: No notes
DAI0_PIN05	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 5 Notes: No notes
DAI0_PIN06	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 6 Notes: No notes
DAI0_PIN07	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 7 Notes: No notes
DAI0_PIN08	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 8 Notes: No notes
DAI0_PIN09	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 9 Notes: No notes
DAI0_PIN10	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 10 Notes: No notes
DAI0_PIN11	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 11 Notes: No notes
DAI0_PIN12	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 12 Notes: No notes
DAI0_PIN13	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 13 Notes: No notes
DAI0_PIN14	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 14 Notes: No notes
DAI0_PIN15	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 15 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC1_DQ09	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 9 Notes: No notes
DMC1_DQ10	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 10 Notes: No notes
DMC1_DQ11	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 11 Notes: No notes
DMC1_DQ12	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 12 Notes: No notes
DMC1_DQ13	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 13 Notes: No notes
DMC1_DQ14	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 14 Notes: No notes
DMC1_DQ15	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 15 Notes: No notes
DMC1_LDM	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Data Mask for Lower Byte Notes: No notes
DMC1_LDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Lower Byte Notes: External weak pull-down required in LPDDR mode
$\overline{\text{DMC1\_LDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Lower Byte (complement) Notes: No notes
DMC1_ODT	Output	B	none	none	none	VDD_DMC	Desc: DMC1 On-die termination Notes: No notes
$\overline{\text{DMC1\_RAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Row Address Strobe Notes: No notes
$\overline{\text{DMC1\_RESET}}$	InOut	B	none	none	none	VDD_DMC	Desc: DMC1 Reset (DDR3 only) Notes: No notes
DMC1_RZQ	a	B	none	none	none	VDD_DMC	Desc: DMC1 External calibration resistor connection Notes: Applicable for DDR2 and DDR3 only. External pull-down of 34 ohms need to be added.

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 15 | EMAC0 PTP Pulse-Per-Second Output 2 | SINC0 Data 1 | SMC0 Address 9 Notes: No notes
PB_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 0 | EMAC0 PTP Pulse-Per-Second Output 1 | EPPI0 Data 14 | SINC0 Data 2 | SMC0 Address 8 | TIMER0 Alternate Clock 3 Notes: No notes
PB_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 1 | EMAC0 PTP Pulse-Per-Second Output 0 | EPPI0 Data 15 | SINC0 Clock 0 | SMC0 Address 7 | TIMER0 Alternate Clock 4 Notes: No notes
PB_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 2 | EMAC0 PTP Clock Input 0 | EPPI0 Data 16 | SMC0 Address 4 | UART1 Transmit Notes: No notes
PB_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 3 | EMAC0 PTP Auxiliary Trigger Input 0 | EPPI0 Data 17 | SMC0 Address 3 | UART1 Receive | TIMER0 Alternate Capture Input 1 Notes: No notes
PB_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 4 | EPPI0 Data 12 | MLB0 Single-Ended Clock | SINC0 Data 3 | SMC0 Asynchronous Ready | EMAC0 PTP Auxiliary Trigger Input 1 Notes: No notes
PB_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 5 | EPPI0 Data 13 | MLB0 Single-Ended Signal | SMC0 Address 1 | EMAC0 PTP Auxiliary Trigger Input 2 Notes: No notes
PB_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 6 | MLB0 Single-Ended Data | PWM0 Channel B High Side | SMC0 Address 2 | EMAC0 PTP Auxiliary Trigger Input 3 Notes: No notes
PB_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 7 | LP1 Data 0 | PWM0 Channel A High Side | SMC0 Data 15 | TIMER0 Timer 3 Notes: No notes
PB_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 8 | LP1 Data 1 | PWM0 Channel A Low Side | SMC0 Data 14 | TIMER0 Timer 4 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 12 | EPPI0 Data 0 | SMC0 Data 0 | SPI1 Slave Select Output 4 | SPI2 Ready Notes: No notes
PE_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 13 | EPPI0 Data 20 | SMC0 Memory Select 1 | SPI1 Clock Notes: No notes
PE_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 14 | EPPI0 Data 21 | SMC0 Byte Enable 0 | SPI1 Master In, Slave Out Notes: No notes
PE_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 15 | EPPI0 Data 22 | SMC0 Byte Enable 1 | SPI1 Master Out, Slave In Notes: No notes
PF_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 0 | SPI1 Slave Select Output 6 | TIMER0 Timer 6 Notes: No notes
PF_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 1 | SPI1 Slave Select Output 7 | TIMER0 Timer 7 Notes: No notes
PF_02	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 2 | HADC0 End of Conversion / Serial Data Out | MSI0 Data 0 Notes: No notes
PF_03	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 3 | HADC0 Controls to external multiplexer | MSI0 Data 1 Notes: No notes
PF_04	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 4 | HADC0 Controls to external multiplexer | MSI0 Data 2 Notes: No notes
PF_05	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 5 | HADC0 Controls to external multiplexer | MSI0 Data 3 Notes: No notes
PF_06	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 6 | MSI0 Data 4 | PWM2 Channel A Low Side Notes: No notes
PF_07	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 7 | MSI0 Data 5 | PWM2 Channel A High Side Notes: No notes

Table 30. Phase-Locked Loop (PLL) Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	250	900	MHz

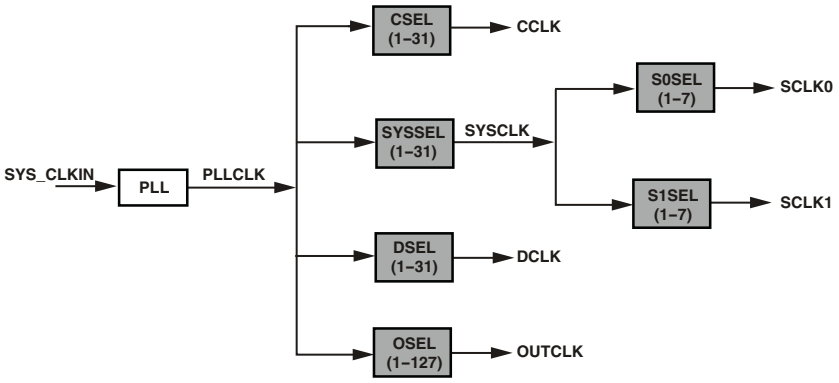


Figure 8. Clock Relationships and Divider Values

Parameter		Conditions	450 MHz Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 450 MHz ASF_{SHARC1} = 0.31 ASF_{SHARC2} = 0.31 ASF_{A5} = 0.29 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 1.1 V		495		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 450 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.73 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) FFT accelerator operating at $f_{SYSCLK/4}$ DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.1 V		1112		mA
I_{DD_INT}[11]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, PCIe, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups including JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals JTAG_TRST, USB0_VBUS, USB1_VBUS.
[9] Applies to signals PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-15, PG0-5, DAI0_PINx, DAI1_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USBx_DM, USBx_DP, and USBx_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC58x/2158x SHARC+ Processors" (EE-392) for further information.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

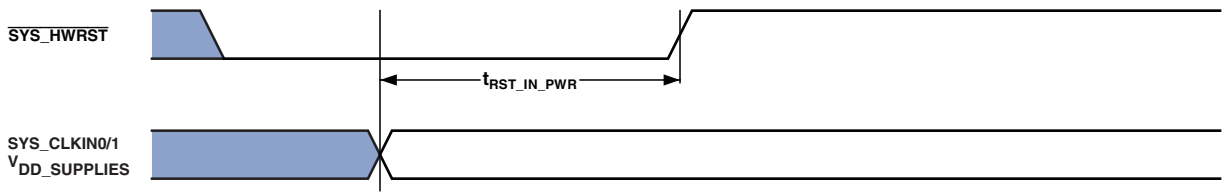
Power-Up Reset Timing

Table 43 and Figure 10 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU).

In Figure 10, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, and $V_{DD\_PCI\_CORE}$.

Table 43. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, $V_{DD\_PCI\_CORE}$) and SYS_CLKINx are Stable and Within Specification	$11 \times t_{CKIN}$		ns



NOTE: $V_{DD\_SUPPLIES}$ REFER TO V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, AND $V_{DD\_PCI\_CORE}$.

Figure 10. Power-Up Reset Timing

Mobile DDR SDRAM Write Cycle Timing

Table 56 and Figure 22 show mobile DDR SDRAM write cycle timing, related to the DMC.

Table 56. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	200 MHz[2] Max	Unit
Switching Characteristics				
t_{DQSS}[3]	DMCx_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMCx_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMCx_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMCx_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMCx_DQS Falling Edge Hold Time From DMCx_CK	0.2		t_{CK}
t_{DQSH}	DMCx_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMCx_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMCx_DQ and DMCx_DM Output Pulse Width	1.8		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] Write command to first DMCx_DQS delay = WL × t_{CK} + t_{DQSS}.

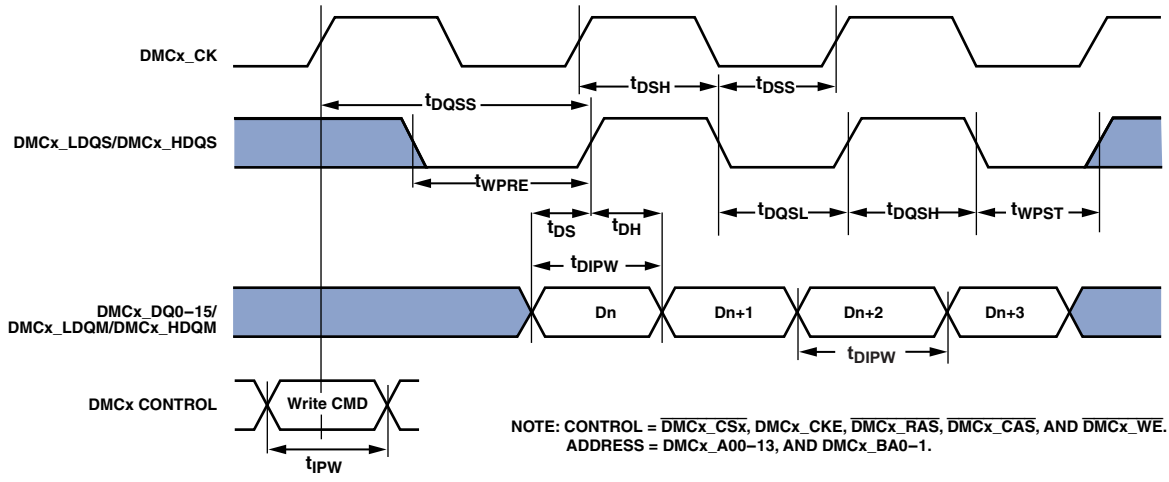


Figure 22. Mobile DDR SDRAM Controller Output AC Timing

DDR3 SDRAM Clock and Control Cycle Timing

Table 57 and Figure 23 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 57. DDR3 SDRAM Clock and Control Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[3]	Minimum Clock Pulse Width	0.43	0.57	t_{CK}
$t_{CL(abs)}$[3]	Maximum Clock Pulse Width	0.43	0.57	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	0.275		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-3F definition.

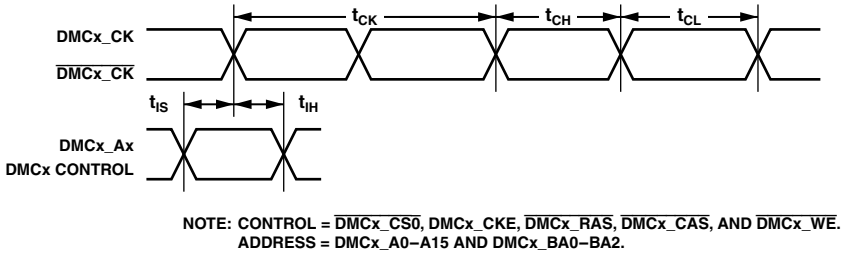


Figure 23. DDR3 SDRAM Clock and Control Cycle Timing

Table 66. Serial Ports—Enable and Three-State[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SPTx_CLK[2]	1		ns
t_{DDTTE}	Data Disable from External Transmit SPTx_CLK[2]		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPTx_CLK[2]	–2.5		ns
t_{DDTTI}	Data Disable from Internal Transmit SPTx_CLK[2]		2.8	ns

[1] Specifications apply to all eight SPORTs.
[2] Referenced to drive edge.

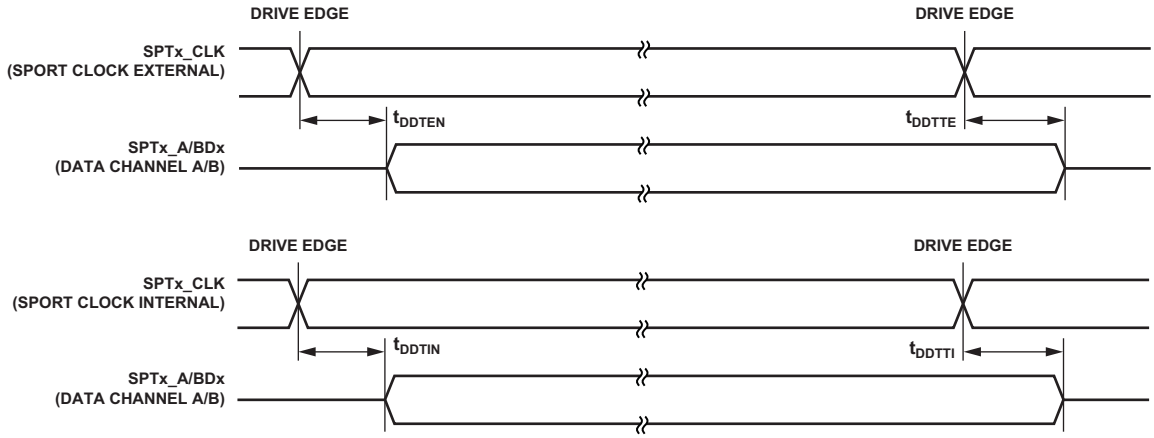


Figure 38. Serial Ports—Enable and Three-State

Sample Rate Converter—Serial Output Port

For the serial output port, the frame sync is an input and it must meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. The serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 70. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		13	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN, SCLK0, or any of the DAI pins.

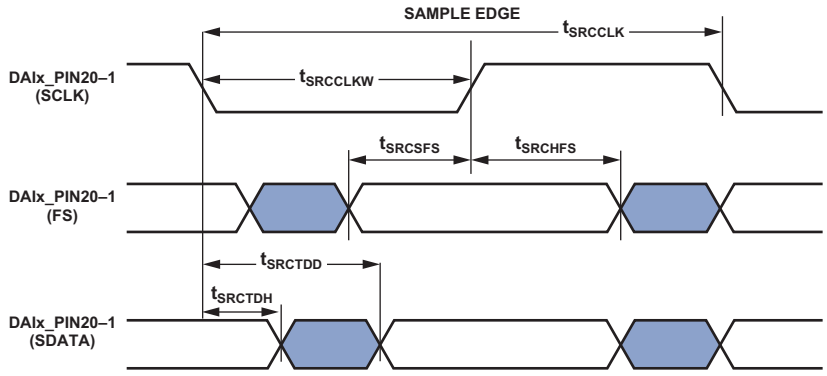


Figure 42. ASRC Serial Output Port Timing

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 76. SPI Port—SPIx_RDY Master Timing[1]

Parameter		Conditions	Min	Max	Unit
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	Baud = 0, CPHA = 0	$4.5 \times t_{SCLK1}$	$5.5 \times t_{SCLK1} + 10$	ns
		Baud = 0, CPHA = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 0	$(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 1	$(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

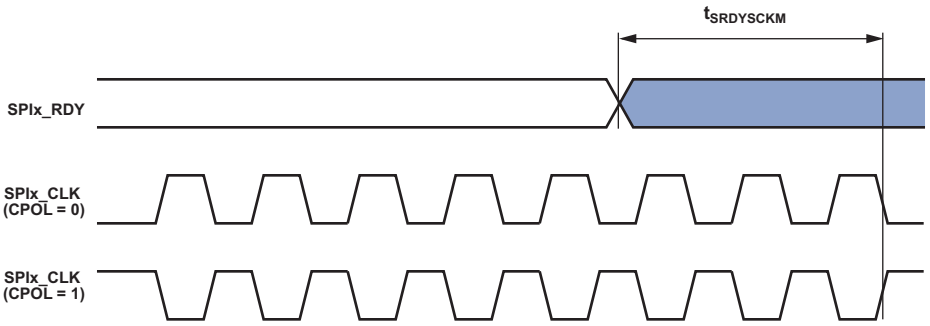


Figure 48. SPIx_RDY Setup Before SPIx_CLK

General-Purpose I/O Port Timing

Table 78 and Figure 51 describe I/O timing, related to the general-purpose I/O port (PORT).

Table 78. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

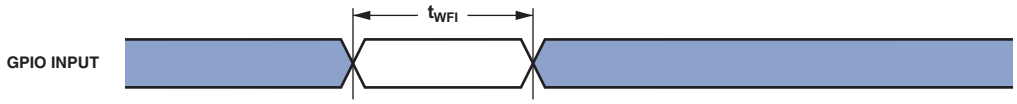


Figure 51. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 79, Table 80, and Figure 52 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of $f_{SCLK}/4$ MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 79. Timer Cycle Timing (Internal Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)[2]	$t_{SCLK} \times WIDTH - 1.5$	$t_{SCLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Table 80. Timer Cycle Timing (External Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times WIDTH - 1.5$	$t_{EXT\_CLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency see the $f_{TMRCLKEXT}$ specification in Table 29.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

OUTPUT DRIVE CURRENTS

Figure 77 through Figure 89 show typical current-voltage characteristics for the output drivers of the ADSP-SC58x and ADSP-2158x processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

Output drive currents for PCIe pins are compliant with PCIe Gen1 and Gen2 x1 lane data rate specifications. Output drive currents for MLB pins are compliant with MOST150 LVDS specifications. Output drive currents for USB pins are compliant with the USB 2.0 specifications.

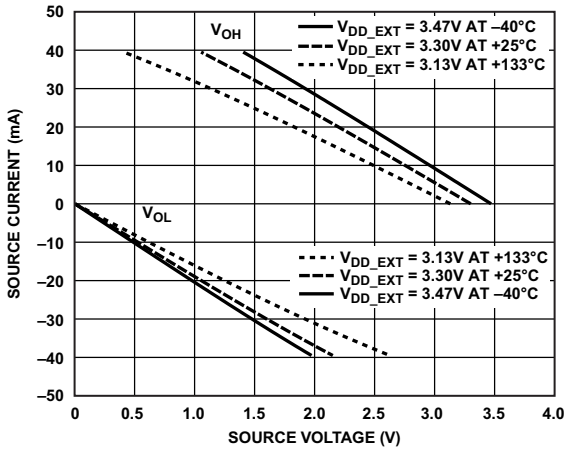


Figure 77. Driver Type A Current (3.3 V V_{DD_EXT})

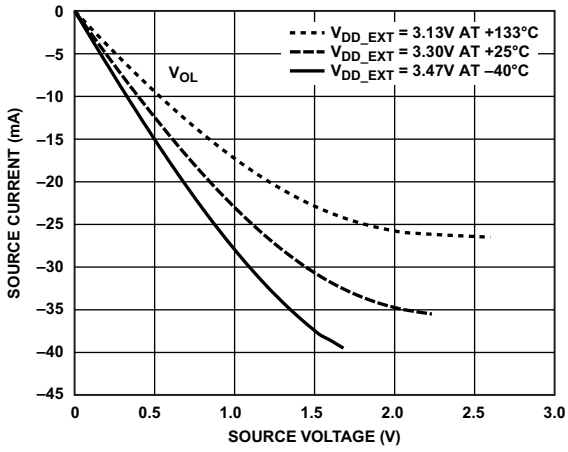


Figure 78. Driver Type D Current (3.3 V V_{DD_EXT})

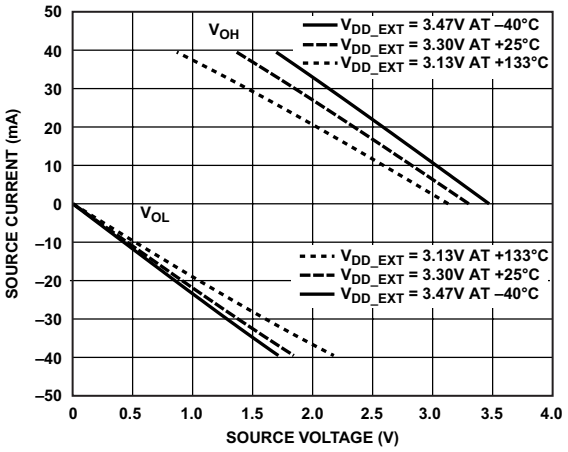


Figure 79. Driver Type H Current (3.3 V V_{DD_EXT})

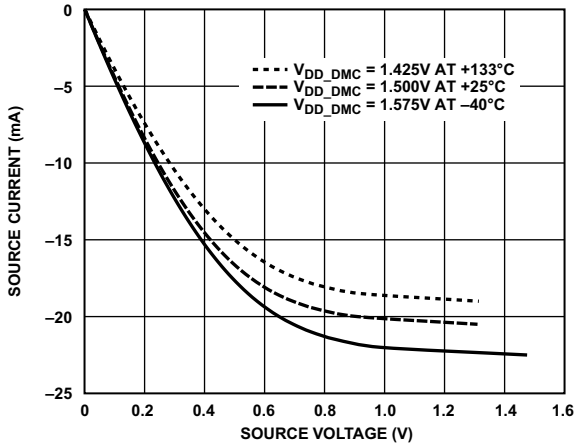


Figure 80. Driver Type B and Driver Type C (DDR3 Drive Strength 40 Ω)

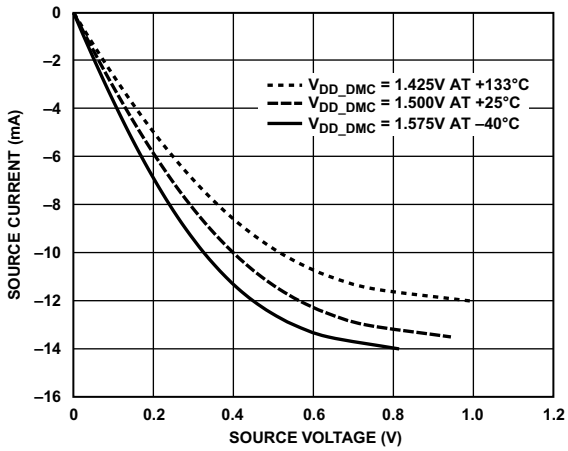


Figure 81. Driver Type B and Driver Type C (DDR3 Drive Strength 60 Ω)