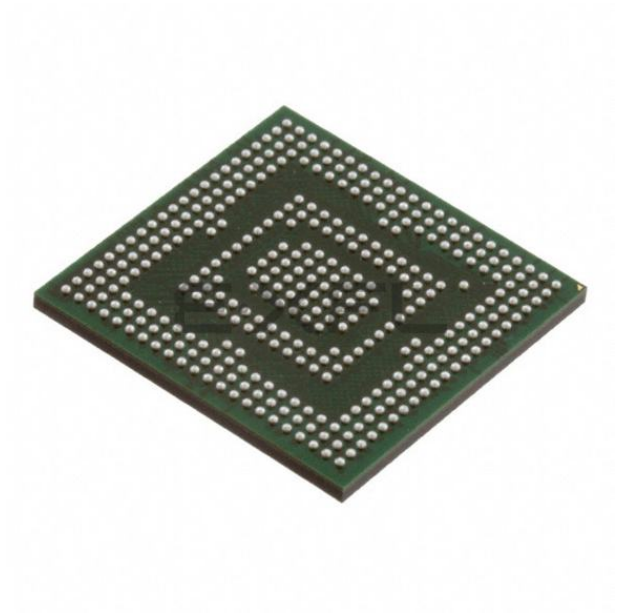

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc582bbcz-4a

The processing elements are referred to as PEx and PEy data registers and each contain an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

Single instruction multiple data (SIMD) mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also affects the way data transfers between memory and processing elements because to sustain computational operation in the processing elements requires twice the data bandwidth. Therefore, entering SIMD mode doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values transfer with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, arithmetic/logic unit (ALU), and shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, IEEE 64-bit double-precision floating-point, and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

Core Timer

Each SHARC+ processor core also has a timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, while control bits in MODE1 activate the secondary registers.

Universal Registers (USTAT)

General-purpose tasks use the universal registers. The four USTAT registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-SC58x/ADSP-2158x processor uses the two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set Architecture (ISA)

The ISA, a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction. Additionally, the double-precision floating-point instruction set is an addition to the SHARC+ core.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the SHARC+ core processors support 16-bit and 32-bit opcodes for many instructions, formerly 48-bit in the ISA. This feature, called variable instruction set architecture (VISA), drops redundant or unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external memories. VISA is not an operating mode; it is only address dependent (refer to memory map ISA/VISA address spaces in Table 7). Furthermore, it allows jumps between ISA and VISA instruction fetches.

Memory Direct Memory Access (MDMA)

The processor supports various MDMA operations, including,

- Standard bandwidth MDMA channels with CRC protection (32-bit bus width, runs on SCLK0)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channels (64-bit bus width, run on SYCLK, one channel can be assigned to the FFT accelerator)

Extended Memory DMA

Extended memory DMA supports various operating modes such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory) with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

Cyclic Redundant C ode (CRC) Protection

The cyclic redundant codes (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, every 100 ms the system software initiates the signature calculation of the entire memory contents and compares these contents with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit/byte mirroring option (endianness)
- Fault/error interrupt mechanisms
- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of a memory or an MMR block

Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for five different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exceptions event occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered on the one side by the SHARC+ core, such as data alignment (SIMD/long word) or compute violations (fixed or floating point), and illegal instructions cause core exceptions. Conditions triggered on the other side by the SEC, such as error correcting codes (ECC)/parity/watchdog/system clock, cause system exceptions.
- An interrupts event occurs asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

Both SHARC+ cores feature a system event controller. The SEC features include the following:

- Comprehensive system event source management including interrupt enable, fault enable, priority, core mapping, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A slave control port that provides access to all SEC registers for configuration, status, and interrupt/fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC1_UDM	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Data Mask for Upper Byte Notes: No notes
DMC1_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode
$\overline{\text{DMC1\_UDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data Strobe for Upper Byte (complement) Notes: No notes
DMC1_VREF	a		none	none	none	VDD_DMC	Desc: DMC1 Voltage Reference Notes: No notes
$\overline{\text{DMC1\_WE}}$	Output	B	none	none	none		Desc: DMC1 Write Enable Notes: No notes
GND	g	NA	none	none	none		Desc: Ground Notes: No notes
HADC0_VIN0	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If Input not used connect to GND
HADC0_VIN1	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If Input not used connect to GND
HADC0_VIN2	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If Input not used connect to GND
HADC0_VIN3	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If Input not used connect to GND
HADC0_VIN4	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 4 Notes: If Input not used connect to GND
HADC0_VIN5	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 5 Notes: If Input not used connect to GND
HADC0_VIN6	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 6 Notes: If Input not used connect to GND
HADC0_VIN7	a	NA	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 7 Notes: If Input not used connect to GND

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
HADC0_VREFN	s	NA	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: No notes
HADC0_VREFP	s	NA	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: No notes
JTG_TCK	Input		PullUp	none	none	VDD_EXT	Desc: JTAG Clock Notes: No notes
JTG_TDI	Input		PullUp	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes
JTG_TDO	Output	A	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out Notes: No notes
JTG_TMS	InOut	A	PullUp	none	none	VDD_EXT	Desc: JTAG Mode Select Notes: No notes
$\overline{\text{JTG\_TRST}}$	Input		PullDown	none	none	VDD_EXT	Desc: JTAG Reset Notes: No notes
MLB0_CLKN	Input	NA	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Clock (-) Notes: No notes
MLB0_CLKP	Input	NA	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Clock (+) Notes: No notes
MLB0_DATN	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Data (-) Notes: No notes
MLB0_DATP	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Data (+) Notes: No notes
MLB0_SIGN	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Signal (-) Notes: No notes
MLB0_SIGP	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Signal (+) Notes: No notes
PA_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 0 | EMAC0 Transmit Data 0 | SMC0 Address 21 Notes: No notes
PA_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 1 | EMAC0 Transmit Data 1 | SMC0 Address 20 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 15 | EMAC0 PTP Pulse-Per-Second Output 2 | SINC0 Data 1 | SMC0 Address 9 Notes: No notes
PB_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 0 | EMAC0 PTP Pulse-Per-Second Output 1 | EPPI0 Data 14 | SINC0 Data 2 | SMC0 Address 8 | TIMER0 Alternate Clock 3 Notes: No notes
PB_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 1 | EMAC0 PTP Pulse-Per-Second Output 0 | EPPI0 Data 15 | SINC0 Clock 0 | SMC0 Address 7 | TIMER0 Alternate Clock 4 Notes: No notes
PB_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 2 | EMAC0 PTP Clock Input 0 | EPPI0 Data 16 | SMC0 Address 4 | UART1 Transmit Notes: No notes
PB_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 3 | EMAC0 PTP Auxiliary Trigger Input 0 | EPPI0 Data 17 | SMC0 Address 3 | UART1 Receive | TIMER0 Alternate Capture Input 1 Notes: No notes
PB_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 4 | EPPI0 Data 12 | MLB0 Single-Ended Clock | SINC0 Data 3 | SMC0 Asynchronous Ready | EMAC0 PTP Auxiliary Trigger Input 1 Notes: No notes
PB_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 5 | EPPI0 Data 13 | MLB0 Single-Ended Signal | SMC0 Address 1 | EMAC0 PTP Auxiliary Trigger Input 2 Notes: No notes
PB_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 6 | MLB0 Single-Ended Data | PWM0 Channel B High Side | SMC0 Address 2 | EMAC0 PTP Auxiliary Trigger Input 3 Notes: No notes
PB_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 7 | LP1 Data 0 | PWM0 Channel A High Side | SMC0 Data 15 | TIMER0 Timer 3 Notes: No notes
PB_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 8 | LP1 Data 1 | PWM0 Channel A Low Side | SMC0 Data 14 | TIMER0 Timer 4 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 9 | CAN1 Transmit | LP1 Data 2 | SMC0 Data 13 Notes: No notes
PB_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 10 | CAN1 Receive | LP1 Data 3 | SMC0 Data 12 | TIMER0 Timer 2 | TIMER0 Alternate Capture Input 4 Notes: No notes
PB_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 11 | LP1 Data 4 | PWM0 Channel D High Side | SMC0 Data 11 | CNT0 Count Zero Marker Notes: No notes
PB_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 12 | LP1 Data 5 | PWM0 Channel D Low Side | SMC0 Data 10 | CNT0 Count Up and Direction Notes: No notes
PB_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 13 | LP1 Data 6 | PWM0 Channel C High Side | SMC0 Data 9 Notes: No notes
PB_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 14 | LP1 Data 7 | PWM0 Channel C Low Side | SMC0 Data 8 | TIMER0 Timer 5 | CNT0 Count Down and Gate Notes: No notes
PB_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 15 | LP1 Acknowledge | PWM0 Shutdown Input 0 | SMC0 Write Enable | TIMER0 Timer 1 Notes: No notes
PCIE0_CLKM	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK - Notes: No notes
PCIE0_CLKP	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK + Notes: No notes
PCIE0_REF	a	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 Reference Notes: No notes
PCIE0_RXM	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX - Notes: No notes
PCIE0_RXP	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX + Notes: No notes
PCIE0_TXM	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX - Notes: No notes
PCIE0_TXP	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX + Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 13 | ACM0 ADC Control Signals | SPI1 Slave Select Output 1 | UART0 Transmit Notes: No notes
PC_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 14 | ACM0 ADC Control Signals | UART0 Receive | TIMER0 Alternate Capture Input 0 Notes: No notes
PC_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 15 | ACM0 ADC Control Signals | EPPI0 Frame Sync 3 (FIELD) | SMC0 Memory Select 0 | UART0 Request to Send Notes: No notes
PD_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 0 | ACM0 ADC Control Signals | EPPI0 Data 23 | SMC0 Data 7 | UART0 Clear to Send Notes: No notes
PD_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 1 | ACM0 ADC Control Signals | SMC0 Output Enable | SPI0 Slave Select Output 2 | SPI0 Slave Select Input Notes: No notes
PD_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 2 | LP0 Data 0 | PWM1 Shutdown Input 0 | TRACE0 Trace Data 0 Notes: No notes
PD_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 3 | LP0 Data 1 | PWM1 Channel A High Side | TRACE0 Trace Data 1 Notes: No notes
PD_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 4 | LP0 Data 2 | PWM1 Channel A Low Side | TRACE0 Trace Data 2 Notes: No notes
PD_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 5 | LP0 Data 3 | PWM1 Channel B High Side | TRACE0 Trace Data 3 Notes: No notes
PD_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 6 | LP0 Data 4 | PWM1 Channel B Low Side | TRACE0 Trace Data 4 Notes: No notes
PD_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 7 | LP0 Data 5 | PWM1 Channel C High Side | TRACE0 Trace Data 5 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PG_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 4 | EMAC1 Receive Data 0 | TRACE0 Trace Data | TRACE0 Trace Data 14 Notes: No notes
PG_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 5 | EMAC1 Receive Data 1 | TRACE0 Trace Data | TRACE0 Trace Data 15 Notes: No notes
RTC0_CLKIN	a	NA	none	none	none	VDD_RTC	Desc: RTC0 Crystal input / external oscillator connection Notes: Connect to GND if not used
RTC0_XTAL	a	NA	none	none	none	VDD_RTC	Desc: RTC0 Crystal output Notes: No notes
SYS_BMODE0	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_BMODE1	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_BMODE2	Input	NA	PullDown	none	none	VDD_EXT	Desc: Boot Mode Control n Notes: No notes
SYS_CLKIN0	a	NA	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: No notes
SYS_CLKIN1	a	NA	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: Connect to GND if not used
SYS_CLKOUT	a	A	none	none	none		Desc: Processor Clock Output Notes: No notes
SYS_FAULT	InOut	A	none	none	none		Desc: Active-High Fault Output Notes: External pull-down required to keep signal in de-asserted state
$\overline{\text{SYS\_FAULT}}$	InOut	A	none	none	none		Desc: Active-Low Fault Output Notes: External pull-up required to keep signal in de-asserted state
$\overline{\text{SYS\_HWRST}}$	Input	NA	none	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No notes
$\overline{\text{SYS\_RESOUT}}$	Output	A	none	none	L	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	a	NA	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
SYS_XTAL1	a	NA	none	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.

Asynchronous Page Mode Read

Table 47 and Figure 14 show asynchronous memory page mode read timing, related to the SMC.

Table 47. Asynchronous Page Mode Read

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AV}	SMC0_Axx (Address) Valid for First Address Minimum Width[1]	(PREST + RST + PREAT + RAT) × t_{SCLK0} – 2		ns
t_{AV1}	SMC0_Axx (Address) Valid for Subsequent SMC0_Ax (Address) Minimum Width	PGWS × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
t_{HARE}	Output[3] Hold After $\overline{\text{SMC0\_ARE}}$ High[4]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[5]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[6, 7]	(RAT + (Nw – 1) × PGWS) × t_{SCLK0} – 2		ns

[1] PREST, RST, PREAT and RAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$.
[4] RHT value set using the SMC_BxTIM.RHT bits.
[5] SMC_BxCTL.ARDYEN bit = 0.
[6] RAT value set using the SMC_BxTIM.RAT bits.
[7] Nw = Number of 16-bit data words read.

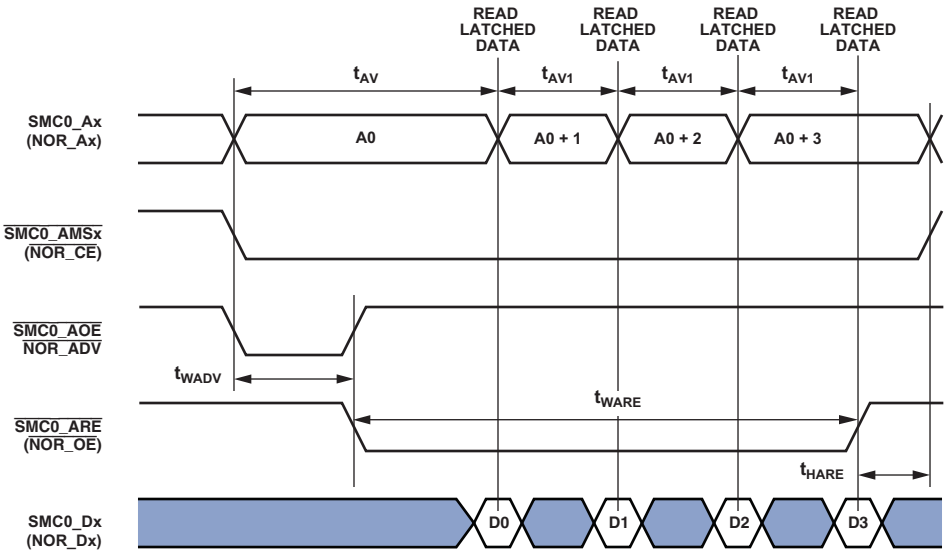

Figure 14. Asynchronous Page Mode Read

Mobile DDR (LPDDR) SDRAM Clock and Control Cycle Timing

Table 54 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the DMC.

Table 54. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	1		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

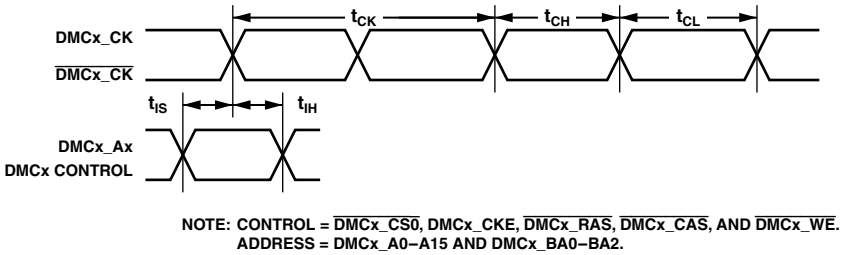

Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Write Cycle Timing

Table 56 and Figure 22 show mobile DDR SDRAM write cycle timing, related to the DMC.

Table 56. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	200 MHz[2] Max	Unit
Switching Characteristics				
t_{DQSS}[3]	DMCx_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMCx_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMCx_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMCx_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMCx_DQS Falling Edge Hold Time From DMCx_CK	0.2		t_{CK}
t_{DQSH}	DMCx_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMCx_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMCx_DQ and DMCx_DM Output Pulse Width	1.8		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] Write command to first DMCx_DQS delay = WL × t_{CK} + t_{DQSS}.

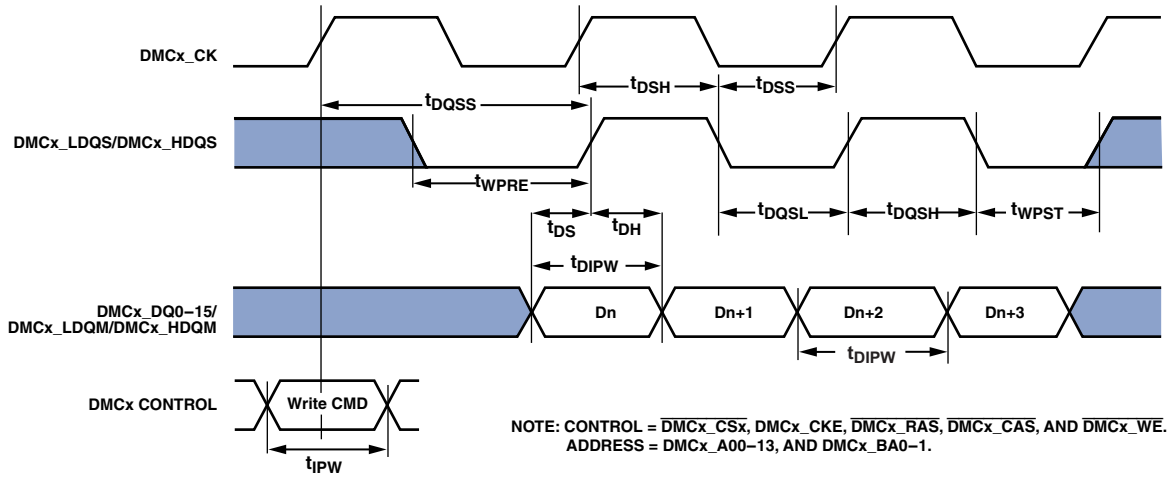

Figure 22. Mobile DDR SDRAM Controller Output AC Timing

Link Ports (LP)

In LP receive mode, the link port clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by:

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In link port transmit mode, the programmed link port clock ($f_{LCLKTPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{CLKO8}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{CLKO8}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}).

Table 62. Link Ports—Receive[1]

Parameter		Min	Max	Unit
Timing Requirements				
$f_{LCLKREXT}$	LPx_CLK Frequency		150	MHz
t_{SLDCL}	Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL}	Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKEW}	LPx_CLK Period[2]	$t_{LCLKREXT}$ – 0.42		ns
$t_{LCLKRWL}$	LPx_CLK Width Low[2]	0.5 × $t_{LCLKREXT}$		ns
$t_{LCLKRWH}$	LPx_CLK Width High[2]	0.5 × $t_{LCLKREXT}$		ns
Switching Characteristic				
t_{DLALC}	LPx_ACK Low Delay After LPx_CLK Low[3]	1.5 × t_{CLKO8} + 4	2.5 × t_{CLKO8} + 12	ns

[1] Specifications apply to LP0 and LP1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency see the $f_{LCLKTEXT}$ specification in Table 29.
[3] LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

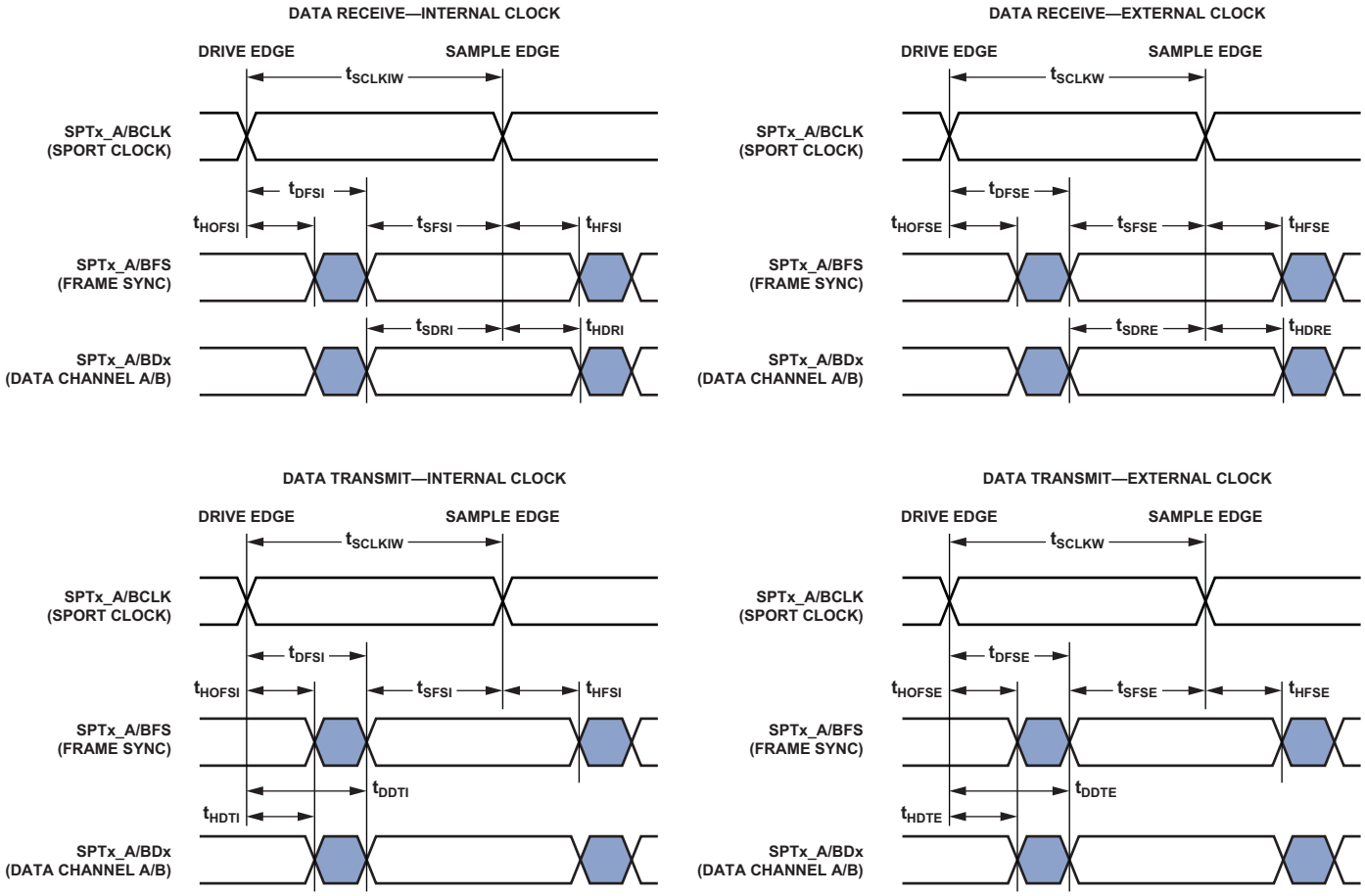

Figure 37. Serial Ports

The SPTx_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPTx_TDV is asserted for communication with external devices.

Table 67. Serial Ports—TDV (Transmit Data Valid)[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DRDVEN}	Data Valid Enable Delay from Drive Edge of External Clock[2]	2		ns
t_{DFDVEN}	Data Valid Disable Delay from Drive Edge of External Clock[2]		14	ns
t_{DRDVIN}	Data Valid Enable Delay from Drive Edge of Internal Clock[2]	–2.5		ns
t_{DFDVIN}	Data Valid Disable Delay from Drive Edge of Internal Clock[2]		3.5	ns

[1] Specifications apply to all eight SPORTs.
[2] Referenced to drive edge.

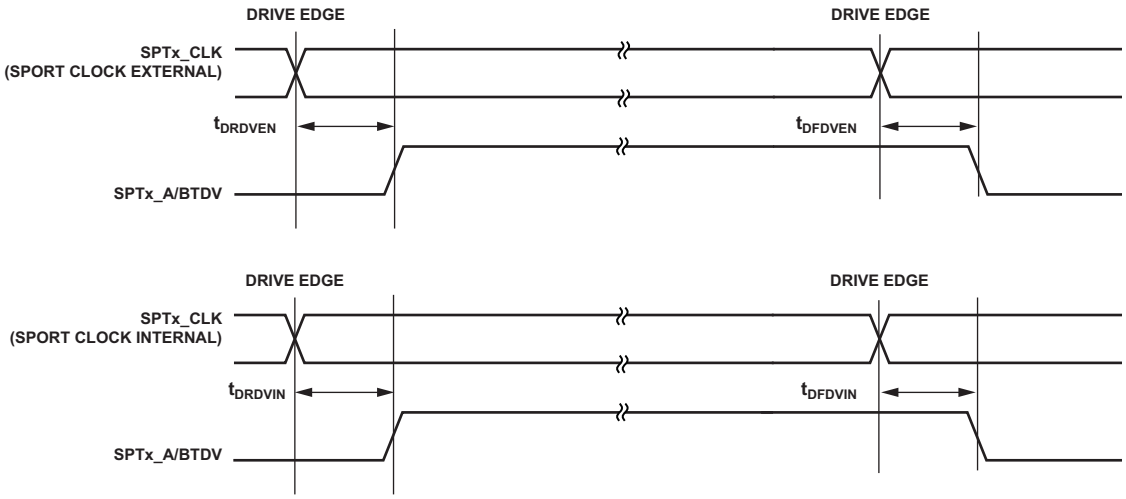

Figure 39. Serial Ports—Transmit Data Valid Internal and External Clock

Sample Rate Converter—Serial Output Port

For the serial output port, the frame sync is an input and it must meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. The serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 70. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		13	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN, SCLK0, or any of the DAI pins.

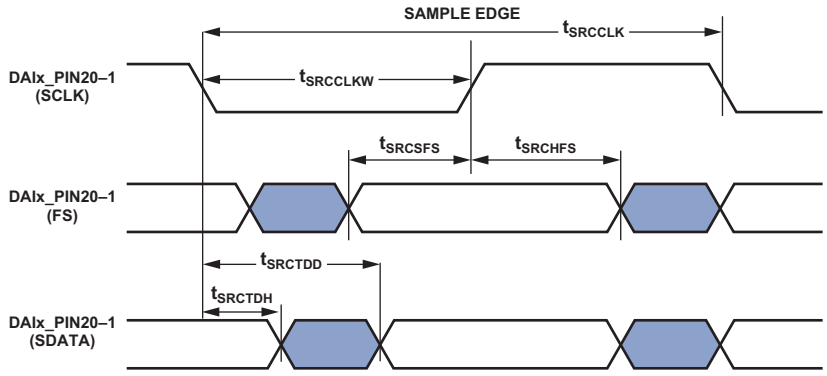

Figure 42. ASRC Serial Output Port Timing

SPI Port—Slave Timing

Table 72 and Figure 44 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 72. SPI Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLK} - 1$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

[1] All specifications apply to all three SPIs.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in Table 29.

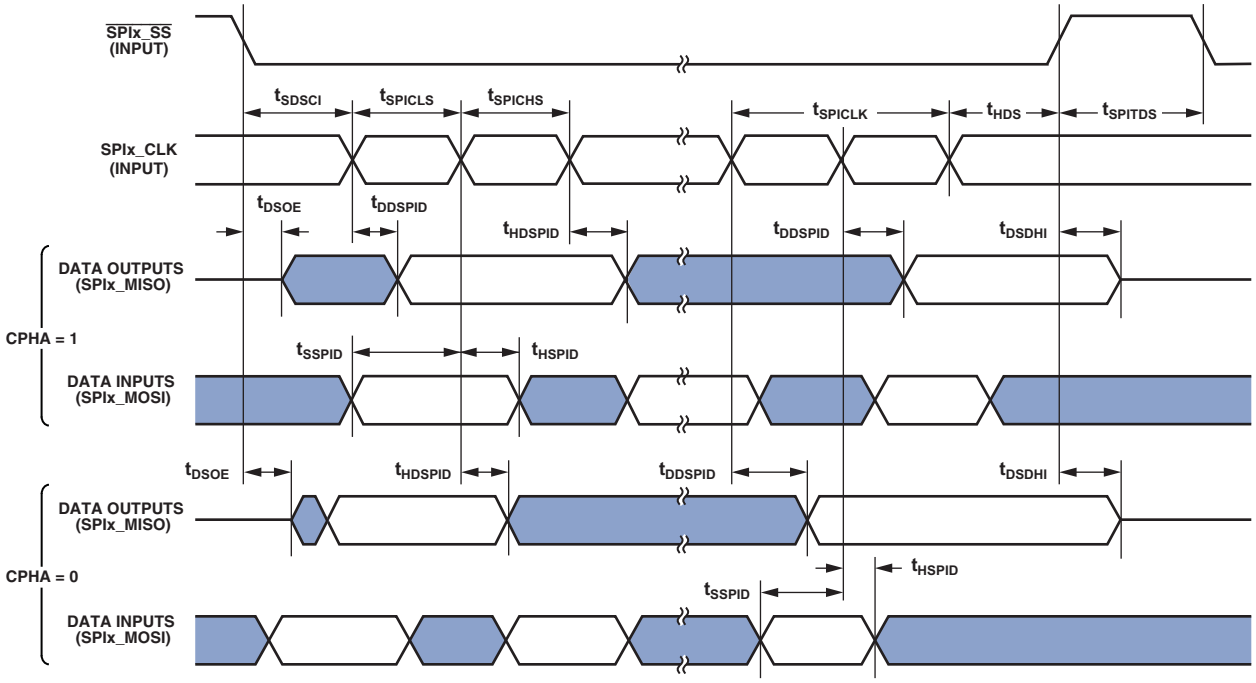

Figure 44. SPI Port—Slave Timing

ADSP-SC58x/ADSP-2158x 349-BALL BGA BALL ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
DAI0_PIN01	Y07	DMC0_CAS	C06	GND	J09	GND	T07
DAI0_PIN02	Y05	DMC0_CK	A13	GND	J10	GND	T08
DAI0_PIN03	Y06	DMC0_CKE	A05	GND	J11	GND	T09
DAI0_PIN04	AA04	DMC0_CK	A12	GND	J12	GND	T10
DAI0_PIN05	AA05	DMC0_CS0	C11	GND	J13	GND	T11
DAI0_PIN06	Y04	DMC0_DQ00	B17	GND	J14	GND	T12
DAI0_PIN07	T03	DMC0_DQ01	A17	GND	K08	GND	T13
DAI0_PIN08	AB03	DMC0_DQ02	B16	GND	K09	GND	T14
DAI0_PIN09	AB02	DMC0_DQ03	B15	GND	K10	GND	T15
DAI0_PIN10	AA03	DMC0_DQ04	B14	GND	K11	GND	T16
DAI0_PIN11	AA01	DMC0_DQ05	B13	GND	K12	GND	Y12
DAI0_PIN12	Y03	DMC0_DQ06	A14	GND	K13	GND	Y20
DAI0_PIN19	W03	DMC0_DQ07	B12	GND	K14	HADC0_VIN0	AB11
DAI0_PIN20	V03	DMC0_DQ08	B11	GND	K15	HADC0_VIN1	AB12
DAI1_PIN01	P20	DMC0_DQ09	A10	GND	L08	HADC0_VIN2	AA11
DAI1_PIN02	N21	DMC0_DQ10	B10	GND	L09	HADC0_VIN3	AB13
DAI1_PIN03	P22	DMC0_DQ11	B09	GND	L10	HADC0_VIN4	AA13
DAI1_PIN04	N20	DMC0_DQ12	B07	GND	L11	HADC0_VIN5	AA12
DAI1_PIN05	P21	DMC0_DQ13	A07	GND	L12	HADC0_VIN6	Y13
DAI1_PIN06	R22	DMC0_DQ14	B06	GND	L13	HADC0_VIN7	AA14
DAI1_PIN07	R21	DMC0_DQ15	A06	GND	L14	HADC0_VREFN	AB10
DAI1_PIN08	R20	DMC0_LDM	C13	GND	L15	HADC0_VREFP	AB09
DAI1_PIN09	T22	DMC0_LDQS	A16	GND	M08	JTG_TCK	M03
DAI1_PIN10	T21	DMC0_LDQS	A15	GND	M09	JTG_TDI	J03
DAI1_PIN11	U21	DMC0_ODT	B05	GND	M10	JTG_TDO	P03
DAI1_PIN12	T20	DMC0_RAS	A04	GND	M11	JTG_TMS	M02
DAI1_PIN19	U22	DMC0_RESET	F01	GND	M12	JTG_TRST	M01
DAI1_PIN20	U20	DMC0_RZQ	C09	GND	M13	MLB0_CLKN	AB19
DMC0_A00	B04	DMC0_UDM	C14	GND	M14	MLB0_CLKP	AB18
DMC0_A01	C08	DMC0_UDQS	A09	GND	M15	MLB0_DATN	AB17
DMC0_A02	B03	DMC0_UDQS	A08	GND	N08	MLB0_DATP	AB16
DMC0_A03	C05	DMC0_VREF	A11	GND	N09	MLB0_SIGN	AB15
DMC0_A04	A03	DMC0_WE	C10	GND	N10	MLB0_SIGP	AB14
DMC0_A05	E05	GND	A01	GND	N11	PA_00	V20
DMC0_A06	A02	GND	A18	GND	N12	PA_01	V21
DMC0_A07	B01	GND	A22	GND	N13	PA_02	V22
DMC0_A08	C04	GND	AA02	GND	N14	PA_03	W21
DMC0_A09	C02	GND	AA21	GND	N15	PA_04	W22
DMC0_A10	C01	GND	AB01	GND	P09	PA_05	W20
DMC0_A11	D01	GND	AB22	GND	P10	PA_06	Y21
DMC0_A12	D02	GND	B02	GND	P11	PA_07	AB21
DMC0_A13	E03	GND	B08	GND	P12	PA_08	Y22
DMC0_A14	E01	GND	B21	GND	P13	PA_09	AA22
DMC0_A15	E02	GND	C03	GND	P14	PA_10	Y18
DMC0_BA0	C07	GND	C12	GND	R01	PA_11	AA20
DMC0_BA1	F03	GND	C20	GND	R07	PA_12	AA19
DMC0_BA2	D03	GND	H16	GND	R16	PA_13	AB20

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
PA_14	AA17	PD_14	E22	VDD_DMC	G09	VDD_INT	J20
PA_15	Y19	PD_15	F21	VDD_DMC	G10	VDD_INT	K06
PB_00	Y15	PE_00	F22	VDD_DMC	G11	VDD_INT	K20
PB_01	Y17	PE_01	G21	VDD_DMC	G12	VDD_INT	L04
PB_02	AA16	PE_02	G22	VDD_DMC	G13	VDD_INT	L06
PB_03	AA18	PE_03	H21	VDD_DMC	G14	VDD_INT	L19
PB_04	Y16	PE_04	H22	VDD_DMC	G15	VDD_INT	M04
PB_05	AA15	PE_05	J21	VDD_DMC	G16	VDD_INT	M06
PB_06	Y14	PE_06	J22	VDD_DMC	G17	VDD_INT	M19
PB_07	U03	PE_07	K22	VDD_DMC	H06	VDD_INT	U09
PB_08	Y02	PE_08	K21	VDD_DMC	H07	VDD_INT	U10
PB_09	Y01	PE_09	L22	VDD_DMC	H17	VDD_INT	U11
PB_10	W01	PE_10	L21	VDD_DMC	J06	VDD_INT	U12
PB_11	W02	PE_11	L20	VDD_EXT	J17	VDD_INT	U13
PB_12	V02	PE_12	M22	VDD_EXT	K17	VDD_INT	W11
PB_13	V01	PE_13	M20	VDD_EXT	L17	VDD_INT	W12
PB_14	R03	PE_14	N22	VDD_EXT	M17	VDD_USB	U08
PB_15	R02	PE_15	M21	VDD_EXT	N06		
PC_00	N03	SYS_BMODE0	N02	VDD_EXT	N17		
PC_01	L01	SYS_BMODE1	P02	VDD_EXT	P06		
PC_02	K02	SYS_BMODE2	T02	VDD_EXT	P17		
PC_03	K01	SYS_CLKIN0	U01	VDD_EXT	R06		
PC_04	G03	SYS_CLKIN1	P01	VDD_EXT	R17		
PC_05	J01	SYS_CLKOUT	C17	VDD_EXT	T06		
PC_06	J02	SYS_FAULT	H03	VDD_EXT	T17		
PC_07	H02	$\overline{\text{SYS\_FAULT}}$	K03	VDD_EXT	U06		
PC_08	H01	$\overline{\text{SYS\_HWRST}}$	L02	VDD_EXT	U07		
PC_09	L03	$\overline{\text{SYS\_RESOUT}}$	U02	VDD_EXT	U14		
PC_10	G02	SYS_XTAL0	T01	VDD_EXT	U15		
PC_11	F02	SYS_XTAL1	N01	VDD_EXT	U16		
PC_12	G01	TWI0_SCL	Y09	VDD_EXT	U17		
PC_13	B18	TWI0_SDA	AA10	VDD_HADC	Y11		
PC_14	C16	TWI1_SCL	AB08	VDD_INT	D11		
PC_15	C18	TWI1_SDA	Y10	VDD_INT	D12		
PD_00	A19	TWI2_SCL	AA08	VDD_INT	E20		
PD_01	C15	TWI2_SDA	AA09	VDD_INT	F07		
PD_02	B19	USB0_DM	AB07	VDD_INT	F08		
PD_03	A20	USB0_DP	AB06	VDD_INT	F09		
PD_04	C19	USB0_ID	AA06	VDD_INT	F10		
PD_05	B20	USB0_VBC	Y08	VDD_INT	F12		
PD_06	A21	USB0_VBUS	AA07	VDD_INT	F13		
PD_07	C21	USB_CLKIN	AB04	VDD_INT	F14		
PD_08	B22	USB_XTAL	AB05	VDD_INT	F15		
PD_09	D21	VDD_DMC	F06	VDD_INT	F16		
PD_10	D20	VDD_DMC	F11	VDD_INT	F17		
PD_11	C22	VDD_DMC	G06	VDD_INT	F20		
PD_12	D22	VDD_DMC	G07	VDD_INT	G20		
PD_13	E21	VDD_DMC	G08	VDD_INT	H20		

CONFIGURATION OF THE 349-BALL CSP_BGA

Figure 98 shows an overview of signal placement on the 349-ball CSP_BGA.

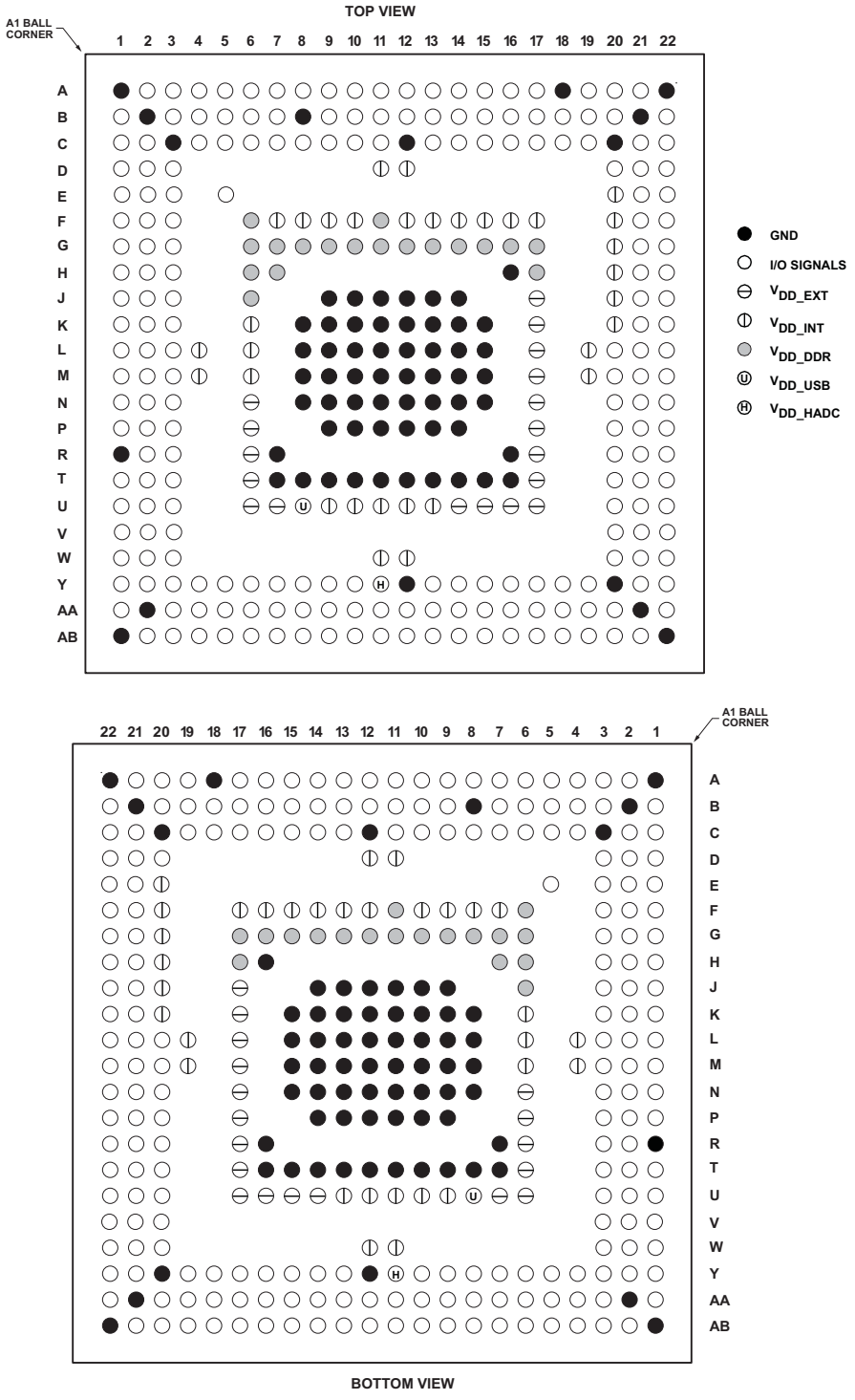

Figure 98. 349-Ball CSP_BGA Configuration