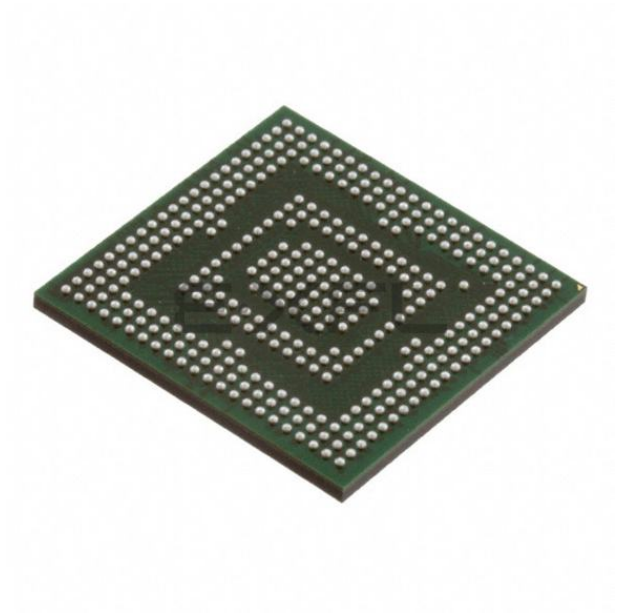

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 95°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc582cbcz-4a

GENERAL DESCRIPTION

The ADSP-SC58x/ADSP-2158x processors are members of the SHARC® family of products. The ADSP-SC58x processor is based on the SHARC+ dual core and the ARM® Cortex®-A5 core. The ADSP-SC58x/ADSP-2158x SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI). New additions to the SHARC+ core include cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a set of industry leading system peripherals and memory (see Table 1, Table 2, and Table 3), the ARM Cortex-A5 and SHARC processor is the platform of choice for applications that require programmability similar to RISC (reduced instruction set computing), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, pro audio, and industrial-based applications that require high floating-point performance.

Table 2 provides comparison information for features that vary across the standard processors. (N/A in the table means not applicable.)

Table 3 provides comparison information for features that vary across the automotive processors. (N/A in the table means not applicable.)

Table 1. Common Product Features

Product Features	ADSP-SC58x/ADSP-2158x
DAI (includes SRU)	2
Full SPORTs	4 per DAI
S/PDIF receive/transmit	1per DAI
ASRCs	4 pair per DAI
PCGs	2 per DAI
I^2C (TWI)	3
Quad-data bit SPI	1
Dual-data bit SPI	2
CAN2.0	2
UARTs	3
Link ports	2
Enhanced PPI	1
GP timer[1]	8
GP counter	1
Enhanced PWMs[2]	3
Watchdog timers	2
ADC control module	Yes
Static memory controller	Yes
Hardware accelerators	
High performance FFT/IFFT	Yes
FIR/IIR	Yes
Harmonic analysis engine	Yes
SINC filter	Yes
Security cryptographic engine	Yes
Multichannel 12-bit ADC	8-channel

[1] Eight timers are available in the 529-BGA package only. The 349-BGA package does not include Timer 6 and 7.

[2] Three 3ePWMs are available in the 529-BGA package only. The 349-BGA package does not include PWM 2.

SYSTEM MEMORY MAP

Table 4. L1 Block 0, Block 1, Block 2, and Block 3 SHARC+ Addressing Memory Map (Private Address Space)

Memory	Long Word (64 Bits)	Extended Precision/ ISA Code (48 Bits)	Normal Word (32 Bits)	Short Word/ VISA Code (16 Bits)	Byte Access (8 Bits)
L1 Block 0 SRAM (1.5 Mb)	0x00048000–0x0004DFFF	0x00090000–0x00097FFF	0x00090000–0x0009BFFF	0x00120000–0x00137FFF	0x00240000–0x0026FFFF
L1 Block 1 SRAM (1.5 Mb)	0x00058000–0x0005DFFF	0x000B0000–0x000B7FFF	0x000B0000–0x000BBFFF	0x00160000–0x00177FFF	0x002C0000–0x002EFFFF
L1 Block 2 SRAM (1 Mb)	0x00060000–0x00063FFF	0x000C0000–0x000C5554	0x000C0000–0x000C7FFF	0x00180000–0x0018FFFF	0x00300000–0x0031FFFF
L1 Block 3 SRAM (1 Mb)	0x00070000–0x00073FFF	0x000E0000–0x000E5554	0x000E0000–0x000E7FFF	0x001C0000–0x001CFFFF	0x00380000–0x0039FFFF

Table 5. L2 Memory Addressing Map

Memory[1]	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	Instruction Fetch VISA Address Space SHARC+	Instruction Fetch ISA Address Space SHARC+
L2 Boot ROM0[2]	ARM: 0x00000000–0x00007FFF SHARC+/DMA: 0x20000000–0x20007FFF	0x08000000–0x08001FFF	0x00B80000–0x00B83FFF	0x00580000–0x00581555
L2 RAM (2 Mb)	0x20080000–0x200BFFFF	0x08020000–0x0802FFFF	0x00BA0000–0x00BBFFFF	0x005A0000–0x005AAAAF
L2 Boot ROM1	0x20100000–0x20107FFF	0x08040000–0x08041FFF	0x00B00000–0x00B03FFF	0x00500000–0x00501555
L2 ROM1	0x20180000–0x201BFFFF	0x08060000–0x0806FFFF	0x00B20000–0x00B3FFFF	0x00520000–0x0052AAAF
L2 Boot ROM2[3]	0x20200000–0x20207FFF	0x08080000–0x08081FFF	0x00B40000–0x00B43FFF	0x00540000–0x00541555
L2 ROM2	0x20280000–0x202BFFFF	0x080A0000–0x080AFFFF	0x00B60000–0x00B7FFFF	0x00560000–0x0056AAAF

[1] All L2 RAM/ROM blocks are subdivided into eight banks.
[2] For ADSP-SC58x products, the L2 Boot ROM0 byte address space is 0x 0000 0000–0x 0000 7FFF.
[3] L2 Boot ROM address for ADSP-2158x products.

Table 6. SHARC+ L1 Memory in Multiprocessor Space

		Memory Block	Byte Address Space for ARM Cortex-A5 and SHARC+	Normal Word Address Space for SHARC+
L1 memory of SHARC1 in multiprocessor space	Address via Slave1 Port	Block 0	0x28240000–0x2826FFFF	0x0A090000–0xA09BFFF
		Block 1	0x282C0000–0x282EFFFF	0x0A0B0000–0xA0BBFFF
		Block 2	0x28300000–0x2831FFFF	0x0A0C0000–0x0A0C7FFF
		Block 3	0x28380000–0x2839FFFF	0x0A0E0000–0x0A0E7FFF
	Address via Slave2 Port	Block 0	0x28640000–0x2866FFFF	0x0A190000–0x0A19BFFF
		Block 1	0x286C0000–0x286EFFFF	0x0A1B0000–0x0A1BBFFF
		Block 2	0x28700000–0x2871FFFF	0x0A1C0000–0x0A1C7FFF
		Block 3	0x28780000–0x2879FFFF	0x0A1E0000–0x0A1E7FFF
L1 memory of SHARC2 in multiprocessor space	Address via Slave1 Port	Block 0	0x28A40000–0x28A6FFFF	0x0A290000–0x0A29BFFF
		Block 1	0x28AC0000–0x28AEFFFF	0x0A2B0000–0x0A2BBFFF
		Block 2	0x28B00000–0x28B1FFFF	0x0A2C0000–0x0A2C7FFF
		Block 3	0x28B80000–0x28B9FFFF	0x0A2E0000–0x0A2E7FFF
	Address via Slave2 Port	Block 0	0x28E40000–0x28E6FFFF	0x0A390000–0x0A39BFFF
		Block 1	0x28EC0000–0x28EEFFFF	0x0A3B0000–0x0A3BBFFF
		Block 2	0x28F00000–0x28F1FFFF	0x0A3C0000–0x0A3C7FFF
		Block 3	0x28F80000–0x28F9FFFF	0x0A3E0000–0x0A3E7FFF

This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in circuit programming of the on-board Flash device to store user specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend the capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product.

Middleware Packages

Analog Devices offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos2
- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/ucusbh
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see "Analog Devices JTAG Emulation Technical Reference" (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-SC58x/ADSP-2158x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0\_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0\_LDQS}}$
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0\_RAS}}$	DMC0 Row Address Strobe	Not Muxed	$\overline{\text{DMC0\_RAS}}$
$\overline{\text{DMC0\_RESET}}$	DMC0 Reset (DDR3 only)	Not Muxed	$\overline{\text{DMC0\_RESET}}$
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0\_UDQS}}$	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0\_UDQS}}$
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
$\overline{\text{DMC0\_WE}}$	DMC0 Write Enable	Not Muxed	$\overline{\text{DMC0\_WE}}$
ETH0_CRS	ETH0 Carrier Sense/RMII Receive Data Valid	A	PA_07
ETH0_MDC	ETH0 Management Channel Clock	A	PA_02
ETH0_MDIO	ETH0 Management Channel Serial Data	A	PA_03
ETH0_PTPAUXIN0	ETH0 PTP Auxiliary Trigger Input 0	B	PB_03
ETH0_PTPAUXIN1	ETH0 PTP Auxiliary Trigger Input 1	B	PB_04
ETH0_PTPAUXIN2	ETH0 PTP Auxiliary Trigger Input 2	B	PB_05
ETH0_PTPAUXIN3	ETH0 PTP Auxiliary Trigger Input 3	B	PB_06
ETH0_PTPCLKIN0	ETH0 PTP Clock Input 0	B	PB_02
ETH0_PTPPPS0	ETH0 PTP Pulse Per Second Output 0	B	PB_01
ETH0_PTPPPS1	ETH0 PTP Pulse Per Second Output 1	B	PB_00
ETH0_PTPPPS2	ETH0 PTP Pulse Per Second Output 2	A	PA_15
ETH0_PTPPPS3	ETH0 PTP Pulse Per Second Output 3	A	PA_14
ETH0_RXCLK_REFCLK	ETH0 RXCLK (GigE) or REFCLK (10/100)	A	PA_06
ETH0_RXCTL_CRS	ETH0 RXCTL (GigE) or CRS (10/100)	A	PA_07
ETH0_RXD0	ETH0 Receive Data 0	A	PA_04
ETH0_RXD1	ETH0 Receive Data 1	A	PA_05
ETH0_RXD2	ETH0 Receive Data 2	A	PA_08
ETH0_RXD3	ETH0 Receive Data 3	A	PA_09
ETH0_TXCLK	ETH0 Transmit Clock	A	PA_11
ETH0_TXCTL_TXEN	ETH0 TXCTL (GigE) or TXEN (10/100)	A	PA_10
ETH0_TXD0	ETH0 Transmit Data 0	A	PA_00
ETH0_TXD1	ETH0 Transmit Data 1	A	PA_01
ETH0_TXD2	ETH0 Transmit Data 2	A	PA_12
ETH0_TXD3	ETH0 Transmit Data 3	A	PA_13
ETH0_TXEN	ETH0 Transmit Enable	A	PA_10
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VIN4	HADC0 Analog Input at channel 4	Not Muxed	HADC0_VIN4

GPIO MULTIPLEXING FOR THE 529-BALL CSP_BGA PACKAGE

Table 20 through Table 26 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 529-ball CSP_BGA package.

Table 20. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	ETH0_TXD0			SMC0_A21	
PA_01	ETH0_TXD1			SMC0_A20	
PA_02	ETH0_MDC			SMC0_A24	
PA_03	ETH0_MDIO			SMC0_A23	
PA_04	ETH0_RXD0			SMC0_A19	
PA_05	ETH0_RXD1			SMC0_A18	
PA_06	ETH0_RXCLK_REFCLK			SMC0_A17	
PA_07	ETH0_CRS			SMC0_A16	
PA_08	ETH0_RXD2			SMC0_A12	
PA_09	ETH0_RXD3			SMC0_A11	
PA_10	ETH0_TXEN			SMC0_A22	
PA_11	ETH0_TXCLK			SMC0_A15	
PA_12	ETH0_TXD2			SMC0_A14	
PA_13	ETH0_TXD3			SMC0_A13	
PA_14	ETH0_PTPPPS3	SINC0_D0		SMC0_A10	
PA_15	ETH0_PTPPPS2	SINC0_D1		SMC0_A09	

Table 21. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_PTPPPS1	SINC0_D2	PPI0_D14	SMC0_A08	TM0_ACLK3
PB_01	ETH0_PTPPPS0	SINC0_CLK0	PPI0_D15	SMC0_A07	TM0_ACLK4
PB_02	ETH0_PTPCLKIN0	$\overline{\text{UART1\_TX}}$	PPI0_D16	SMC0_A04	
PB_03	ETH0_PTPAUXIN0	$\overline{\text{UART1\_RX}}$	PPI0_D17	SMC0_A03	TM0_ACI1
PB_04	MLB0_CLK	SINC0_D3	PPI0_D12	SMC0_ARDY	ETH0_PTPAUXIN1
PB_05	MLB0_SIG		PPI0_D13	SMC0_A01	ETH0_PTPAUXIN2
PB_06	MLB0_DAT		PWM0_BH	SMC0_A02	ETH0_PTPAUXIN3
PB_07	LP1_D0	PWM0_AH	TM0_TMR3	SMC0_D15	
PB_08	LP1_D1	PWM0_AL	TM0_TMR4	SMC0_D14	
PB_09	LP1_D2		CAN1_TX	SMC0_D13	
PB_10	LP1_D3	TM0_TMR2	CAN1_RX	SMC0_D12	TM0_ACI4
PB_11	LP1_D4		PWM0_DH	SMC0_D11	CNT0_ZM
PB_12	LP1_D5		PWM0_DL	SMC0_D10	CNT0_UD
PB_13	LP1_D6		PWM0_CH	SMC0_D09	
PB_14	LP1_D7	TM0_TMR5	PWM0_CL	SMC0_D08	CNT0_DG
PB_15	LP1_ACK	$\overline{\text{PWM0\_TRIP0}}$	TM0_TMR1	$\overline{\text{SMC0\_AWE}}$	

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 2 | EMAC0 Management Channel Clock | SMC0 Address 24 Notes: No notes
PA_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 3 | EMAC0 Management Channel Serial Data | SMC0 Address 23 Notes: No notes
PA_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 4 | EMAC0 Receive Data 0 | SMC0 Address 19 Notes: No notes
PA_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 5 | EMAC0 Receive Data 1 | SMC0 Address 18 Notes: No notes
PA_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 6 | EMAC0 RXCLK (GigE) or REFCLK (10/100) | SMC0 Address 17 Notes: No notes
PA_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 RXCTL (GigE) or CRS (10/100) | PORTA Position 7 | EMAC0 Carrier Sense/RMII Receive Data Valid | SMC0 Address 16 Notes: No notes
PA_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 8 | EMAC0 Receive Data 2 | SMC0 Address 12 Notes: No notes
PA_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 9 | EMAC0 Receive Data 3 | SMC0 Address 11 Notes: No notes
PA_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 TXCTL (GigE) or TXEN (10/100) | PORTA Position 10 | EMAC0 Transmit Enable | SMC0 Address 22 Notes: No notes
PA_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 11 | EMAC0 Transmit Clock | SMC0 Address 15 Notes: No notes
PA_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 12 | EMAC0 Transmit Data 2 | SMC0 Address 14 Notes: No notes
PA_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 13 | EMAC0 Transmit Data 3 | SMC0 Address 13 Notes: No notes
PA_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 14 | EMAC0 PTP Pulse-Per-Second Output 3 | SINC0 Data 0 | SMC0 Address 10 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
USB_XTAL	a		none	none	none		Desc: USB0/USB1 Crystal Notes: Services both USB0 and USB1
VDD_DMC	s	NA	none	none	none		Desc: DMC VDD Notes: No notes
VDD_EXT	s	NA	none	none	none		Desc: External Voltage Domain Notes: No notes
VDD_HADC	s	NA	none	none	none		Desc: HADC VDD Notes: No notes
VDD_INT	s	NA	none	none	none		Desc: Internal Voltage Domain Notes: No notes
VDD_PCIE	s	NA	none	none	none		Desc: PCIE Supply Voltage Notes: Connect to GND if not used[1]
VDD_PCIE_RX	s	NA	none	none	none		Desc: PCIE RX Supply Voltage Notes: Connect to GND if not used[1]
VDD_PCIE_TX	s	NA	none	none	none		Desc: PCIE TX Supply Voltage Notes: Connect to GND if not used[1]
VDD_RTC	s	NA	none	none	none		Desc: RTC VDD Notes: No notes
VDD_USB	s	NA	none	none	none		Desc: USB VDD Notes: Connect to VDD_EXT when USB is not used

[1] Guidance also applies to models that do not feature the associated hardware block. See Table 2 or Table 3 for further information.

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	450 MHz Min	450 MHz Typ	450 MHz Max	Unit
V_{OH}[1]	High Level Output Voltage	At V_{DD_EXT} = minimum, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	At V_{DD_EXT} = minimum, I_{OL} = 1.0 mA[2]			0.4	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_LPDDR}[5]	High Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OH} = –6.0 mA	1.38			V
V_{OL_LPDDR}[5]	Low Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OL} = 6.0 mA			0.32	V
I_{IH}[6, 7]	High Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			10	µA
I_{IL}[6]	Low Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = 0 V			10	µA
I_{IL_PU}[7]	Low Level Input Current Pull-up	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{IH_PD}[8]	High Level Input Current Pull-down	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{OZH}[9]	Three-State Leakage Current	At V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = V_{DD_EXT}/V_{DD_DDR} maximum			10	µA
I_{OZL}[9]	Three-State Leakage Current	at V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = 0 V			10	µA
C_{IN}[10]	Input Capacitance	T_{CASE} = 25°C			5	pF

Clock and Reset Timing

Table 44 and Figure 11 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLK, DCLK, and OCLK timing specifications in Table 29, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 44. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKINx Frequency (Crystal)[1, 2, 3]	20	50	MHz
	SYS_CLKINx Frequency (External CLKIN)[1, 2, 3]	20	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 11) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 43 and Figure 10 for power-up reset timing.

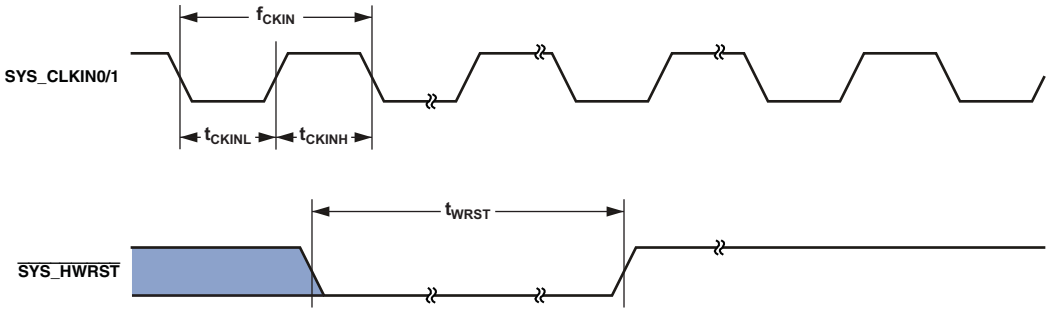

Figure 11. Clock and Reset Timing

DDR3 SDRAM Read Cycle Timing

Table 58 and Figure 24 show mobile DDR3 SDRAM read cycle timing, related to the DMC.

Table 58. DDR3 SDRAM Read Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	Max	Unit
Timing Requirements				
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQ Signals		0.2	ns
t_{QH}	DMCx_DQ, DMCx_DQS Output Hold Time From DMCx_DQS	0.38		t_{CK}
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.3		t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

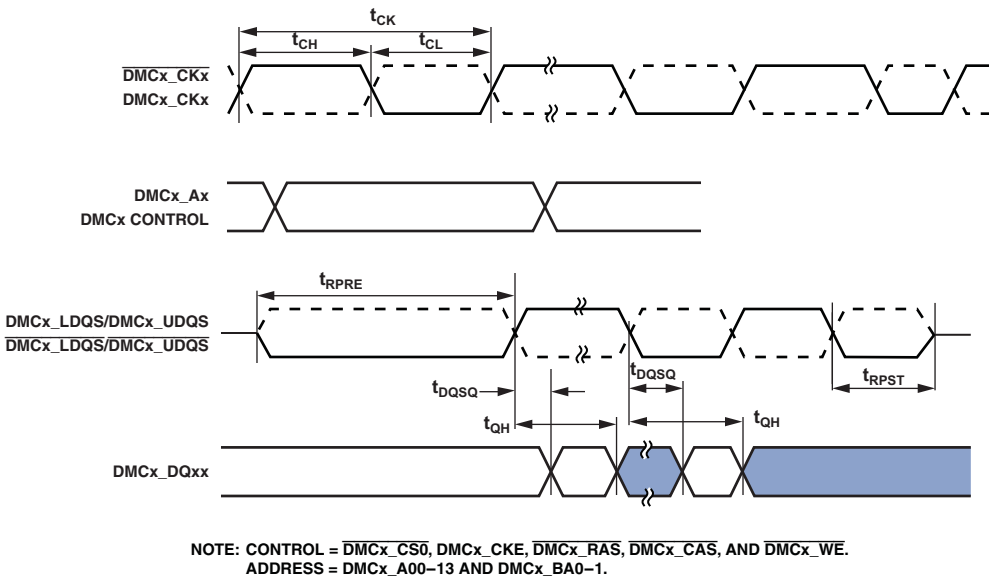

Figure 24. DDR3 SDRAM Controller Input AC Timing

DDR3 SDRAM Write Cycle Timing

Table 59 and Figure 25 show mobile DDR3 SDRAM output ac timing, related to the DMC.

Table 59. DDR3 SDRAM Write Cycle Timing VDD_DMCx Nominal 1.5 V[1]

Parameter		450 MHz[2] Min	450 MHz[2] Max	Unit
Switching Characteristics				
t_{DQSS}	DMCx_DQS Latching Rising Transitions to Associated Clock Edges[3]	–0.25	0.25	t_{CK}
t_{DS}	Last Data Valid to DMCx_DQS Delay (Slew > 1 V/ns)	0.125		ns
t_{DH}	DMCx_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.150		ns
t_{DSS}	DMCx_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMCx_DQS Falling Edge Hold Time From DMCx_CK	0.2		t_{CK}
t_{DQSH}	DMCx_DQS Input High Pulse Width	0.45	0.55	t_{CK}
t_{DQSL}	DMCx_DQS Input Low Pulse Width	0.45	0.55	t_{CK}
t_{WPRE}	Write Preamble	0.9		t_{CK}
t_{WPST}	Write Postamble	0.3		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.840		ns
t_{DIPW}	DMCx_DQ and DMCx_DM Output Pulse Width	0.550		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of the DDR3, all the DDR3 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] Write command to first DMCx_DQS delay = WL × t_{CK} + t_{DQSS}.

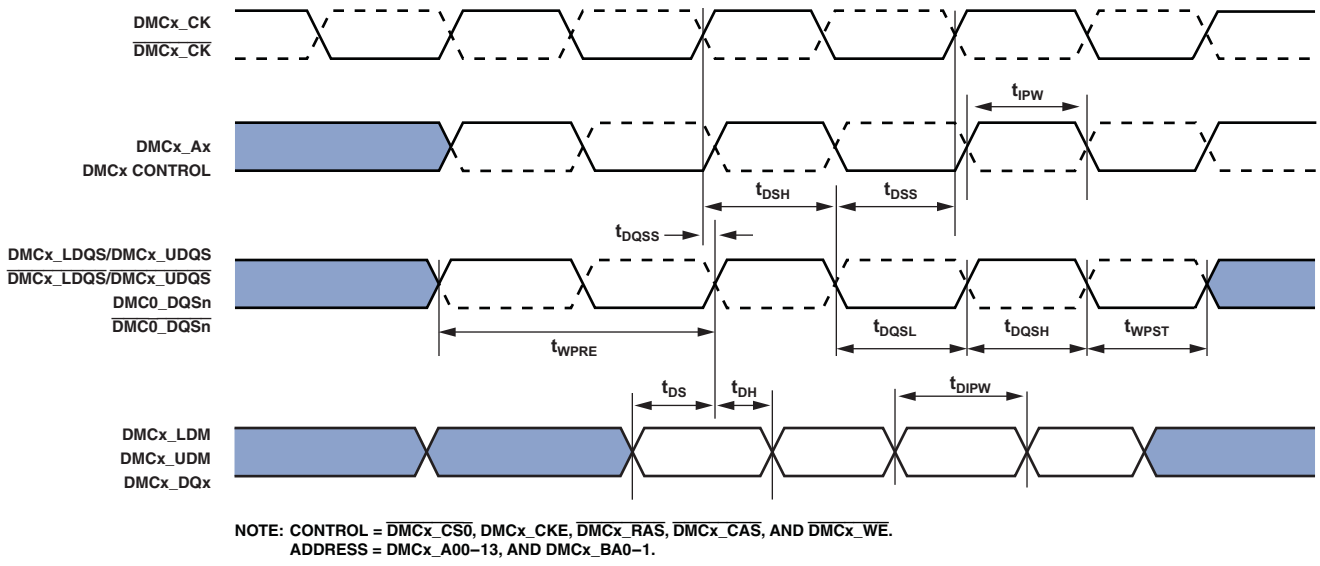

Figure 25. DDR3 SDRAM Controller Output AC Timing

Enhanced Parallel Peripheral Interface (EPPI) Timing

Table 60 and Table 61 and Figure 26 through Figure 34 describe enhanced parallel peripheral interface (EPPI) timing operations. In Figure 26 through Figure 34, POLC[1:0] represents the setting of the EPPI_CTL register, which sets the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated, the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 60. Enhanced Parallel Peripheral Interface (EPPI)—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	0		ns
Switching Characteristics				
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 1.5$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 1.5$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		3.5	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–0.5		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		3.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–0.5		ns

[1] See Table 29 for details on the minimum period that can be programmed for $t_{PCLKPROG}$.

Serial Ports (SPORT)

To determine whether a device is compatible with the SPORT at clock speed n, the following specifications must be confirmed: frame sync delay and frame sync setup and hold; data delay and data setup and hold; and serial clock (SPTx_CLK) width. In Figure 37, either the rising edge or the falling edge of SPTx_CLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK0}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 64. Serial Ports—External Clock[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	Frame Sync Setup Before SPTx_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[2]	2		ns
t_{HFSE}	Frame Sync Hold After SPTx_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[2]	2.7		ns
t_{SDRE}	Receive Data Setup Before Receive SPTx_CLK[2]	2		ns
t_{HDRE}	Receive Data Hold After SPTx_CLK[2]	2.7		ns
$t_{SPTCLKW}$	SPTx_CLK Width[3]	$0.5 \times t_{SPTCLKEXT} - 1.5$		ns
t_{SPTCLK}	SPTx_CLK Period[3]	$t_{SPTCLKEXT} - 1.5$		ns
Switching Characteristics				
t_{DFSE}	Frame Sync Delay After SPTx_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[4]		14.5	ns
t_{HOFSE}	Frame Sync Hold After SPTx_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[4]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPTx_CLK[4]		14	ns
t_{HDTE}	Transmit Data Hold After Transmit SPTx_CLK[4]	2		ns

[1] Specifications apply to all eight SPORTs.
[2] Referenced to sample edge.
[3] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPTx_CLK. For the external SPTx_CLK ideal maximum frequency see the $f_{SPTCLKEXT}$ specification in Table 29.
[4] Referenced to drive edge.

Table 68. Serial Ports—External Late Frame Sync[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0[2]		14	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[2]	0.5		ns

[1] Specifications apply to all eight SPORTs.
[2] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left justified as well as standard serial mode and MCE = 1, MFD = 0.

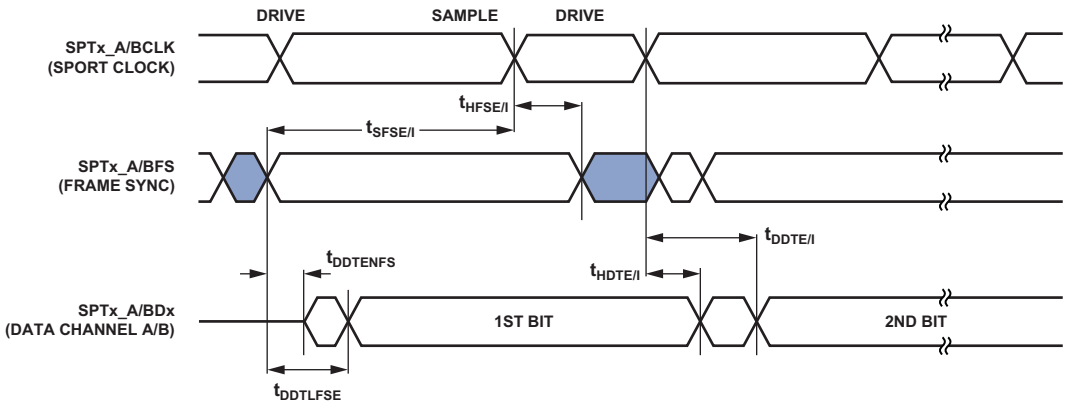

Figure 40. External Late Frame Sync

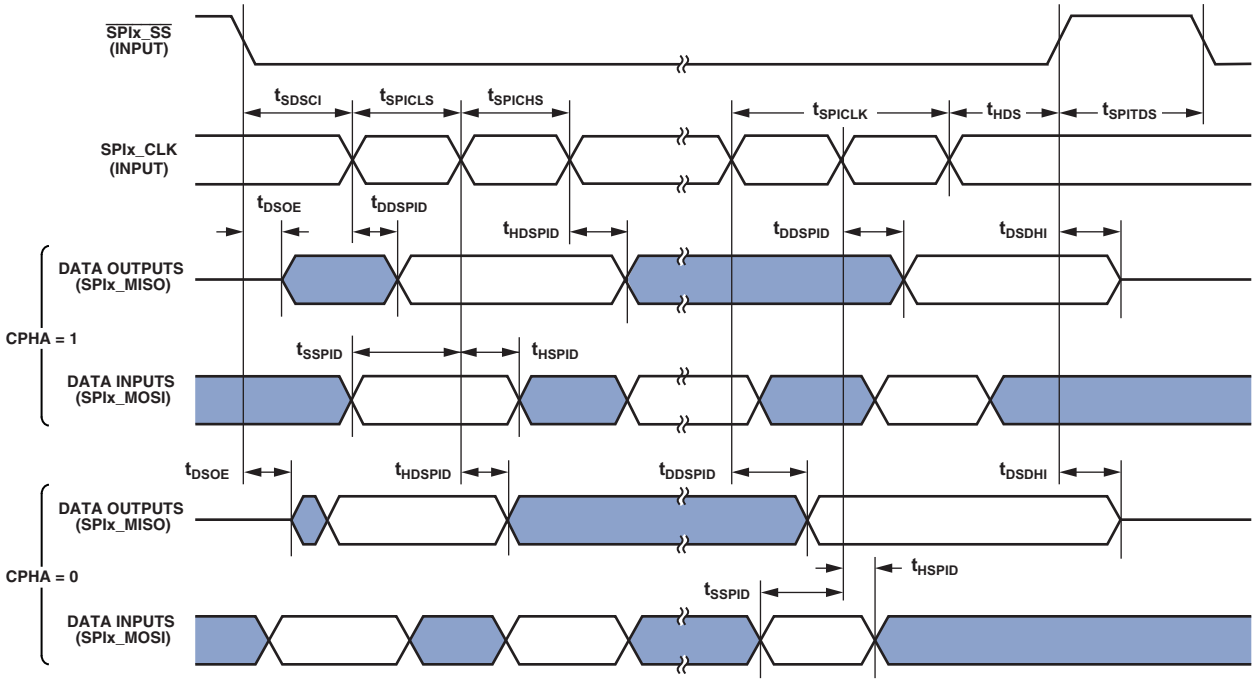

Figure 44. SPI Port—Slave Timing

SPI Port—Open Drain Mode (ODM) Timing

In Figure 46 and Figure 47 and Table 75 and Table 76, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3 depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 74. SPI Port ODM Master Mode Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance from Data Out Valid	–1		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid from High Impedance	–1	+6	ns

[1] All specifications apply to all three SPIs.

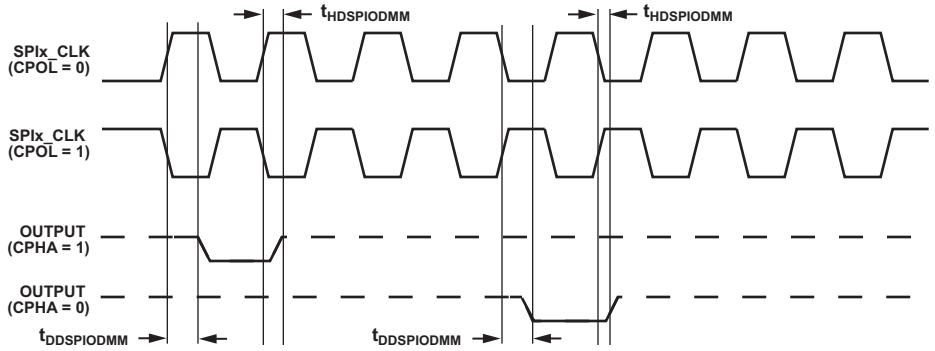

Figure 46. ODM Master Mode

Table 75. SPI Port—ODM Slave Mode[1]

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

[1] All specifications apply to all three SPIs.

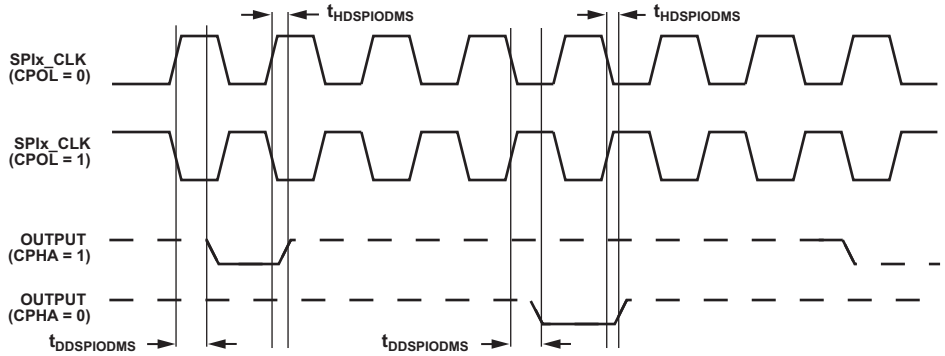

Figure 47. ODM Slave Mode

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 76. SPI Port—SPIx_RDY Master Timing[1]

Parameter		Conditions	Min	Max	Unit
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	Baud = 0, CPHA = 0	$4.5 \times t_{SCLK1}$	$5.5 \times t_{SCLK1} + 10$	ns
		Baud = 0, CPHA = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 0	$(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 1	$(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

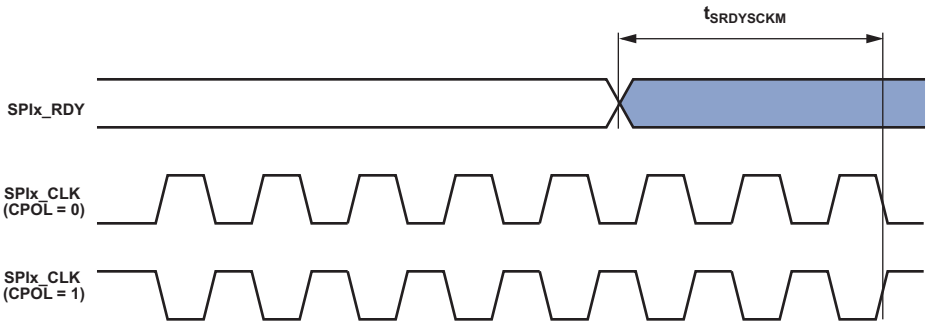

Figure 48. SPIx_RDY Setup Before SPIx_CLK

Program Trace Macrocell (PTM) Timing

Table 102 and Figure 75 provide I/O timing related to the PTM.

Table 102. Trace Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTRD}	Trace Data Delay From Trace Clock Maximum		5	ns
t_{HTRD}	Trace Data Hold From Trace Clock Minimum	2		ns
t_{PTRCK}	Trace Clock Period Minimum	12.32		ns

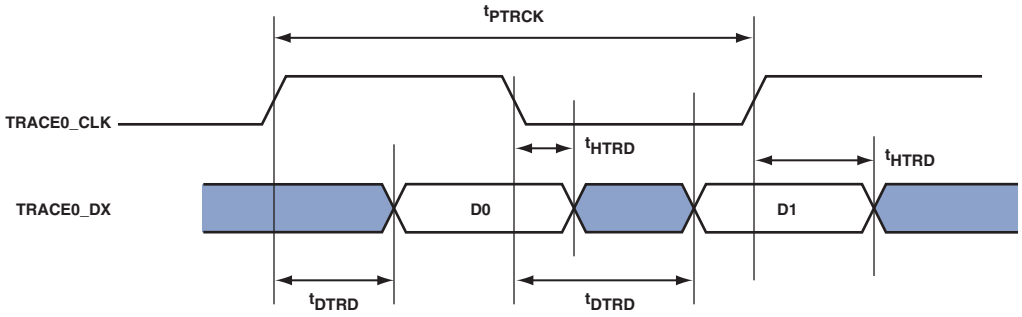

Figure 75. Trace Timing

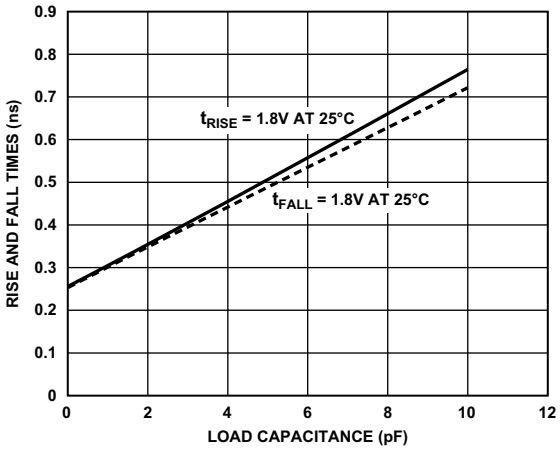

Figure 96. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for DDR2

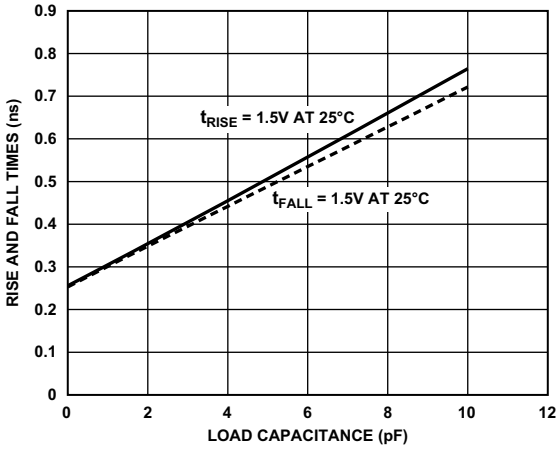

Figure 97. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.5 V) for DDR3

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured at top center of package.
Ψ_{JT} = from Table 104 and Table 105.
P_D = power dissipation (see the Total Internal Power Dissipation section for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 104 and Table 105, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 6-layer PCB with 101.6 mm × 152.4 mm dimensions.

Table 104. Thermal Characteristics for 349 CSP_BGA

Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.3	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.65	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.12	°C/W
Ψ_{JT}	2 linear m/s air flow	0.14	°C/W

Table 105. Thermal Characteristics for 529 CSP_BGA

Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.4	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.63	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.11	°C/W
Ψ_{JT}	2 linear m/s air flow	0.13	°C/W

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
T08	GND	V10	VDD_EXT	Y12	HADC0_VIN0	AB14	HADC0_VIN3
T09	GND	V11	VDD_EXT	Y13	HADC0_VIN7	AB15	RTC0_XTAL
T10	GND	V12	HADC0_VIN4	Y14	GND	AB16	MLB0_SIGN
T11	GND	V13	VDD_EXT	Y15	PB_05	AB17	MLB0_DATN
T12	GND	V14	VDD_EXT	Y16	PA_14	AB18	MLB0_CLKN
T13	GND	V15	VDD_EXT	Y17	PA_13	AB19	PA_15
T14	GND	V16	VDD_EXT	Y18	PA_12	AB20	PA_11
T15	GND	V17	VDD_EXT	Y19	PA_10	AB21	PA_06
T16	GND	V18	VDD_EXT	Y20	PA_00	AB22	PA_04
T17	GND	V19	VDD_INT	Y21	DAI1_PIN14	AB23	PA_02
T18	VDD_EXT	V20	DAI1_PIN16	Y22	DAI1_PIN17	AC01	GND
T19	VDD_INT	V21	DAI1_PIN06	Y23	DAI1_PIN15	AC02	PCIE0_RXP
T20	DAI1_PIN03	V22	DAI1_PIN12	AA01	PB_08	AC03	PCIE0_RXM
T21	PG_03	V23	DAI1_PIN09	AA02	PB_07	AC04	PCIE0_CLKM
T22	PG_02	W01	PB_12	AA03	DAI0_PIN16	AC05	PCIE0_CLKP
T23	DAI1_PIN01	W02	PB_09	AA04	DAI0_PIN07	AC06	PCIE0_TXP
U01	SYS_XTAL0	W03	DAI0_PIN18	AA05	DAI0_PIN06	AC07	PCIE0_TXM
U02	$\overline{\text{SYS\_RESOUT}}$	W04	DAI0_PIN11	AA06	DAI0_PIN01	AC08	USB1_DM
U03	PC_00	W05	VDD_INT	AA07	PCIE0_REF	AC09	USB1_DP
U04	DAI0_PIN20	W06	VDD_INT	AA08	USB1_VBUS	AC10	USB0_DP
U05	VDD_INT	W07	VDD_PCIE	AA09	USB0_VBUS	AC11	USB0_DM
U06	VDD_EXT	W08	VDD_INT	AA10	TWI1_SCL	AC12	HADC0_VREFP
U07	GND	W09	VDD_INT	AA11	TWI1_SDA	AC13	VDD_HADC
U08	GND	W10	VDD_INT	AA12	HADC0_VIN1	AC14	GND
U09	GND	W11	VDD_INT	AA13	HADC0_VIN5	AC15	RTC0_CLKIN
U10	GND	W12	HADC0_VIN6	AA14	PB_06	AC16	MLB0_SIGP
U11	GND	W13	VDD_INT	AA15	PB_02	AC17	MLB0_DATP
U12	GND	W14	VDD_RTC	AA16	PB_04	AC18	MLB0_CLKP
U13	GND	W15	VDD_INT	AA17	PB_03	AC19	PB_01
U14	GND	W16	VDD_INT	AA18	PB_00	AC20	PA_07
U15	GND	W17	VDD_INT	AA19	PA_09	AC21	PA_08
U16	GND	W18	VDD_INT	AA20	PA_05	AC22	PA_03
U17	GND	W19	VDD_INT	AA21	PA_01	AC23	GND
U18	VDD_EXT	W20	DAI1_PIN20	AA22	DAI1_PIN19		
U19	DAI1_PIN08	W21	DAI1_PIN11	AA23	DAI1_PIN18		
U20	DAI1_PIN07	W22	DAI1_PIN10	AB01	DAI0_PIN15		
U21	DAI1_PIN04	W23	DAI1_PIN13	AB02	DAI0_PIN14		
U22	DAI1_PIN05	Y01	PB_11	AB03	DAI0_PIN09		
U23	DAI1_PIN02	Y02	PB_10	AB04	DAI0_PIN13		
V01	SYS_CLKIN0	Y03	DAI0_PIN17	AB05	DAI0_PIN04		
V02	PB_13	Y04	DAI0_PIN08	AB06	DAI0_PIN02		
V03	DAI0_PIN19	Y05	DAI0_PIN05	AB07	DAI0_PIN03		
V04	DAI0_PIN12	Y06	DAI0_PIN10	AB08	USB_XTAL		
V05	VDD_INT	Y07	USB0_ID	AB09	USB_CLKIN		
V06	VDD_EXT	Y08	VDD_USB	AB10	TWI2_SCL		
V07	VDD_PCIE_RX	Y09	USB0_VBC	AB11	TWI0_SDA		
V08	VDD_PCIE_TX	Y10	TWI0_SCL	AB12	HADC0_VREFN		
V09	VDD_EXT	Y11	TWI2_SDA	AB13	HADC0_VIN2		