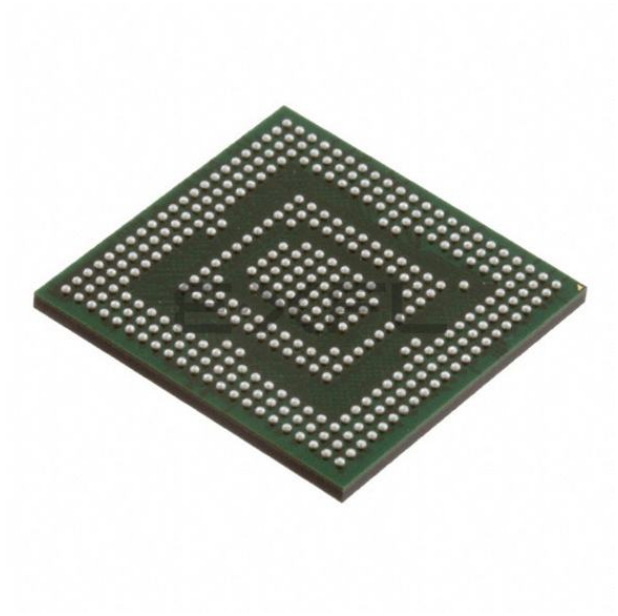

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc582kbcz-4a

Table 2. Comparison of ADSP-SC58x/ADSP-2158x Processor Features

Processor Feature		ADSP-SC582	ADSP-SC583	ADSP-SC584	ADSP-SC587	ADSP-SC589	ADSP-21583	ADSP-21584	ADSP-21587
ARM Cortex-A5 (MHz, Max)		450	450	450	450	450	N/A	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	32, 32	N/A	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	256	N/A	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	640	384	640	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1 Controller (16-bit)	1	1	1	2	2	1	1	2
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	1	N/A	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
10/100/1000 /AVB EMAC + Timer IEEE 1588		1	1	1	1	1	N/A	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	1	N/A	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	1	N/A	N/A	N/A
RTC		N/A	N/A	N/A	1	1	N/A	N/A	1
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to G	Port A to E	Port A to E	Port A to G
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	102 + 40	80 + 28	80 + 28	102 + 40
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	529-BGA	349-BGA	349-BGA	529-BGA

Table 3. Comparison of ADSP-SC58x/ADSP-2158x Processor Features for Automotive

Processor Feature		ADSP-SC582W	ADSP-SC583W	ADSP-SC584W	ADSP-SC587W	ADSP-21583W	ADSP-21584W
ARM Cortex-A5 (MHz, Max)		450	450	450	450	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	450	450	450	450	450
SHARC+ Core2 (MHz, Max)		N/A	450	450	450	450	450
SHARC L1 SRAM/Core (kB)		640	384	640	640	384	640
System Memory	L2 SRAM (Shared) (kB)	256	256	256	256	256	256
	L2 ROM (Shared) (kB)	512	512	512	512	512	512
	DDR3/DDR2/LPDDR1 Controller (16-bit)	1	1	1	2	1	1
USB 2.0 HS + PHY (Host/Device/OTG)		1	1	1	1	N/A	N/A
USB 2.0 HS + PHY (Host/Device)		N/A	N/A	N/A	1	N/A	N/A
10/100 Std EMAC		N/A	N/A	N/A	1	N/A	N/A
10/100/1000/AVB EMAC + Timer IEEE 1588		1	1	1	1	N/A	N/A
SDIO/eMMC		N/A	N/A	N/A	1	N/A	N/A
PCIe 2.0 (1 Lane)		N/A	N/A	N/A	N/A	N/A	N/A
MLB 3-Pin/6-Pin		1	1	1	1	1	1
RTC		N/A	N/A	N/A	1	N/A	N/A
GPIO Ports		Port A to E	Port A to E	Port A to E	Port A to G	Port A to E	Port A to E
GPIO + DAI Pins		80 + 28	80 + 28	80 + 28	102 + 40	80 + 28	80 + 28
19 mm × 19 mm Package Options		349-BGA	349-BGA	349-BGA	529-BGA	349-BGA	349-BGA

The processing elements are referred to as PEx and PEy data registers and each contain an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

Single instruction multiple data (SIMD) mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also affects the way data transfers between memory and processing elements because to sustain computational operation in the processing elements requires twice the data bandwidth. Therefore, entering SIMD mode doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values transfer with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, arithmetic/logic unit (ALU), and shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, IEEE 64-bit double-precision floating-point, and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

Core Timer

Each SHARC+ processor core also has a timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, while control bits in MODE1 activate the secondary registers.

Universal Registers (USTAT)

General-purpose tasks use the universal registers. The four USTAT registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-SC58x/ADSP-2158x processor uses the two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set Architecture (ISA)

The ISA, a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction. Additionally, the double-precision floating-point instruction set is an addition to the SHARC+ core.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the SHARC+ core processors support 16-bit and 32-bit opcodes for many instructions, formerly 48-bit in the ISA. This feature, called variable instruction set architecture (VISA), drops redundant or unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external memories. VISA is not an operating mode; it is only address dependent (refer to memory map ISA/VISA address spaces in Table 7). Furthermore, it allows jumps between ISA and VISA instruction fetches.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART1_RTS	UART1 Request to Send	E	PE_02
UART1_RX	UART1 Receive	B	PB_03
UART1_TX	UART1 Transmit	B	PB_02
UART2_CTS	UART2 Clear to Send	E	PE_11
UART2_RTS	UART2 Request to Send	E	PE_10
UART2_RX	UART2 Receive	D	PD_13
UART2_TX	UART2 Transmit	D	PD_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Negative Data (–)	Not Muxed	USB0_DM
USB0_DP	USB0 Positive Data (+)	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_CK	DMC0 Clock (complement)	Not Muxed	DMC0_CK
DMC0_CS0	DMC0 Chip Select 0	Not Muxed	DMC0_CS0
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
DMC0_LDQS	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	DMC0_LDQS
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
DMC0_RAS	DMC0 Row Address Strobe	Not Muxed	DMC0_RAS
DMC0_RESET	DMC0 Reset (DDR3 only)	Not Muxed	DMC0_RESET
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
DMC0_UDQS	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	DMC0_UDQS
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
DMC0_WE	DMC0 Write Enable	Not Muxed	DMC0_WE
DMC1_A00	DMC1 Address 0	Not Muxed	DMC1_A00
DMC1_A01	DMC1 Address 1	Not Muxed	DMC1_A01
DMC1_A02	DMC1 Address 2	Not Muxed	DMC1_A02
DMC1_A03	DMC1 Address 3	Not Muxed	DMC1_A03
DMC1_A04	DMC1 Address 4	Not Muxed	DMC1_A04
DMC1_A05	DMC1 Address 5	Not Muxed	DMC1_A05
DMC1_A06	DMC1 Address 6	Not Muxed	DMC1_A06
DMC1_A07	DMC1 Address 7	Not Muxed	DMC1_A07
DMC1_A08	DMC1 Address 8	Not Muxed	DMC1_A08
DMC1_A09	DMC1 Address 9	Not Muxed	DMC1_A09
DMC1_A10	DMC1 Address 10	Not Muxed	DMC1_A10
DMC1_A11	DMC1 Address 11	Not Muxed	DMC1_A11
DMC1_A12	DMC1 Address 12	Not Muxed	DMC1_A12
DMC1_A13	DMC1 Address 13	Not Muxed	DMC1_A13
DMC1_A14	DMC1 Address 14	Not Muxed	DMC1_A14
DMC1_A15	DMC1 Address 15	Not Muxed	DMC1_A15
DMC1_BA0	DMC1 Bank Address 0	Not Muxed	DMC1_BA0
DMC1_BA1	DMC1 Bank Address 1	Not Muxed	DMC1_BA1

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_AMS2	SMC0 Memory Select 2	C	PC_07
SMC0_AMS3	SMC0 Memory Select 3	C	PC_08
SMC0_AOE	SMC0 Output Enable	D	PD_01
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_04
SMC0_ARE	SMC0 Read Enable	C	PC_00
SMC0_AWE	SMC0 Write Enable	B	PB_15
SMC0_D00	SMC0 Data 0	E	PE_12
SMC0_D01	SMC0 Data 1	E	PE_11
SMC0_D02	SMC0 Data 2	E	PE_10
SMC0_D03	SMC0 Data 3	E	PE_09
SMC0_D04	SMC0 Data 4	E	PE_00
SMC0_D05	SMC0 Data 5	D	PD_15
SMC0_D06	SMC0 Data 6	D	PD_14
SMC0_D07	SMC0 Data 7	D	PD_00
SMC0_D08	SMC0 Data 8	B	PB_14
SMC0_D09	SMC0 Data 9	B	PB_13
SMC0_D10	SMC0 Data 10	B	PB_12
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_10
SMC0_D13	SMC0 Data 13	B	PB_09
SMC0_D14	SMC0 Data 14	B	PB_08
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_10
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_11
SPI0_RDY	SPI0 Ready	C	PC_12
SPI0_SEL1	SPI0 Slave Select Output 1	C	PC_07
SPI0_SEL2	SPI0 Slave Select Output 2	D	PD_01
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_12
SPI0_SEL4	SPI0 Slave Select Output 4	C	PC_00
SPI0_SEL5	SPI0 Slave Select Output 5	E	PE_01
SPI0_SEL6	SPI0 Slave Select Output 6	E	PE_02
SPI0_SEL7	SPI0 Slave Select Output 7	E	PE_03
SPI0_SS	SPI0 Slave Select Input	D	PD_01
SPI1_CLK	SPI1 Clock	E	PE_13
SPI1_MISO	SPI1 Master In, Slave Out	E	PE_14
SPI1_MOSI	SPI1 Master Out, Slave In	E	PE_15
SPI1_RDY	SPI1 Ready	E	PE_08
SPI1_SEL1	SPI1 Slave Select Output 1	C	PC_13
SPI1_SEL2	SPI1 Slave Select Output 2	E	PE_07
SPI1_SEL3	SPI1 Slave Select Output 3	E	PE_11
SPI1_SEL4	SPI1 Slave Select Output 4	E	PE_12
SPI1_SEL5	SPI1 Slave Select Output 5	E	PE_08
SPI1_SEL6	SPI1 Slave Select Output 6	F	PF_00
SPI1_SEL7	SPI1 Slave Select Output 7	F	PF_01
SPI1_SS	SPI1 Slave Select Input	E	PE_11
SPI2_CLK	SPI2 Clock	C	PC_01
SPI2_D2	SPI2 Data 2	C	PC_04

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TRACE0_D03	TRACE0 Trace Data (first instance)	G	PG_01
TRACE0_D03	TRACE0 Trace Data 3 (second instance)	D	PD_05
TRACE0_D04	TRACE0 Trace Data (first instance)	G	PG_02
TRACE0_D04	TRACE0 Trace Data 4 (second instance)	D	PD_06
TRACE0_D05	TRACE0 Trace Data 5 (first instance)	D	PD_07
TRACE0_D05	TRACE0 Trace Data (second instance)	G	PG_03
TRACE0_D06	TRACE0 Trace Data (first instance)	G	PG_04
TRACE0_D06	TRACE0 Trace Data 6 (second instance)	D	PD_08
TRACE0_D07	TRACE0 Trace Data (first instance)	G	PG_05
TRACE0_D07	TRACE0 Trace Data 7 (second instance)	D	PD_09
TRACE0_D08	TRACE0 Trace Data 8	F	PF_13
TRACE0_D09	TRACE0 Trace Data 9	F	PF_14
TRACE0_D10	TRACE0 Trace Data 10	F	PF_15
TRACE0_D11	TRACE0 Trace Data 11	G	PG_01
TRACE0_D12	TRACE0 Trace Data 12	G	PG_02
TRACE0_D13	TRACE0 Trace Data 13	G	PG_03
TRACE0_D14	TRACE0 Trace Data 14	G	PG_04
TRACE0_D15	TRACE0 Trace Data 15	G	PG_05
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_00
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	C	PC_15
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_14
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_13
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	E	PE_01
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	E	PE_02
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_03
$\overline{\text{UART1\_TX}}$	UART1 Transmit	B	PB_02
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	E	PE_11
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	E	PE_10
$\overline{\text{UART2\_RX}}$	UART2 Receive	D	PD_13
$\overline{\text{UART2\_TX}}$	UART2 Transmit	D	PD_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
USB1_DM	USB1 Data -	Not Muxed	USB1_DM
USB1_DP	USB1 Data +	Not Muxed	USB1_DP
USB1_VBUS	USB1 Bus Voltage	Not Muxed	USB1_VBUS
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC VDD	Not Muxed	VDD_HADC

ADSP-SC58X/ADSP-2158X DESIGNER QUICK REFERENCE

Table 27 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are a (analog), s (supply), g (ground) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The int term column specifies the termination present when the processor is not in the reset state.
- The reset term column specifies the termination present when the processor is in the reset state.
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 1 Notes: No notes
DAI0_PIN02	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 2 Notes: No notes
DAI0_PIN03	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 3 Notes: No notes
DAI0_PIN04	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 4 Notes: No notes
DAI0_PIN05	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 5 Notes: No notes
DAI0_PIN06	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 6 Notes: No notes
DAI0_PIN07	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 7 Notes: No notes
DAI0_PIN08	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 8 Notes: No notes
DAI0_PIN09	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 9 Notes: No notes
DAI0_PIN10	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 10 Notes: No notes
DAI0_PIN11	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 11 Notes: No notes
DAI0_PIN12	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 12 Notes: No notes
DAI0_PIN13	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 13 Notes: No notes
DAI0_PIN14	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 14 Notes: No notes
DAI0_PIN15	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 15 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC0_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: No notes
DMC0_VREF	a		none	none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: No notes
DMC0_WE	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes
DMC1_A00	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 0 Notes: No notes
DMC1_A01	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 1 Notes: No notes
DMC1_A02	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 2 Notes: No notes
DMC1_A03	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 3 Notes: No notes
DMC1_A04	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 4 Notes: No notes
DMC1_A05	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 5 Notes: No notes
DMC1_A06	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 6 Notes: No notes
DMC1_A07	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 7 Notes: No notes
DMC1_A08	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 8 Notes: No notes
DMC1_A09	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 9 Notes: No notes
DMC1_A10	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 10 Notes: No notes
DMC1_A11	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 11 Notes: No notes
DMC1_A12	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 12 Notes: No notes
DMC1_A13	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 13 Notes: No notes
DMC1_A14	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 14 Notes: No notes
DMC1_A15	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Address 15 Notes: No notes
DMC1_BA0	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 0 Notes: No notes
DMC1_BA1	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 1 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 15 | EMAC0 PTP Pulse-Per-Second Output 2 | SINC0 Data 1 | SMC0 Address 9 Notes: No notes
PB_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 0 | EMAC0 PTP Pulse-Per-Second Output 1 | EPPI0 Data 14 | SINC0 Data 2 | SMC0 Address 8 | TIMER0 Alternate Clock 3 Notes: No notes
PB_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 1 | EMAC0 PTP Pulse-Per-Second Output 0 | EPPI0 Data 15 | SINC0 Clock 0 | SMC0 Address 7 | TIMER0 Alternate Clock 4 Notes: No notes
PB_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 2 | EMAC0 PTP Clock Input 0 | EPPI0 Data 16 | SMC0 Address 4 | UART1 Transmit Notes: No notes
PB_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 3 | EMAC0 PTP Auxiliary Trigger Input 0 | EPPI0 Data 17 | SMC0 Address 3 | UART1 Receive | TIMER0 Alternate Capture Input 1 Notes: No notes
PB_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 4 | EPPI0 Data 12 | MLB0 Single-Ended Clock | SINC0 Data 3 | SMC0 Asynchronous Ready | EMAC0 PTP Auxiliary Trigger Input 1 Notes: No notes
PB_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 5 | EPPI0 Data 13 | MLB0 Single-Ended Signal | SMC0 Address 1 | EMAC0 PTP Auxiliary Trigger Input 2 Notes: No notes
PB_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 6 | MLB0 Single-Ended Data | PWM0 Channel B High Side | SMC0 Address 2 | EMAC0 PTP Auxiliary Trigger Input 3 Notes: No notes
PB_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 7 | LP1 Data 0 | PWM0 Channel A High Side | SMC0 Data 15 | TIMER0 Timer 3 Notes: No notes
PB_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 8 | LP1 Data 1 | PWM0 Channel A Low Side | SMC0 Data 14 | TIMER0 Timer 4 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 9 | CAN1 Transmit | LP1 Data 2 | SMC0 Data 13 Notes: No notes
PB_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 10 | CAN1 Receive | LP1 Data 3 | SMC0 Data 12 | TIMER0 Timer 2 | TIMER0 Alternate Capture Input 4 Notes: No notes
PB_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 11 | LP1 Data 4 | PWM0 Channel D High Side | SMC0 Data 11 | CNT0 Count Zero Marker Notes: No notes
PB_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 12 | LP1 Data 5 | PWM0 Channel D Low Side | SMC0 Data 10 | CNT0 Count Up and Direction Notes: No notes
PB_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 13 | LP1 Data 6 | PWM0 Channel C High Side | SMC0 Data 9 Notes: No notes
PB_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 14 | LP1 Data 7 | PWM0 Channel C Low Side | SMC0 Data 8 | TIMER0 Timer 5 | CNT0 Count Down and Gate Notes: No notes
PB_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTB Position 15 | LP1 Acknowledge | PWM0 Shutdown Input 0 | SMC0 Write Enable | TIMER0 Timer 1 Notes: No notes
PCIE0_CLKM	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK - Notes: No notes
PCIE0_CLKP	Input	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 CLK + Notes: No notes
PCIE0_REF	a	NA	PullDown	none	none	VDD_PCIE	Desc: PCIE0 Reference Notes: No notes
PCIE0_RXM	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX - Notes: No notes
PCIE0_RXP	Input	NA	PullDown	none	none	VDD_PCIE_RX	Desc: PCIE0 RX + Notes: No notes
PCIE0_TXM	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX - Notes: No notes
PCIE0_TXP	InOut	J	PullDown	none	none	VDD_PCIE_TX	Desc: PCIE0 TX + Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 13 | ACM0 ADC Control Signals | SPI1 Slave Select Output 1 | UART0 Transmit Notes: No notes
PC_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 14 | ACM0 ADC Control Signals | UART0 Receive | TIMER0 Alternate Capture Input 0 Notes: No notes
PC_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 15 | ACM0 ADC Control Signals | EPPI0 Frame Sync 3 (FIELD) | SMC0 Memory Select 0 | UART0 Request to Send Notes: No notes
PD_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 0 | ACM0 ADC Control Signals | EPPI0 Data 23 | SMC0 Data 7 | UART0 Clear to Send Notes: No notes
PD_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 1 | ACM0 ADC Control Signals | SMC0 Output Enable | SPI0 Slave Select Output 2 | SPI0 Slave Select Input Notes: No notes
PD_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 2 | LP0 Data 0 | PWM1 Shutdown Input 0 | TRACE0 Trace Data 0 Notes: No notes
PD_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 3 | LP0 Data 1 | PWM1 Channel A High Side | TRACE0 Trace Data 1 Notes: No notes
PD_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 4 | LP0 Data 2 | PWM1 Channel A Low Side | TRACE0 Trace Data 2 Notes: No notes
PD_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 5 | LP0 Data 3 | PWM1 Channel B High Side | TRACE0 Trace Data 3 Notes: No notes
PD_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 6 | LP0 Data 4 | PWM1 Channel B Low Side | TRACE0 Trace Data 4 Notes: No notes
PD_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 7 | LP0 Data 5 | PWM1 Channel C High Side | TRACE0 Trace Data 5 Notes: No notes

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.1	1.15	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_RTC}	RTC Voltage		2.0	3.3	3.60	V
$V_{DD\_PCIE\_TX}$	PCIe Core Transmit Voltage		1.05	1.1	1.15	V
$V_{DD\_PCIE\_RX}$	PCIe Core Receive Voltage		1.05	1.1	1.15	V
V_{DD_PCIE}	PCIe Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = maximum	2.0			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.8	V
$V_{IL\_DDR2/3}$[5]	Low Level Input Voltage	V_{DD_DMC} = minimum			V_{REF} – 0.25	V
$V_{IH\_DDR2/3}$[5]	High Level Input Voltage	V_{DD_DMC} = maximum	V_{REF} + 0.25			V
V_{IL_LPDDR}[6]	Low Level Input Voltage	V_{DD_DMC} = minimum			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[6]	High Level Input Voltage	V_{DD_DMC} = maximum	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		100	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+110	°C
T_J	Junction Temperature 349-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +95°C	–40		+125	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ 0°C to +70°C	0		110	°C
T_J	Junction Temperature 529-Lead CSP_BGA	$T_{AMBIENT}$ –40°C to +85°C	–40		+125	°C
AUTOMOTIVE USE ONLY						
T_J	Junction Temperature 349-Lead CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ –40°C to +105°C	–40		+133[7]	°C

[1] Applies to DDR2/DDR3/LPDDR signals.
[2] If not used, V_{DD_USB} must be connected to 3.3V.
[3] V_{HADC_VREF} must always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional pins except the TWI, DMC, USB, PCIe, and MLB pins.
[5] This parameter applies to all DMC0/1 signals in DDR2/DDR3 mode. V_{REF} is the voltage applied to the V_{REF_DMC} pin, nominally $V_{DD\_DMC/2}$.
[6] This parameter applies to DMC0/1 signals in LPDDR mode.
[7] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Table 28. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_VSEL Selections	V_{DD_EXT} Nominal	V_{BUSTWI}			Unit
		Min	Nominal	Max	
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Table 30. Phase-Locked Loop (PLL) Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	250	900	MHz

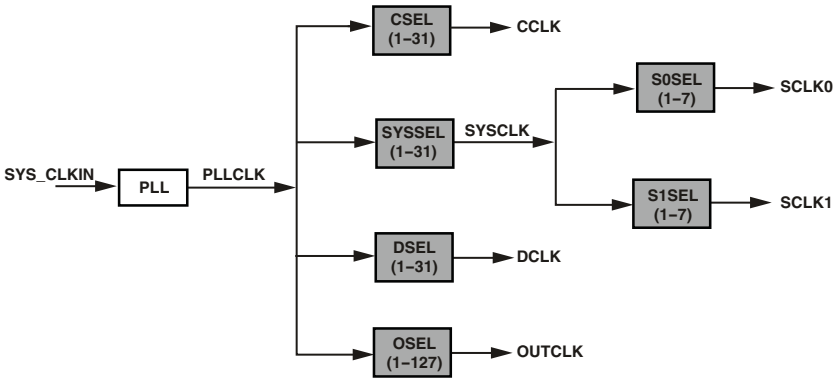

Figure 8. Clock Relationships and Divider Values

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	450 MHz Min	450 MHz Typ	450 MHz Max	Unit
V_{OH}[1]	High Level Output Voltage	At V_{DD_EXT} = minimum, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	At V_{DD_EXT} = minimum, I_{OL} = 1.0 mA[2]			0.4	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR2}[3]	High Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.38			V
V_{OL_DDR2}[3]	Low Level Output Voltage for DDR2 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OH} = –5.8 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 40 Ω	At V_{DD_DDR} = minimum, I_{OL} = 5.8 mA			0.32	V
V_{OH_DDR3}[4]	High Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OH} = –3.4 mA	1.105			V
V_{OL_DDR3}[4]	Low Level Output Voltage for DDR3 DS = 60 Ω	At V_{DD_DDR} = minimum, I_{OL} = 3.4 mA			0.32	V
V_{OH_LPDDR}[5]	High Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OH} = –6.0 mA	1.38			V
V_{OL_LPDDR}[5]	Low Level Output Voltage for LPDDR	At V_{DD_DDR} = minimum, I_{OL} = 6.0 mA			0.32	V
I_{IH}[6, 7]	High Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			10	µA
I_{IL}[6]	Low Level Input Current	At V_{DD_EXT} = maximum, V_{IN} = 0 V			10	µA
I_{IL_PU}[7]	Low Level Input Current Pull-up	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{IH_PD}[8]	High Level Input Current Pull-down	At V_{DD_EXT} = maximum, V_{IN} = 0 V			200	µA
I_{OZH}[9]	Three-State Leakage Current	At V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = V_{DD_EXT}/V_{DD_DDR} maximum			10	µA
I_{OZL}[9]	Three-State Leakage Current	at V_{DD_EXT}/V_{DD_DDR} = maximum, V_{IN} = 0 V			10	µA
C_{IN}[10]	Input Capacitance	T_{CASE} = 25°C			5	pF

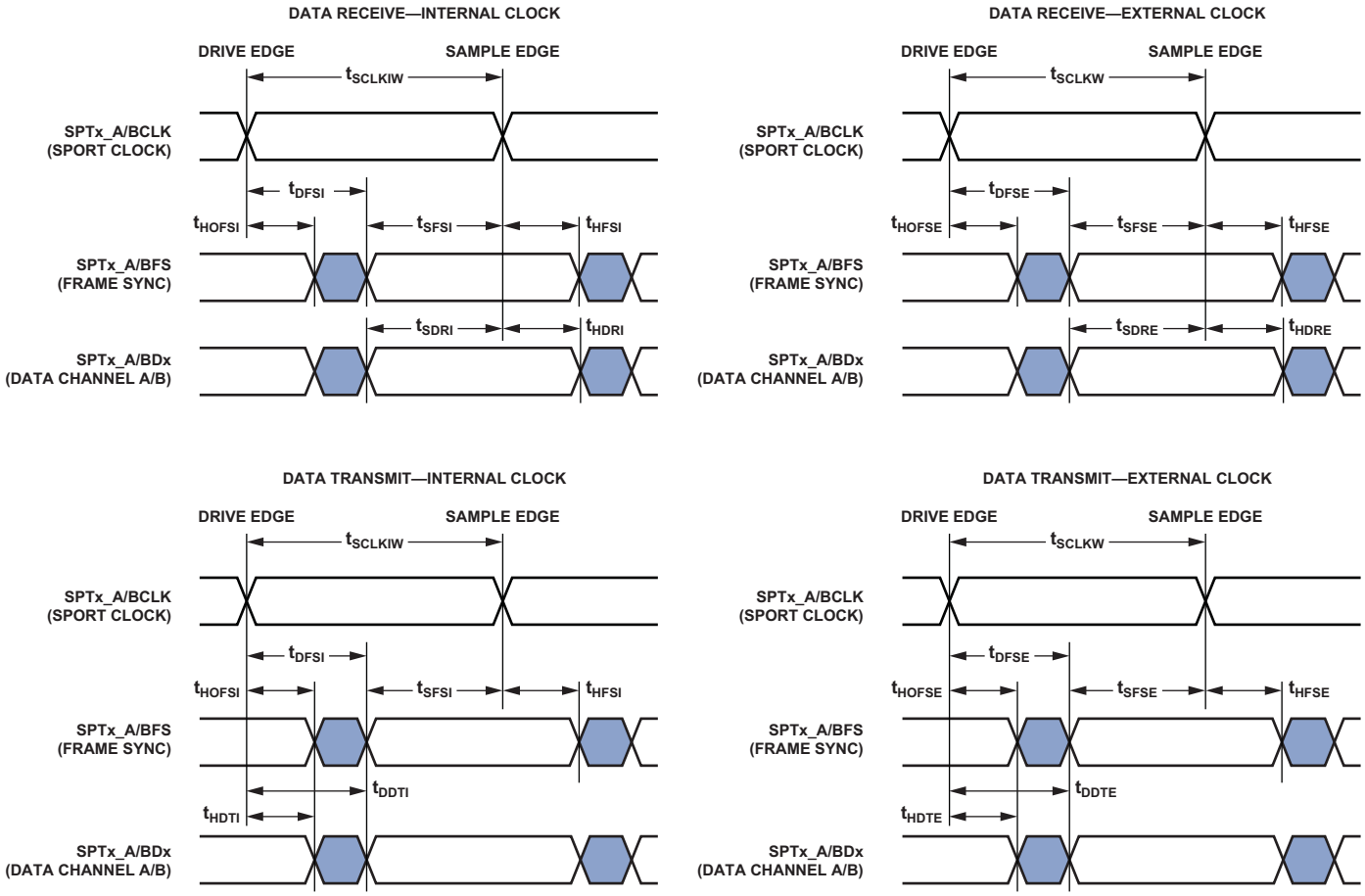

Figure 37. Serial Ports

SPI Port—Open Drain Mode (ODM) Timing

In Figure 46 and Figure 47 and Table 75 and Table 76, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3 depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 74. SPI Port ODM Master Mode Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance from Data Out Valid	–1		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid from High Impedance	–1	+6	ns

[1] All specifications apply to all three SPIs.

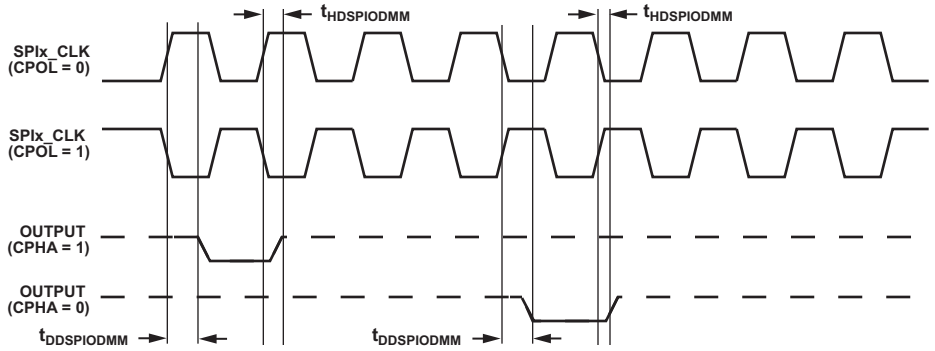

Figure 46. ODM Master Mode

Table 75. SPI Port—ODM Slave Mode[1]

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

[1] All specifications apply to all three SPIs.

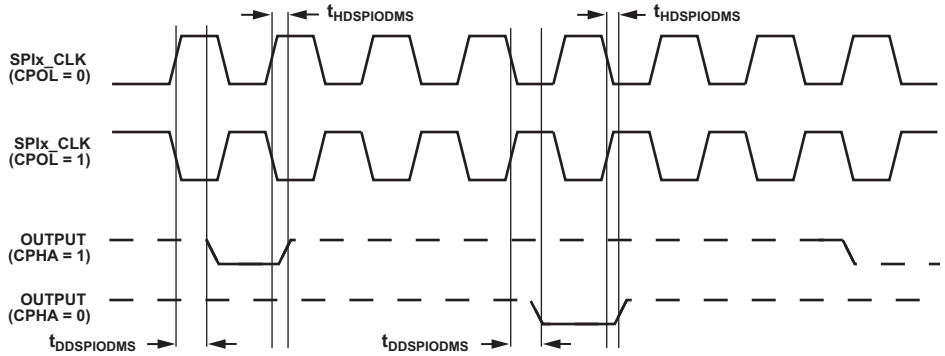

Figure 47. ODM Slave Mode

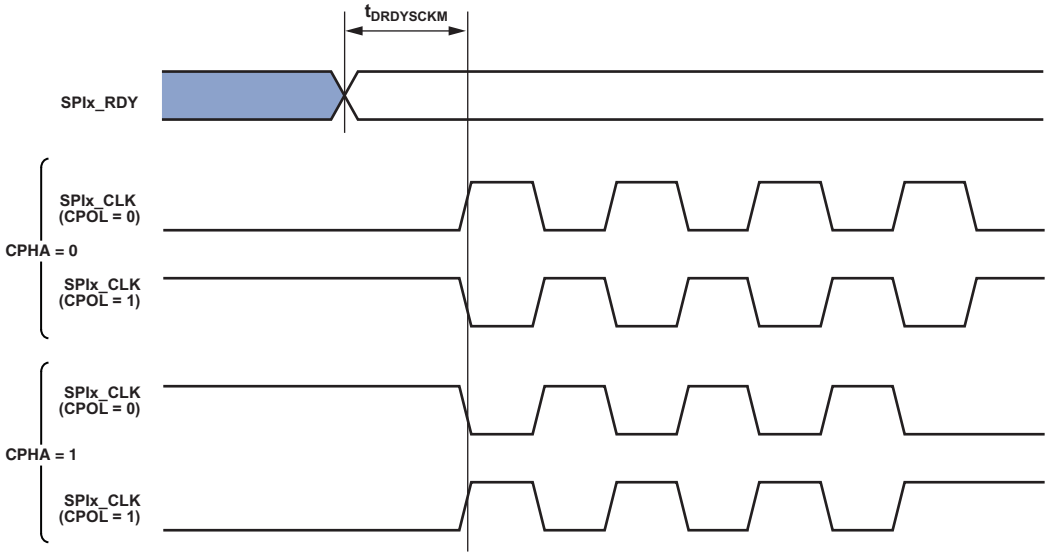

Figure 49. SPIx_CLK Switching Diagram After SPIx_RDY Assertion

Precision Clock Generator (PCG) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes inputs directly from the DAI pins (via pin buffers) and sends outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAIx_PINx).

Table 77. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{SCLK} \times 2$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	13.5	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$13.5 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$[1]	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$13.5 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[2]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

[1] D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.
[2] Normal mode of operation.

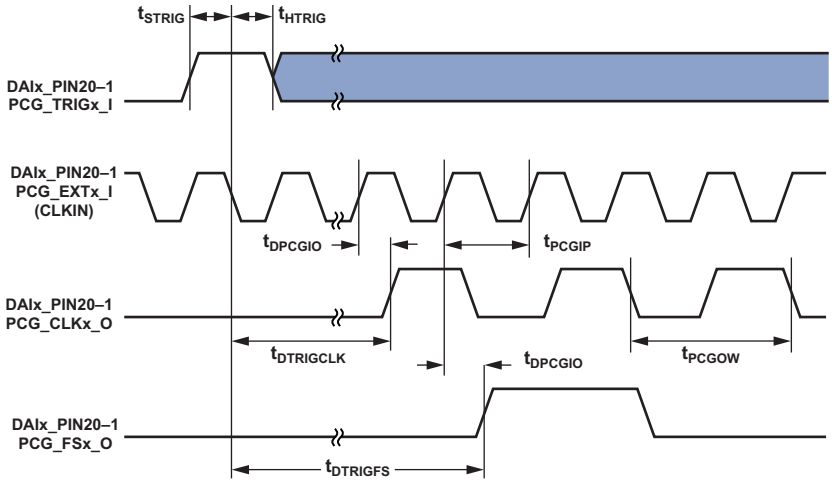

Figure 50. PCG (Direct Pin Routing)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
T08	GND	V10	VDD_EXT	Y12	HADC0_VIN0	AB14	HADC0_VIN3
T09	GND	V11	VDD_EXT	Y13	HADC0_VIN7	AB15	RTC0_XTAL
T10	GND	V12	HADC0_VIN4	Y14	GND	AB16	MLB0_SIGN
T11	GND	V13	VDD_EXT	Y15	PB_05	AB17	MLB0_DATN
T12	GND	V14	VDD_EXT	Y16	PA_14	AB18	MLB0_CLKN
T13	GND	V15	VDD_EXT	Y17	PA_13	AB19	PA_15
T14	GND	V16	VDD_EXT	Y18	PA_12	AB20	PA_11
T15	GND	V17	VDD_EXT	Y19	PA_10	AB21	PA_06
T16	GND	V18	VDD_EXT	Y20	PA_00	AB22	PA_04
T17	GND	V19	VDD_INT	Y21	DAI1_PIN14	AB23	PA_02
T18	VDD_EXT	V20	DAI1_PIN16	Y22	DAI1_PIN17	AC01	GND
T19	VDD_INT	V21	DAI1_PIN06	Y23	DAI1_PIN15	AC02	PCIE0_RXP
T20	DAI1_PIN03	V22	DAI1_PIN12	AA01	PB_08	AC03	PCIE0_RXM
T21	PG_03	V23	DAI1_PIN09	AA02	PB_07	AC04	PCIE0_CLKM
T22	PG_02	W01	PB_12	AA03	DAI0_PIN16	AC05	PCIE0_CLKP
T23	DAI1_PIN01	W02	PB_09	AA04	DAI0_PIN07	AC06	PCIE0_TXP
U01	SYS_XTAL0	W03	DAI0_PIN18	AA05	DAI0_PIN06	AC07	PCIE0_TXM
U02	$\overline{\text{SYS\_RESOUT}}$	W04	DAI0_PIN11	AA06	DAI0_PIN01	AC08	USB1_DM
U03	PC_00	W05	VDD_INT	AA07	PCIE0_REF	AC09	USB1_DP
U04	DAI0_PIN20	W06	VDD_INT	AA08	USB1_VBUS	AC10	USB0_DP
U05	VDD_INT	W07	VDD_PCIE	AA09	USB0_VBUS	AC11	USB0_DM
U06	VDD_EXT	W08	VDD_INT	AA10	TWI1_SCL	AC12	HADC0_VREFP
U07	GND	W09	VDD_INT	AA11	TWI1_SDA	AC13	VDD_HADC
U08	GND	W10	VDD_INT	AA12	HADC0_VIN1	AC14	GND
U09	GND	W11	VDD_INT	AA13	HADC0_VIN5	AC15	RTC0_CLKIN
U10	GND	W12	HADC0_VIN6	AA14	PB_06	AC16	MLB0_SIGP
U11	GND	W13	VDD_INT	AA15	PB_02	AC17	MLB0_DATP
U12	GND	W14	VDD_RTC	AA16	PB_04	AC18	MLB0_CLKP
U13	GND	W15	VDD_INT	AA17	PB_03	AC19	PB_01
U14	GND	W16	VDD_INT	AA18	PB_00	AC20	PA_07
U15	GND	W17	VDD_INT	AA19	PA_09	AC21	PA_08
U16	GND	W18	VDD_INT	AA20	PA_05	AC22	PA_03
U17	GND	W19	VDD_INT	AA21	PA_01	AC23	GND
U18	VDD_EXT	W20	DAI1_PIN20	AA22	DAI1_PIN19		
U19	DAI1_PIN08	W21	DAI1_PIN11	AA23	DAI1_PIN18		
U20	DAI1_PIN07	W22	DAI1_PIN10	AB01	DAI0_PIN15		
U21	DAI1_PIN04	W23	DAI1_PIN13	AB02	DAI0_PIN14		
U22	DAI1_PIN05	Y01	PB_11	AB03	DAI0_PIN09		
U23	DAI1_PIN02	Y02	PB_10	AB04	DAI0_PIN13		
V01	SYS_CLKIN0	Y03	DAI0_PIN17	AB05	DAI0_PIN04		
V02	PB_13	Y04	DAI0_PIN08	AB06	DAI0_PIN02		
V03	DAI0_PIN19	Y05	DAI0_PIN05	AB07	DAI0_PIN03		
V04	DAI0_PIN12	Y06	DAI0_PIN10	AB08	USB_XTAL		
V05	VDD_INT	Y07	USB0_ID	AB09	USB_CLKIN		
V06	VDD_EXT	Y08	VDD_USB	AB10	TWI2_SCL		
V07	VDD_PCIE_RX	Y09	USB0_VBC	AB11	TWI0_SDA		
V08	VDD_PCIE_TX	Y10	TWI0_SCL	AB12	HADC0_VREFN		
V09	VDD_EXT	Y11	TWI2_SDA	AB13	HADC0_VIN2		

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
GND	L16	GND	T08	PA_02	AB23	PC_11	K02
GND	L17	GND	T09	PA_03	AC22	PC_12	L02
GND	M07	GND	T10	PA_04	AB22	PC_13	C20
GND	M08	GND	T11	PA_05	AA20	PC_14	D21
GND	M09	GND	T12	PA_06	AB21	PC_15	E20
GND	M10	GND	T13	PA_07	AC20	PD_00	B22
GND	M11	GND	T14	PA_08	AC21	PD_01	C21
GND	M12	GND	T15	PA_09	AA19	PD_02	F21
GND	M13	GND	T16	PA_10	Y19	PD_03	J19
GND	M14	GND	T17	PA_11	AB20	PD_04	B23
GND	M15	GND	U07	PA_12	Y18	PD_05	C23
GND	M16	GND	U08	PA_13	Y17	PD_06	C22
GND	M17	GND	U09	PA_14	Y16	PD_07	J20
GND	N07	GND	U10	PA_15	AB19	PD_08	E21
GND	N08	GND	U11	PB_00	AA18	PD_09	D23
GND	N09	GND	U12	PB_01	AC19	PD_10	D22
GND	N10	GND	U13	PB_02	AA15	PD_11	E23
GND	N11	GND	U14	PB_03	AA17	PD_12	F23
GND	N12	GND	U15	PB_04	AA16	PD_13	F22
GND	N13	GND	U16	PB_05	Y15	PD_14	E22
GND	N14	GND	U17	PB_06	AA14	PD_15	K20
GND	N15	GND	Y14	PB_07	AA02	PE_00	G23
GND	N16	GND	AC01	PB_08	AA01	PE_01	G22
GND	N17	GND	AC14	PB_09	W02	PE_02	H23
GND	P07	GND	AC23	PB_10	Y02	PE_03	L20
GND	P08	HADC0_VIN0	Y12	PB_11	Y01	PE_04	G20
GND	P09	HADC0_VIN1	AA12	PB_12	W01	PE_05	H22
GND	P10	HADC0_VIN2	AB13	PB_13	V02	PE_06	F20
GND	P11	HADC0_VIN3	AB14	PB_14	T04	PE_07	J23
GND	P12	HADC0_VIN4	V12	PB_15	T02	PE_08	M19
GND	P13	HADC0_VIN5	AA13	PCIE0_CLKM	AC04	PE_09	L22
GND	P14	HADC0_VIN6	W12	PCIE0_CLKP	AC05	PE_10	K23
GND	P15	HADC0_VIN7	Y13	PCIE0_REF	AA07	PE_11	M20
GND	P16	HADC0_VREFN	AB12	PCIE0_RXM	AC03	PE_12	H21
GND	P17	HADC0_VREFP	AC12	PCIE0_RXP	AC02	PE_13	G21
GND	R07	JTG_TCK	P04	PCIE0_TXM	AC07	PE_14	L23
GND	R08	JTG_TDI	P02	PCIE0_TXP	AC06	PE_15	N20
GND	R09	JTG_TDO	P01	PC_00	U03	PF_00	M22
GND	R10	JTG_TMS	N01	PC_01	M01	PF_01	J22
GND	R11	$\overline{\text{JTG\_TRST}}$	N02	PC_02	M03	PF_02	M23
GND	R12	MLB0_CLKN	AB18	PC_03	N04	PF_03	M21
GND	R13	MLB0_CLKP	AC18	PC_04	L01	PF_04	N21
GND	R14	MLB0_DATN	AB17	PC_05	M02	PF_05	N22
GND	R15	MLB0_DATP	AC17	PC_06	K03	PF_06	K22
GND	R16	MLB0_SIGN	AB16	PC_07	L03	PF_07	N23
GND	R17	MLB0_SIGP	AC16	PC_08	J04	PF_08	P20
GND	T03	PA_00	Y20	PC_09	K04	PF_09	L21
GND	T07	PA_01	AA21	PC_10	L04	PF_10	P19