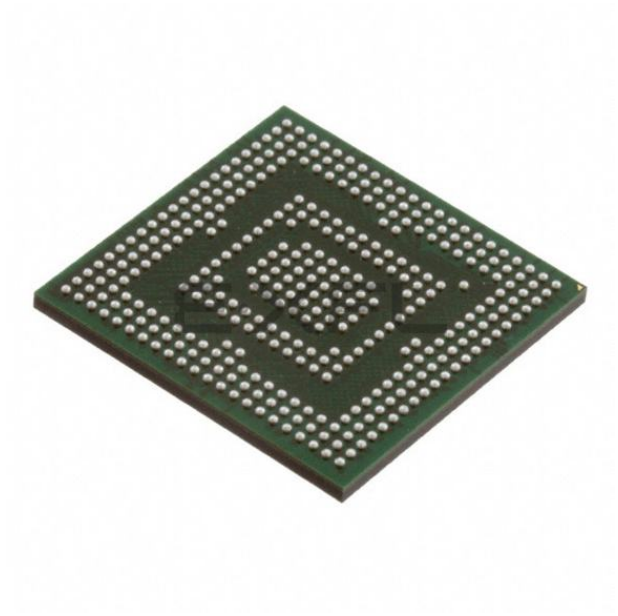


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc583bbcz-4a

Table 7. Memory Map of Mapped I/Os

	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	SHARC+ Core Instruction Fetch	
			VISA Space	ISA Space
SMC Bank 0 (64 MB)	0x40000000–0x43FFFFFF	0x01000000–0x01FFFFFF	0x00F00000–0x00F3FFFF	0x00700000–0x0073FFFF
SMC Bank 1 (64 MB)	0x44000000–0x47FFFFFF	Not applicable	Not applicable	Not applicable
SMC Bank 2 (64 MB)	0x48000000–0x4BFFFFFF	Not applicable	Not applicable	Not applicable
SMC Bank 3 (64 MB)	0x4C000000–0x4FFFFFFF	Not applicable	Not applicable	Not applicable
PCIe Data (256 MB)	0x50000000–0x5FFFFFFF	0x02000000–0x03FFFFFF	0x00F40000–0x00F7FFFF	0x00740000–0x0077FFFF
SPI2 Memory (512 MB)	0x60000000–0x7FFFFFFF	0x04000000–0x07FFFFFF	0x00F80000–0x00FFFFFF	0x00780000–0x007FFFFF

Table 8. DMC Memory Map

	Byte Address Space ARM Cortex-A5 – Data Access and Instruction Fetch SHARC+ – Data Access	Normal Word Address Space for Data Access SHARC+	SHARC+ Core Instruction Fetch	
			VISA Space	ISA Space
DMC0 (1 GB)	0x80000000–0xBFFFFFFF	0x10000000–0x17FFFFFF	0x00800000–0x00AFFFFF	0x00400000–0x004FFFFF
DMC1 (1 GB)	0xC0000000–0xFFFFFFFF	0x18000000–0x1FFFFFFF	0x00C00000–0x00EFFFFF	0x00600000–0x006FFFFF

System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch-fabric style for on-chip system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: one channel is the source channel and the second is the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based.

Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address
- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

CRC checksums can be calculated or compared automatically during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling or lack of toggling of system level signals.

System Event Controller (SEC)

Besides system events, the system event controller (SEC) further supports fault management including fault action configuration as timeout, internal indication by system interrupt, or external indication through the $\overline{\text{SYS\_FAULT}}$ pin and system reset.

PROCESSOR PERIPHERALS

The following sections describe the peripherals of the ADSP-SC58x/ADSP-2158x processors.

Dynamic Memory Controller (DMC)

The 16-bit dynamic memory controller (DMC) interfaces to:

- LPDDR1 (JESD209A) maximum frequency 200 MHz, DDRCLK (64 Mb to 2 Gb)
- DDR2 (JESD79-2E) maximum frequency 400 MHz, DDRCLK (256 Mb to 4 Gb)
- DDR3 (JESD79-3E) maximum frequency 450 MHz, DDRCLK (512 Mb to 8 Gb)
- DDR3L (1.5 V compatible only) maximum frequency 450 MHz, DDRCLK (512 Mb to 8 Gb)

See Table 8 for the DMC memory map.

Digital Audio Interface (DAI)

The processors support two mirrored digital audio interface (DAI) units. Each DAI can connect various peripherals to any of the DAI pins (DAI_PIN20–DAI_PIN01).

The application code makes these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to interconnect under software control. This functionality allows easy use of the DAI associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes the peripherals described in the following sections (SPORTs, ASRC, S/PDIF, and PCG). DAI pin buffers 20 and 19 can change the polarity of the input signals. Most signals of the peripherals belonging to different DAIs cannot be interconnected, with few exceptions.

The DAI_PINx pin buffers may also be used as GPIO pins. DAI input signals allow the triggering of interrupts on the rising edge, the falling edge, or both edges.

See the Digital Audio Interface (DAI) chapter of the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference for complete information on the use of the DAIs and SRUs.

Serial Ports (SPORTs)

The processors feature eight synchronous full serial ports. These ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. These devices include Analog Devices AD19xx/ADAU19xx family of audio codecs, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Two data lines, a clock, and frame sync make up the serial ports. The data lines can be programmed to either transmit or receive data and each data line has a dedicated DMA channel.

An individual full SPORT module consists of two independently configurable SPORT halves with identical functionality. Two bidirectional data lines—primary (0) and secondary (1)—are available per SPORT half and are configurable as either transmitters or receivers. Therefore, each SPORT half permits two unidirectional streams into or out of the same SPORT. This bidirectional functionality provides greater flexibility for serial communications. For full-duplex configuration, one half SPORT provides two transmit signals, while the other half SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in the following six modes:

- Standard DSP serial mode
- Multichannel time division multiplexing (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left justified mode
- Right justified mode

Asynchronous Sample Rate Converter (ASRC)

The asynchronous sample rate converter (ASRC) contains eight ASRC blocks. It is the same core in the AD1896 192 kHz stereo asynchronous sample rate converter. The ASRC provides up to 140 dB signal-to-noise ratio (SNR). The ASRC block performs synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The ASRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can clean up audio data from jittery clock sources such as the S/PDIF receiver.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The Sony/Philips Digital Interface Format (S/PDIF) is a standard audio data transfer format that allows the transfer of digital audio signals from one device to another without converting them to an analog signal. There are two S/PDIF transmit/receive

- DMC (VDD_DMC)
- PCIe (VDD_PCIE, VDD_PCIE_TX and VDD_PCIE_RX)

All power supplies must meet the specifications provided in the Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 27.)

Table 10. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR3/DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
PCIe_TX	$V_{DD\_PCIE\_TX}$
PCIe_RX	$V_{DD\_PCIE\_RX}$
PCIe	V_{DD_PCIE}
All other I/O (includes SYS, JTAG, and port pins)	V_{DD_EXT}

The power dissipated by the processors is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

Debug Access Port (DAP)

Debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment (CrossCore® Embedded Studio), evaluation products, emulators, and a variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore Embedded Studio integrated development environment (IDE).

CrossCore Embedded Studio is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Various EZ-Extenders® are also available, which are daughter cards that deliver additional specialized functionality, including audio and video processing. For more information visit www.analog.com.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit.

This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in circuit programming of the on-board Flash device to store user specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend the capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product.

Middleware Packages

Analog Devices offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos2
- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/ucusbh
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see "Analog Devices JTAG Emulation Technical Reference" (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-SC58x/ADSP-2158x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
HADC0_VIN5	HADC0 Analog Input at channel 5	Not Muxed	HADC0_VIN5
HADC0_VIN6	HADC0 Analog Input at channel 6	Not Muxed	HADC0_VIN6
HADC0_VIN7	HADC0 Analog Input at channel 7	Not Muxed	HADC0_VIN7
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_TCK	TAPC JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	TAPC JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC JTAG Serial Data Out	Not Muxed	JTG_TDO
JTG_TMS	TAPC JTAG Mode Select	Not Muxed	JTG_TMS
$\overline{\text{JTG\_TRST}}$	TAPC JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LP0_ACK	LP0 Acknowledge	D	PD_11
LP0_CLK	LP0 Clock	D	PD_10
LP0_D0	LP0 Data 0	D	PD_02
LP0_D1	LP0 Data 1	D	PD_03
LP0_D2	LP0 Data 2	D	PD_04
LP0_D3	LP0 Data 3	D	PD_05
LP0_D4	LP0 Data 4	D	PD_06
LP0_D5	LP0 Data 5	D	PD_07
LP0_D6	LP0 Data 6	D	PD_08
LP0_D7	LP0 Data 7	D	PD_09
LP1_ACK	LP1 Acknowledge	B	PB_15
LP1_CLK	LP1 Clock	C	PC_00
LP1_D0	LP1 Data 0	B	PB_07
LP1_D1	LP1 Data 1	B	PB_08
LP1_D2	LP1 Data 2	B	PB_09
LP1_D3	LP1 Data 3	B	PB_10
LP1_D4	LP1 Data 4	B	PB_11
LP1_D5	LP1 Data 5	B	PB_12
LP1_D6	LP1 Data 6	B	PB_13
LP1_D7	LP1 Data 7	B	PB_14
MLB0_CLKN	MLB0 Negative Differential Clock (–)	Not Muxed	MLB0_CLKN
MLB0_CLKP	MLB0 Positive Differential Clock (+)	Not Muxed	MLB0_CLKP
MLB0_DATN	MLB0 Negative Differential Data (–)	Not Muxed	MLB0_DATN
MLB0_DATP	MLB0 Positive Differential Data (+)	Not Muxed	MLB0_DATP
MLB0_SIGN	MLB0 Negative Differential Signal (–)	Not Muxed	MLB0_SIGN
MLB0_SIGP	MLB0 Positive Differential Signal (+)	Not Muxed	MLB0_SIGP
MLB0_CLK	MLB0 Single-Ended Clock	B	PB_04
MLB0_DAT	MLB0 Single-Ended Data	B	PB_06
MLB0_SIG	MLB0 Single-Ended Signal	B	PB_05
MLB0_CLKOUT	MLB0 Single-Ended Clock Out	D	PD_14
PA_00-15	PORTA Position 00 through Position 15	A	PA_00-15
PB_00-15	PORTB Position 00 through Position 15	B	PB_00-15
PC_00-15	PORTC Position 00 through Position 15	C	PC_00-15
PD_00-15	PORTD Position 00 through Position 15	D	PD_00-15
PE_00-15	PORTE Position 00 through Position 15	E	PE_00-15
PPI0_CLK	EPPI0 Clock	E	PE_03
PPI0_D00	EPPI0 Data 0	E	PE_12
PPI0_D01	EPPI0 Data 1	E	PE_11

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_BMODE0	Boot Mode Control n	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control n	Not Muxed	SYS_BMODE1
SYS_BMODE2	Boot Mode Control n	Not Muxed	SYS_BMODE2
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKIN1	Clock/Crystal Input	Not Muxed	SYS_CLKIN1
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_FAULT	Active High Fault Output	Not Muxed	SYS_FAULT
$\overline{\text{SYS\_FAULT}}$	Active Low Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
SYS_XTAL1	Crystal Output	Not Muxed	SYS_XTAL1
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_14
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_03
TM0_ACI2	TIMER0 Alternate Capture Input 2	D	PD_13
TM0_ACI3	TIMER0 Alternate Capture Input 3	C	PC_07
TM0_ACI4	TIMER0 Alternate Capture Input 4	B	PB_10
TM0_ACLK1	TIMER0 Alternate Clock 1	D	PD_08
TM0_ACLK2	TIMER0 Alternate Clock 2	D	PD_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_01
TM0_CLK	TIMER0 Clock	C	PC_11
TM0_TMR0	TIMER0 Timer 0	E	PE_09
TM0_TMR1	TIMER0 Timer 1	B	PB_15
TM0_TMR2	TIMER0 Timer 2	B	PB_10
TM0_TMR3	TIMER0 Timer 3	B	PB_07
TM0_TMR4	TIMER0 Timer 4	B	PB_08
TM0_TMR5	TIMER0 Timer 5	B	PB_14
TRACE0_CLK	TRACE0 Trace Clock	D	PD_10
TRACE0_D00	TRACE0 Trace Data 0	D	PD_02
TRACE0_D01	TRACE0 Trace Data 1	D	PD_03
TRACE0_D02	TRACE0 Trace Data 2	D	PD_04
TRACE0_D03	TRACE0 Trace Data 3	D	PD_05
TRACE0_D04	TRACE0 Trace Data 4	D	PD_06
TRACE0_D05	TRACE0 Trace Data 5	D	PD_07
TRACE0_D06	TRACE0 Trace Data 6	D	PD_08
TRACE0_D07	TRACE0 Trace Data 7	D	PD_09
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_00
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	C	PC_15
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_14
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_13
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	E	PE_01

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
VDD_PCIE	PCIE Supply Voltage	Not Muxed	VDD_PCIE
VDD_PCIE_RX	PCIE RX Supply Voltage	Not Muxed	VDD_PCIE_RX
VDD_PCIE_TX	PCIE TX Supply Voltage	Not Muxed	VDD_PCIE_TX
VDD_RTC	RTC VDD	Not Muxed	VDD_RTC
VDD_USB	USB VDD	Not Muxed	VDD_USB

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DAI0_PIN16	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 16 Notes: No notes
DAI0_PIN17	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 17 Notes: No notes
DAI0_PIN18	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 18 Notes: No notes
DAI0_PIN19	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 19 Notes: No notes
DAI0_PIN20	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 20 Notes: No notes
DAI1_PIN01	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 1 Notes: No notes
DAI1_PIN02	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 2 Notes: No notes
DAI1_PIN03	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 3 Notes: No notes
DAI1_PIN04	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 4 Notes: No notes
DAI1_PIN05	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 5 Notes: No notes
DAI1_PIN06	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 6 Notes: No notes
DAI1_PIN07	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 7 Notes: No notes
DAI1_PIN08	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 8 Notes: No notes
DAI1_PIN09	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 9 Notes: No notes
DAI1_PIN10	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 10 Notes: No notes
DAI1_PIN11	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 11 Notes: No notes
DAI1_PIN12	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 12 Notes: No notes
DAI1_PIN13	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 13 Notes: No notes
DAI1_PIN14	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 14 Notes: No notes
DAI1_PIN15	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 15 Notes: No notes
DAI1_PIN16	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 16 Notes: No notes
DAI1_PIN17	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 17 Notes: No notes
DAI1_PIN18	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 18 Notes: No notes
DAI1_PIN19	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 19 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 2 | EMAC0 Management Channel Clock | SMC0 Address 24 Notes: No notes
PA_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 3 | EMAC0 Management Channel Serial Data | SMC0 Address 23 Notes: No notes
PA_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 4 | EMAC0 Receive Data 0 | SMC0 Address 19 Notes: No notes
PA_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 5 | EMAC0 Receive Data 1 | SMC0 Address 18 Notes: No notes
PA_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 6 | EMAC0 RXCLK (GigE) or REFCLK (10/100) | SMC0 Address 17 Notes: No notes
PA_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 RXCTL (GigE) or CRS (10/100) | PORTA Position 7 | EMAC0 Carrier Sense/RMII Receive Data Valid | SMC0 Address 16 Notes: No notes
PA_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 8 | EMAC0 Receive Data 2 | SMC0 Address 12 Notes: No notes
PA_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 9 | EMAC0 Receive Data 3 | SMC0 Address 11 Notes: No notes
PA_10	InOut	A	PullDown	none	none	VDD_EXT	Desc: EMAC0 TXCTL (GigE) or TXEN (10/100) | PORTA Position 10 | EMAC0 Transmit Enable | SMC0 Address 22 Notes: No notes
PA_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 11 | EMAC0 Transmit Clock | SMC0 Address 15 Notes: No notes
PA_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 12 | EMAC0 Transmit Data 2 | SMC0 Address 14 Notes: No notes
PA_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 13 | EMAC0 Transmit Data 3 | SMC0 Address 13 Notes: No notes
PA_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 14 | EMAC0 PTP Pulse-Per-Second Output 3 | SINC0 Data 0 | SMC0 Address 10 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_00	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTC Position 0 | LP1 Clock | PWM0 Channel B Low Side | SMC0 Read Enable | SPI0 Slave Select Output 4 Notes: No notes
PC_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 1 | SPI2 Clock Notes: No notes
PC_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 2 | SPI2 Master In, Slave Out Notes: No notes
PC_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 3 | SPI2 Master Out, Slave In Notes: No notes
PC_04	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 4 | SPI2 Data 2 Notes: No notes
PC_05	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 5 | SPI2 Data 3 Notes: No notes
PC_06	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 6 | SPI2 Slave Select Output 1 | SPI2 Slave Select Input Notes: No notes
PC_07	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 7 | CAN0 Receive | SMC0 Memory Select 2 | SPI0 Slave Select Output 1 | TIMER0 Alternate Capture Input 3 Notes: No notes
PC_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 8 | CAN0 Transmit | SMC0 Memory Select 3 Notes: No notes
PC_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 9 | SPI0 Clock Notes: No notes
PC_10	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTC Position 10 | SPI0 Master In, Slave Out Notes: No notes
PC_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 11 | SPI0 Master Out, Slave In | TIMER0 Clock Notes: No notes
PC_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTC Position 12 | ACM0 External Trigger n | SMC0 Address 25 | SPI0 Ready | SPI0 Slave Select Output 3 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 12 | EPPI0 Data 0 | SMC0 Data 0 | SPI1 Slave Select Output 4 | SPI2 Ready Notes: No notes
PE_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 13 | EPPI0 Data 20 | SMC0 Memory Select 1 | SPI1 Clock Notes: No notes
PE_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 14 | EPPI0 Data 21 | SMC0 Byte Enable 0 | SPI1 Master In, Slave Out Notes: No notes
PE_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 15 | EPPI0 Data 22 | SMC0 Byte Enable 1 | SPI1 Master Out, Slave In Notes: No notes
PF_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 0 | SPI1 Slave Select Output 6 | TIMER0 Timer 6 Notes: No notes
PF_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 1 | SPI1 Slave Select Output 7 | TIMER0 Timer 7 Notes: No notes
PF_02	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 2 | HADC0 End of Conversion / Serial Data Out | MSI0 Data 0 Notes: No notes
PF_03	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 3 | HADC0 Controls to external multiplexer | MSI0 Data 1 Notes: No notes
PF_04	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 4 | HADC0 Controls to external multiplexer | MSI0 Data 2 Notes: No notes
PF_05	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 5 | HADC0 Controls to external multiplexer | MSI0 Data 3 Notes: No notes
PF_06	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 6 | MSI0 Data 4 | PWM2 Channel A Low Side Notes: No notes
PF_07	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 7 | MSI0 Data 5 | PWM2 Channel A High Side Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PF_08	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 8 | MSI0 Data 6 | PWM2 Channel B Low Side Notes: No notes
PF_09	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 9 | MSI0 Data 7 | PWM2 Channel B High Side Notes: No notes
PF_10	InOut	A	PullDown/ Programmable PullUp	none	none	VDD_EXT	Desc: PORTF Position 10 | MSI0 Command Notes: No notes
PF_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 11 | MSI0 Clock Notes: No notes
PF_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 12 | MSI0 Card Detect Notes: No notes
PF_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 13 | EMAC1 Carrier Sense/RMII Receive Data Valid | MSI0 eSDIO Interrupt Input | TRACE0 Trace Data | TRACE0 Trace Data 8 Notes: No notes
PF_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 14 | EMAC1 Management Channel Clock | TRACE0 Trace Data | TRACE0 Trace Data 9 Notes: No notes
PF_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTF Position 15 | EMAC1 Management Channel Serial Data | TRACE0 Trace Data | TRACE0 Trace Data 10 Notes: No notes
PG_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 0 | EMAC1 Reference Clock | TRACE0 Trace Clock Notes: No notes
PG_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 1 | EMAC1 Transmit Enable | TRACE0 Trace Data | TRACE0 Trace Data 11 Notes: No notes
PG_02	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 2 | EMAC1 Transmit Data 0 | TRACE0 Trace Data | TRACE0 Trace Data 12 Notes: No notes
PG_03	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTG Position 3 | EMAC1 Transmit Data 1 | TRACE0 Trace Data | TRACE0 Trace Data 13 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
TWI0_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
TWI1_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI1 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.
TWI1_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI1 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
TWI2_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI2 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.
TWI2_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI2 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
USB0_DM	InOut	F	none	none	none	VDD_USB	Desc: USB0 Data - Notes: Add external pull-down if not used[1]
USB0_DP	InOut	F	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Add external pull-down if not used[1]
USB0_ID	InOut		none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: Connect to GND when USB is not used[1]
USB0_VBC	InOut	E	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: Add external pull-down if not used[1]
USB0_VBUS	InOut	G	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: Connect to GND if not used[1]
USB1_DM	InOut	F	none	none	none	VDD_USB	Desc: USB1 Data - Notes: Add external pull-down if not used[1]
USB1_DP	InOut	F	none	none	none	VDD_USB	Desc: USB1 Data + Notes: Add external pull-down if not used[1]
USB1_VBUS	InOut	G	none	none	none	VDD_USB	Desc: USB1 Bus Voltage Notes: Connect to GND if not used[1]
USB_CLKIN	a		none	none	none		Desc: USB0/USB1 Clock/Crystal Input Notes: Services both USB0 and USB1. Connect to GND if not used.[1]

HADC

HADC Electrical Characteristics

Table 37. HADC Electrical Characteristics

Parameter	Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down.	10	µA

HADC DC Accuracy

Table 38. HADC DC Accuracy[1]

Parameter	Typ	Unit[2]
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±8	LSB
Offset Error Matching	±10	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 4096.

HADC Timing Specifications

Table 39. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

TMU

TMU Characteristics

Table 40. TMU Characteristics

Parameter	Typ	Unit
Resolution	1	°C
Accuracy	±6	°C

Asynchronous Flash Write

Table 49 and Figure 16 show asynchronous flash memory write timing, related to the SMC.

Table 49. Asynchronous Flash Write

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax/$\overline{\text{SMC0\_AMSx}}$ Assertion Before ADV Low[1]	PREST × t_{SCLK0} – 2		ns
$t_{DADVAWE}$	$\overline{\text{SMC0\_AWE}}$ Low Delay From ADV High[2]	PREAT × t_{SCLK0} – 2		ns
t_{WADV}	NR_ADV Active Low Width[3]	WST × t_{SCLK0} – 2		ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]	WHT × t_{SCLK0} – 3.5		ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[7]	WAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] PREAT value set using the SMC_BxETIM.PREAT bits.
[3] WST value set using the SMC_BxTIM.WST bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.
[7] WAT value set using the SMC_BxTIM.WAT bits.

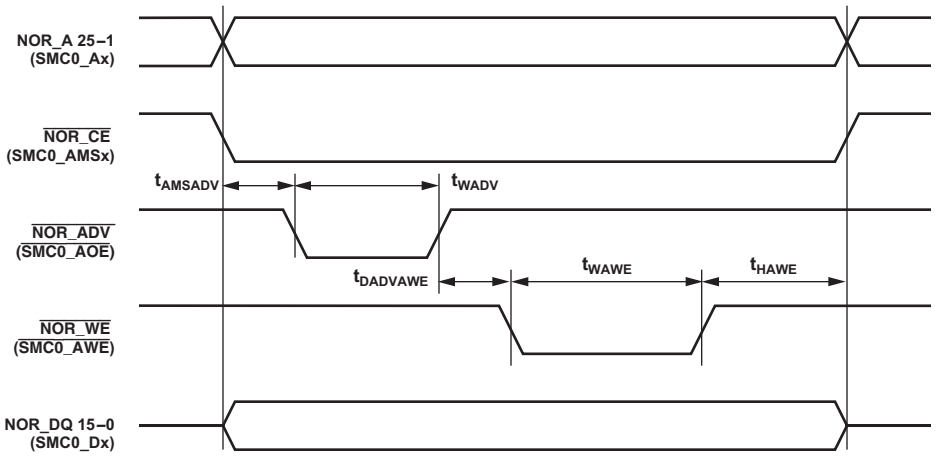


Figure 16. Asynchronous Flash Write

All Accesses

Table 50 describes timing that applies to all memory accesses, related to the SMC.

Table 50. All Accesses

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TURN}	$\overline{\text{SMC0\_AMSx}}$ Inactive Width	(IT + TT) × t_{SCLK0} – 2		ns

Mobile DDR SDRAM Read Cycle Timing

Table 55 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the DMC.

Table 55. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	Max	Unit
Timing Requirements				
t_{QH}	DMCx_DQ, DMCx_DQS Output Hold Time From DMCx_DQS	1.75		ns
t_{DQSQ}	DMCx_DQS to DMCx_DQ Skew for DMCx_DQS and Associated DMCx_DQ Signals		0.4	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

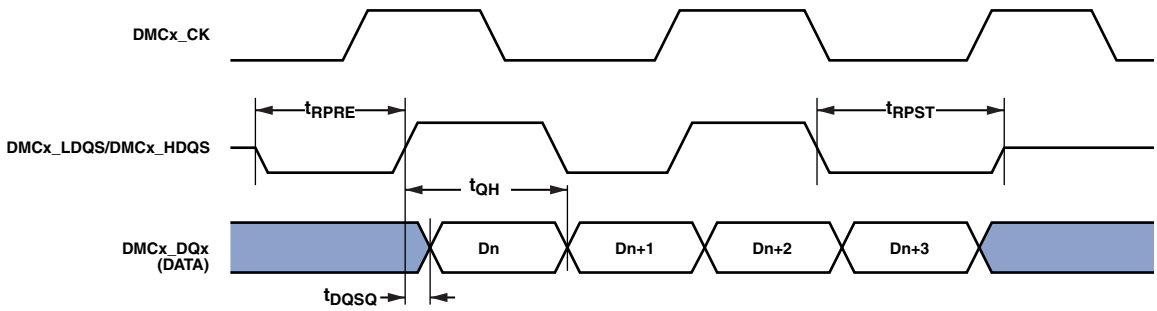


Figure 21. Mobile DDR SDRAM Controller Input AC Timing

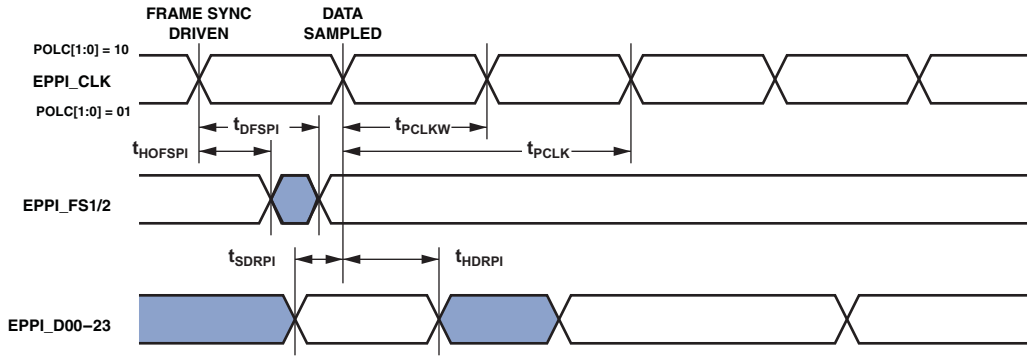


Figure 26. EPPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

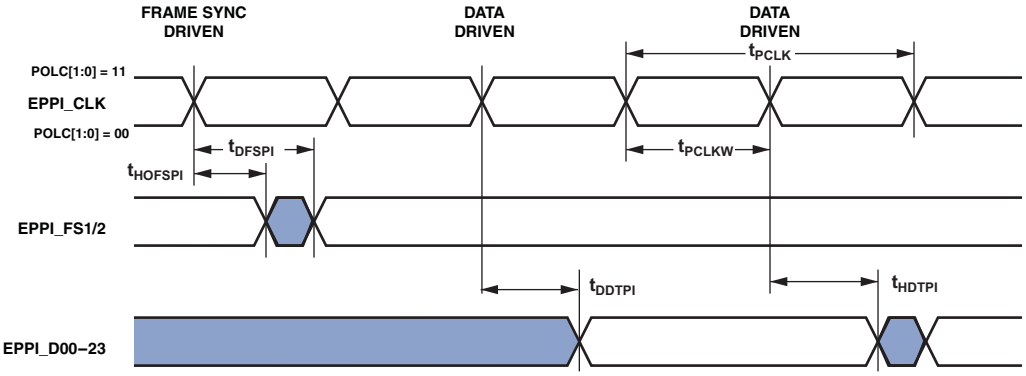


Figure 27. EPPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

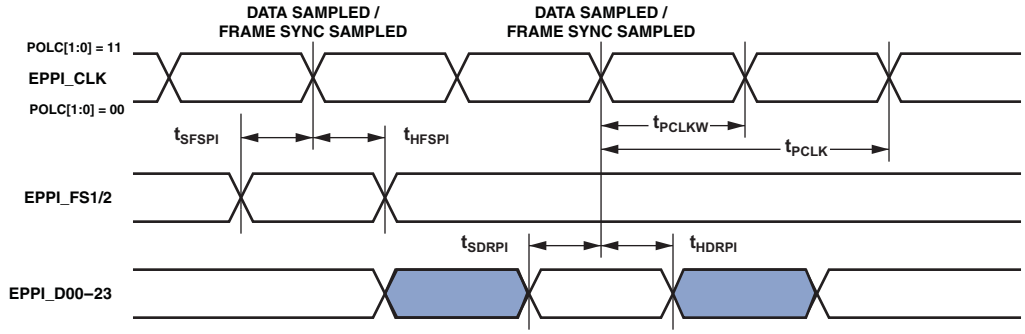


Figure 28. EPPI Internal Clock GP Receive Mode with External Frame Sync Timing

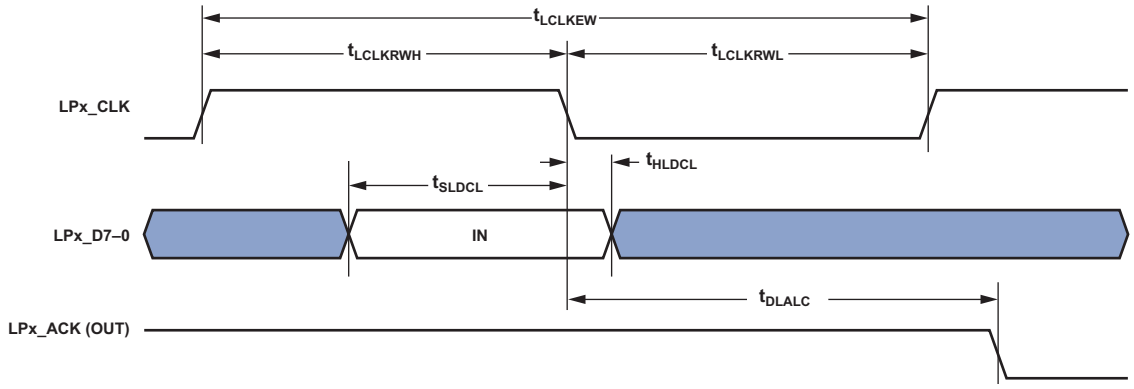


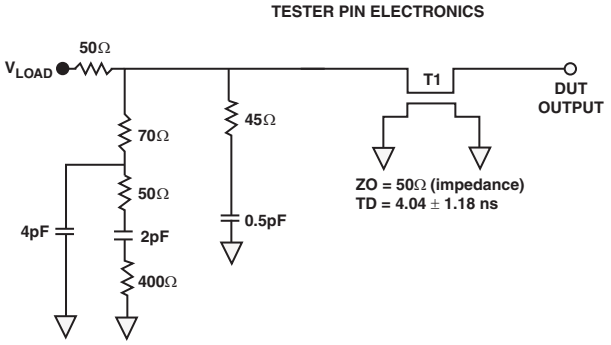
Figure 35. Link Ports—Receive

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the output voltage of the processor and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line) and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications section.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 92). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 93 through Figure 97 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 92. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

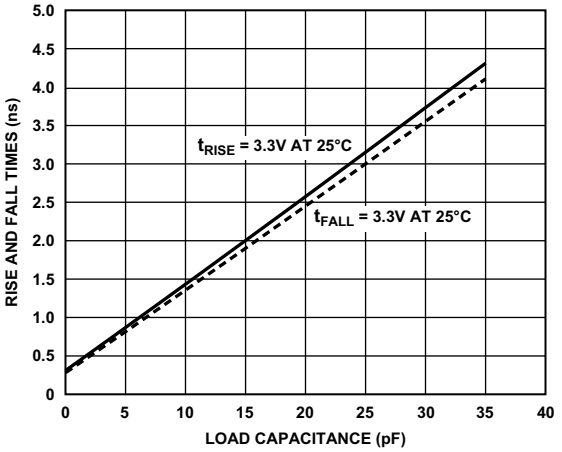


Figure 93. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

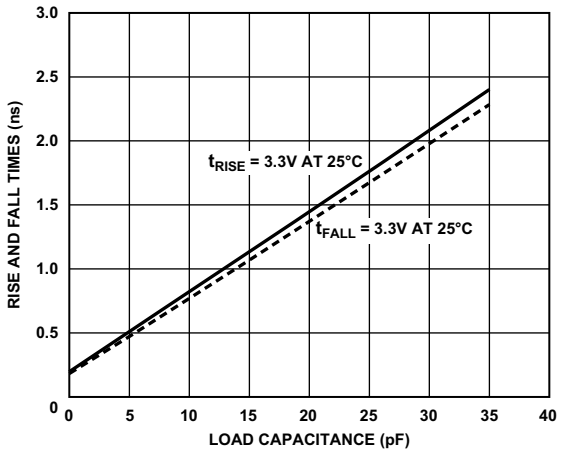


Figure 94. Driver Type H Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

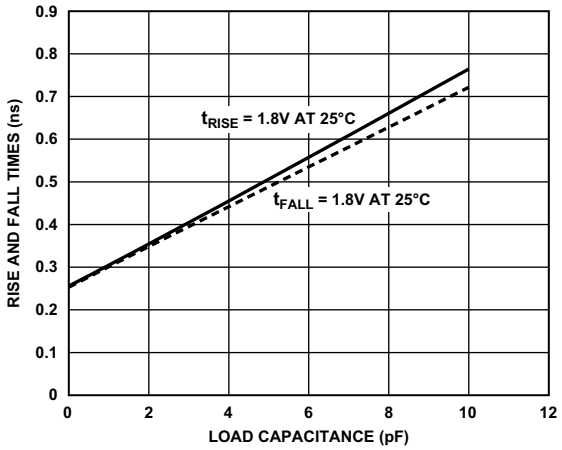


Figure 95. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for LPDDR

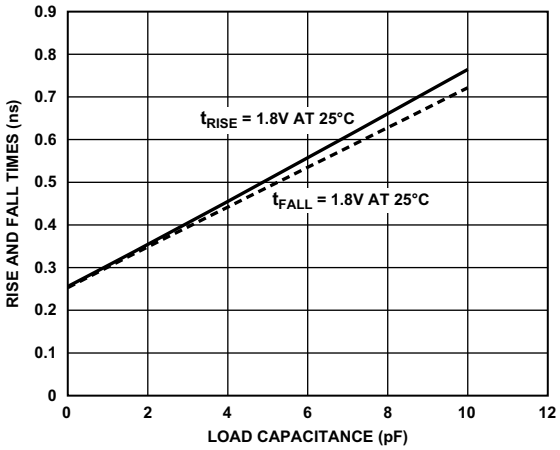


Figure 96. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for DDR2

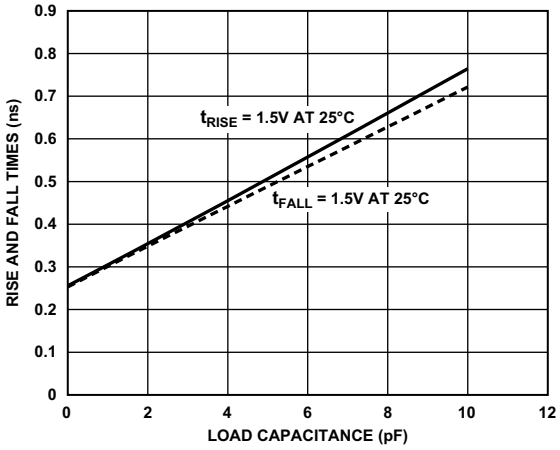


Figure 97. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.5 V) for DDR3

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured at top center of package.
Ψ_{JT} = from Table 104 and Table 105.
P_D = power dissipation (see the Total Internal Power Dissipation section for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 104 and Table 105, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 6-layer PCB with 101.6 mm × 152.4 mm dimensions.

Table 104. Thermal Characteristics for 349 CSP_BGA

Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.3	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.65	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.12	°C/W
Ψ_{JT}	2 linear m/s air flow	0.14	°C/W

Table 105. Thermal Characteristics for 529 CSP_BGA

Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.4	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.63	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.11	°C/W
Ψ_{JT}	2 linear m/s air flow	0.13	°C/W