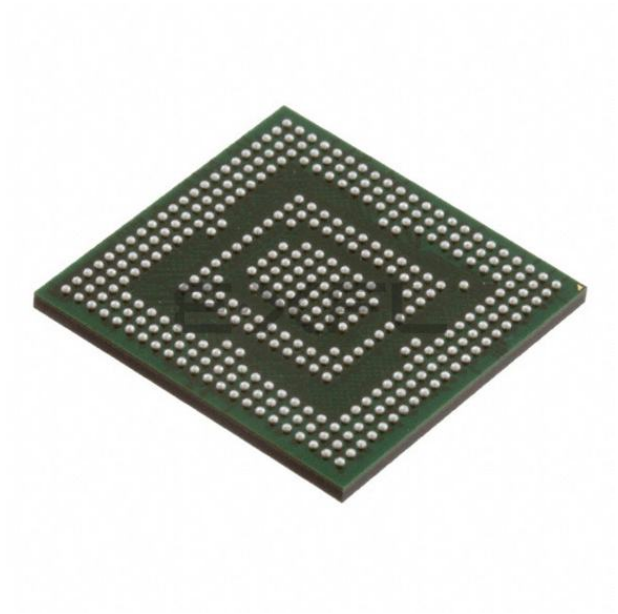

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc583kbcz-4a

ADC Control Module (ACM) Interface

The ADC control module (ACM) provides an interface that synchronizes the controls between the processors and an ADC. The analog-to-digital conversions are initiated by the processors, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process, generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by an internal DAI routing of the ACM with the SPORT0 block.

The processors interface directly to many ADCs without any glue logic required.

3-Phase Pulse Width Modulator (PWM) Units

The pulse width modulator (PWM) module is a flexible and programmable waveform generator. With minimal CPU intervention, the PWM generates complex waveforms for motor control, pulse coded modulation (PCM), DAC conversions, power switching, and power conversion. The PWM module has four PWM pairs capable of 3-phase PWM generation for source inverters for ac induction and dc brushless motors.

Each of the three 3-phase PWM generation units features the following:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single update mode with an option for asymmetric duty
- Programmable dead time and switching frequency
- Programmable dead time per channel
- Twos complement implementation which permits smooth transition to full on and full off states
- Dedicated asynchronous PWM shutdown signal

Ethernet Media Access Controller (EMAC)

The processor features two ethernet media access controllers (EMACs): 10/100 Ethernet and 10/100/1000/AVB Ethernet with precision time protocol IEEE 1588.

The processors can directly connect to a network through embedded fast EMAC that supports 10-BaseT (10 Mb/sec), 100-BaseT (100 Mb/sec) and 1000-BaseT (1 Gb/sec) operations. The 10/100 EMAC peripheral on the processors is fully compliant to the IEEE 802.3-2002 standard. The peripheral provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features of the EMAC are as follows:

- Support and RMII/RGMII protocols for external PHYs
- Full-duplex and half-duplex modes
- Media access management (in half-duplex operation)
- Flow control
- Station management, including the generation of MDC/MDIO frames for read/write access to PHY registers

Some advanced features of the EMAC are as follows:

- Automatic checksum computation of IP header and IP payload fields of receive frames
- Independent 32-bit descriptor driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Transmit DMA support for separate descriptors for MAC header and payload fields to eliminate buffer copy operations
- Convenient frame alignment modes
- 47 MAC management statistics counters with selectable clear on read behavior and programmable interrupts on half maximum value
- Advanced power management
- Magic packet detection and wakeup frame filtering
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression

Audio Video Bridging (AVB) Support (10/100/1000 EMAC Only)

The 10/100/1000 EMAC supports the following audio video (AVB) features:

- Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes
- IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Configuring up to two additional channels (Channel 1 and Channel 2) on the transmit and receive paths for AV traffic. Channel 0 is available by default and carries the legacy best effort Ethernet traffic on the transmit side.
- Separate DMA, transmit and receive FIFO for AVB latency class
- Programmable control to route received VLAN tagged non AV packets to channels or queues

Precision Time Protocol (PTP) IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC).

This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the engine are as follows:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment

Table 11. ADSP-SC58x/ADSP-2158x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
DMC_UDQS	InOut	**Data Strobe for Upper Byte (Complement).** Complement of UDQS. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Externally driven to VDD_DMC/2.
DMC_WE	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the WE input of dynamic memory.
ETH_CRS	Input	**Carrier Sense/RMII Receive Data Valid.** Multiplexed on alternate clock cycles. CRS— asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle. RXDV—asserted by the PHY when the data on RXDn is valid.
ETH_MDC	Output	**Management Channel Clock.** Clocks the MDC input of the PHY.
ETH_MDIO	InOut	**Management Channel Serial Data.** Bidirectional data bus for PHY control.
ETH_PTPAUXIN[n]	Input	**PTP Auxiliary Trigger Input.** Assert this signal to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO.
ETH_PTPCLKIN[n]	Input	**PTP Clock Input.** Optional external PTP clock input.
ETH_PTPPPS[n]	Output	**PTP Pulse Per Second Output.** When the advanced time stamp feature enables, this signal is asserted based on the PPS mode selected. Otherwise, PTPPPS is asserted every time the seconds counter is incremented.
ETH_REFCLK	Input	**Reference Clock.** Externally supplied Ethernet clock.
ETH_RXCLK_REFCLK	Input	**RXCLK (GigE) or REFCLK (10/100).**
ETH_RXCTL_CRS	Input	**RXCTL (GigE) or CRS (10/100).**
ETH_RXD[n]	Input	**Receive Data n.** Receive data bus.
ETH_TXCLK	Output	**Transmit Clock.**
ETH_TXCTL_TXEN	Output	**TXCTL (GigE) or TXEN (10/100).**
ETH_TXD[n]	Output	**Transmit Data n.** Transmits data bus.
ETH_TXEN	Output	**Transmit Enable.** When asserted, signal indicates the data on TXDn is valid.
HADC_EOC_DOUT	Output	**End of Conversion/Serial Data Out.** Transitions high for one cycle of the HADC internal clock at the end of every conversion. Alternatively, HADC serial data out can be seen by setting the appropriate bit in HADC_CTL.
HADC_MUX[n]	Input	**Controls to External Multiplexer.** Allows additional input channels when connected to an external multiplexer.
HADC_VIN[n]	Input	**Analog Input at Channel n.** Analog voltage inputs for digital conversion.
HADC_VREFN	Input	**Ground Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
HADC_VREFP	Input	**External Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
JTG_TRST	Input	**JTAG Reset.** JTAG test access port reset.
LP_ACK	InOut	**Acknowledge.** Provides handshaking. When the link port is configured as a receiver, ACK is an output. When the link port is configured as a transmitter, ACK is an input.
LP_CLK	InOut	**Clock.** When the link port is configured as a receiver, CLK is an input. When the link port is configured as a transmitter, CLK is an output.
LP_D[n]	InOut	**Data n.** Data bus. Input when receiving, output when transmitting.
MLB_CLKN	Input	**Differential Clock (–).**
MLB_CLKP	Input	**Differential Clock (+).**
MLB_DATN	InOut	**Differential Data (–).**
MLB_DATP	InOut	**Differential Data (+).**
MLB_SIGN	InOut	**Differential Signal (–).**

Table 11. ADSP-SC58x/ADSP-2158x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SMC_ABE[n]	Output	**Byte Enable n.** Indicates whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1 = 0 and SMC_ABE0 = 1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1 = 1 and SMC_ABE0 = 0.
SMC_AMS[n]	Output	**Memory Select n.** Typically connects to the chip select of a memory device.
SMC_AOE	Output	**Output Enable.** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready.** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable.** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable.** Asserts for the duration of a write access period.
SMC_A[nn]	Output	**Address n.** Address bus.
SMC_D[nn]	InOut	**Data n.** Bidirectional data bus.
SPI_CLK	InOut	**Clock.** Input in slave mode, output in master mode.
SPI_D2	InOut	**Data 2.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_D3	InOut	**Data 3.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	InOut	**Ready.** Optional flow signal. Output in slave mode, input in master mode.
SPI_SEL[n]	Output	**Slave Select Output n.** Used in master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input.** Slave mode—acts as the slave select input. Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	InOut	**Channel A Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	InOut	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AD1	InOut	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AFS	InOut	**Channel A Frame Sync.** The frame sync pulse initiates shifting of the serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SPT_BCLK	InOut	**Channel B Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	InOut	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BD1	InOut	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BFS	InOut	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SYS_BMODE[n]	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN0	Input	**Clock/Crystal Input.**
SYS_CLKIN1	Input	**Clock/Crystal Input.**
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference for more details.

349-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 12 for the 349-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference for complete information on the use of the DAI and SRUs.

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	C	PC_13
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	D	PD_00
ACM0_A4	ACM0 ADC Control Signals	D	PD_01
ACM0_T0	ACM0 External Trigger n	C	PC_12
C1_FLG0	SHARC Core 1 Flag Pin	E	PE_01
C1_FLG1	SHARC Core 1 Flag Pin	E	PE_03
C1_FLG2	SHARC Core 1 Flag Pin	E	PE_05
C1_FLG3	SHARC Core 1 Flag Pin	E	PE_07
C2_FLG0	SHARC Core 2 Flag Pin	E	PE_02
C2_FLG1	SHARC Core 2 Flag Pin	E	PE_04
C2_FLG2	SHARC Core 2 Flag Pin	E	PE_06
C2_FLG3	SHARC Core 2 Flag Pin	E	PE_08
CAN0_RX	CAN0 Receive	C	PC_07
CAN0_TX	CAN0 Transmit	C	PC_08
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_09
CNT0_DG	CNT0 Count Down and Gate	B	PB_14
CNT0_UD	CNT0 Count Up and Direction	B	PB_12
CNT0_ZM	CNT0 Count Zero Marker	B	PB_11
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN19	DAI0 Pin 19	Not Muxed	DAI0_PIN19
DAI0_PIN20	DAI0 Pin 20	Not Muxed	DAI0_PIN20

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D02	EPPI0 Data 2	E	PE_10
PPI0_D03	EPPI0 Data 3	E	PE_09
PPI0_D04	EPPI0 Data 4	E	PE_08
PPI0_D05	EPPI0 Data 5	E	PE_07
PPI0_D06	EPPI0 Data 6	E	PE_06
PPI0_D07	EPPI0 Data 7	E	PE_05
PPI0_D08	EPPI0 Data 8	E	PE_04
PPI0_D09	EPPI0 Data 9	E	PE_00
PPI0_D10	EPPI0 Data 10	D	PD_15
PPI0_D11	EPPI0 Data 11	D	PD_14
PPI0_D12	EPPI0 Data 12	B	PB_04
PPI0_D13	EPPI0 Data 13	B	PB_05
PPI0_D14	EPPI0 Data 14	B	PB_00
PPI0_D15	EPPI0 Data 15	B	PB_01
PPI0_D16	EPPI0 Data 16	B	PB_02
PPI0_D17	EPPI0 Data 17	B	PB_03
PPI0_D18	EPPI0 Data 18	D	PD_13
PPI0_D19	EPPI0 Data 19	D	PD_12
PPI0_D20	EPPI0 Data 20	E	PE_13
PPI0_D21	EPPI0 Data 21	E	PE_14
PPI0_D22	EPPI0 Data 22	E	PE_15
PPI0_D23	EPPI0 Data 23	D	PD_00
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_02
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_01
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_15
PWM0_AH	PWM0 Channel A High Side	B	PB_07
PWM0_AL	PWM0 Channel A Low Side	B	PB_08
PWM0_BH	PWM0 Channel B High Side	B	PB_06
PWM0_BL	PWM0 Channel B Low Side	C	PC_00
PWM0_CH	PWM0 Channel C High Side	B	PB_13
PWM0_CL	PWM0 Channel C Low Side	B	PB_14
PWM0_DH	PWM0 Channel D High Side	B	PB_11
PWM0_DL	PWM0 Channel D Low Side	B	PB_12
PWM0_SYNC	PWM0 PWMTMR Grouped	E	PE_09
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	B	PB_15
PWM1_AH	PWM1 Channel A High Side	D	PD_03
PWM1_AL	PWM1 Channel A Low Side	D	PD_04
PWM1_BH	PWM1 Channel B High Side	D	PD_05
PWM1_BL	PWM1 Channel B Low Side	D	PD_06
PWM1_CH	PWM1 Channel C High Side	D	PD_07
PWM1_CL	PWM1 Channel C Low Side	D	PD_08
PWM1_DH	PWM1 Channel D High Side	D	PD_09
PWM1_DL	PWM1 Channel D Low Side	D	PD_10
PWM1_SYNC	PWM1 PWMTMR Grouped	D	PD_11
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	D	PD_02
PWM2_CH	PWM2 Channel C High Side	D	PD_15
PWM2_CL	PWM2 Channel C Low Side	E	PE_00
PWM2_DH	PWM2 Channel D High Side	E	PE_04

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
LP0_D7	LP0 Data 7	D	PD_09
LP1_ACK	LP1 Acknowledge	B	PB_15
LP1_CLK	LP1 Clock	C	PC_00
LP1_D0	LP1 Data 0	B	PB_07
LP1_D1	LP1 Data 1	B	PB_08
LP1_D2	LP1 Data 2	B	PB_09
LP1_D3	LP1 Data 3	B	PB_10
LP1_D4	LP1 Data 4	B	PB_11
LP1_D5	LP1 Data 5	B	PB_12
LP1_D6	LP1 Data 6	B	PB_13
LP1_D7	LP1 Data 7	B	PB_14
MLB0_CLKN	MLB0 Differential Clock (–)	Not Muxed	MLB0_CLKN
MLB0_CLKP	MLB0 Differential Clock (+)	Not Muxed	MLB0_CLKP
MLB0_DATN	MLB0 Differential Data (–)	Not Muxed	MLB0_DATN
MLB0_DATP	MLB0 Differential Data (+)	Not Muxed	MLB0_DATP
MLB0_SIGN	MLB0 Differential Signal (–)	Not Muxed	MLB0_SIGN
MLB0_SIGP	MLB0 Differential Signal (+)	Not Muxed	MLB0_SIGP
MLB0_CLK	MLB0 Single-Ended Clock	B	PB_04
MLB0_DAT	MLB0 Single-Ended Data	B	PB_06
MLB0_SIG	MLB0 Single-Ended Signal	B	PB_05
MLB0_CLKOUT	MLB0 Single-Ended Clock Out	D	PD_14
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	F	PF_12
MSI0_CLK	MSI0 Clock	F	PF_11
MSI0_CMD	MSI0 Command	F	PF_10
MSI0_D0	MSI0 Data 0	F	PF_02
MSI0_D1	MSI0 Data 1	F	PF_03
MSI0_D2	MSI0 Data 2	F	PF_04
MSI0_D3	MSI0 Data 3	F	PF_05
MSI0_D4	MSI0 Data 4	F	PF_06
MSI0_D5	MSI0 Data 5	F	PF_07
MSI0_D6	MSI0 Data 6	F	PF_08
MSI0_D7	MSI0 Data 7	F	PF_09
$\overline{\text{MSI0\_INT}}$	MSI0 eSDIO Interrupt Input	F	PF_13
PA_00-15	PORTA Position 00 through Position 15	A	PA_00-15
PB_00-15	PORTB Position 00 through Position 15	B	PB_00-15
PCIE0_CLKM	PCIE0 CLK -	Not Muxed	PCIE0_CLKM
PCIE0_CLKP	PCIE0 CLK +	Not Muxed	PCIE0_CLKP
PCIE0_REF	PCIE0 Reference	Not Muxed	PCIE0_REF
PCIE0_RXM	PCIE0 RX -	Not Muxed	PCIE0_RXM
PCIE0_RXP	PCIE0 RX +	Not Muxed	PCIE0_RXP
PCIE0_TXM	PCIE0 TX -	Not Muxed	PCIE0_TXM
PCIE0_TXP	PCIE0 TX +	Not Muxed	PCIE0_TXP
PC_00-15	PORTC Position 00 through Position 15	C	PC_00-15
PD_00-15	PORTD Position 00 through Position 15	D	PD_00-15
PE_00-15	PORTE Position 00 through Position 15	E	PE_00-15
PF_00-15	PORTF Position 00 through Position 15	F	PF_00-15
PG_00-5	PORTG Position 00 through Position 5	G	PG_00-5
PPI0_CLK	EPPI0 Clock	E	PE_03

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DAI0_PIN16	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 16 Notes: No notes
DAI0_PIN17	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 17 Notes: No notes
DAI0_PIN18	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 18 Notes: No notes
DAI0_PIN19	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 19 Notes: No notes
DAI0_PIN20	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI0 Pin 20 Notes: No notes
DAI1_PIN01	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 1 Notes: No notes
DAI1_PIN02	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 2 Notes: No notes
DAI1_PIN03	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 3 Notes: No notes
DAI1_PIN04	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 4 Notes: No notes
DAI1_PIN05	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 5 Notes: No notes
DAI1_PIN06	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 6 Notes: No notes
DAI1_PIN07	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 7 Notes: No notes
DAI1_PIN08	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 8 Notes: No notes
DAI1_PIN09	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 9 Notes: No notes
DAI1_PIN10	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 10 Notes: No notes
DAI1_PIN11	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 11 Notes: No notes
DAI1_PIN12	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 12 Notes: No notes
DAI1_PIN13	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 13 Notes: No notes
DAI1_PIN14	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 14 Notes: No notes
DAI1_PIN15	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 15 Notes: No notes
DAI1_PIN16	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 16 Notes: No notes
DAI1_PIN17	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 17 Notes: No notes
DAI1_PIN18	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 18 Notes: No notes
DAI1_PIN19	InOut	A	PullDown	none	none	VDD_EXT	Desc: DAI1 Pin 19 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC0_DQ11	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes
DMC0_DQ12	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes
DMC0_DQ13	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes
DMC0_DQ14	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes
DMC0_DQ15	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes
DMC0_LDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes
$\overline{\text{DMC0\_LDQS}}$	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: No notes
DMC0_LDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: External weak pull-down required in LPDDR mode
DMC0_ODT	Output	B	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: No notes
$\overline{\text{DMC0\_RAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes
$\overline{\text{DMC0\_RESET}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Reset (DDR3 only) Notes: No notes
DMC0_RZQ	a	B	none	none	none	VDD_DMC	Desc: DMC0 External calibration resistor connection Notes: Applicable for DDR2 and DDR3 only. External pull-down of 34 ohms need to be added.
DMC0_UDM	Output	B	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes
DMC0_UDQS	InOut	C	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
HADC0_VREFN	s	NA	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: No notes
HADC0_VREFP	s	NA	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: No notes
JTG_TCK	Input		PullUp	none	none	VDD_EXT	Desc: JTAG Clock Notes: No notes
JTG_TDI	Input		PullUp	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes
JTG_TDO	Output	A	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out Notes: No notes
JTG_TMS	InOut	A	PullUp	none	none	VDD_EXT	Desc: JTAG Mode Select Notes: No notes
$\overline{\text{JTG\_TRST}}$	Input		PullDown	none	none	VDD_EXT	Desc: JTAG Reset Notes: No notes
MLB0_CLKN	Input	NA	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Clock (-) Notes: No notes
MLB0_CLKP	Input	NA	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Clock (+) Notes: No notes
MLB0_DATN	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Data (-) Notes: No notes
MLB0_DATP	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Data (+) Notes: No notes
MLB0_SIGN	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Signal (-) Notes: No notes
MLB0_SIGP	InOut	I	Internal logic ensures that input signal does not float	none	none	VDD_EXT	Desc: MLB0 Differential Signal (+) Notes: No notes
PA_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 0 | EMAC0 Transmit Data 0 | SMC0 Address 21 Notes: No notes
PA_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTA Position 1 | EMAC0 Transmit Data 1 | SMC0 Address 20 Notes: No notes

Table 30. Phase-Locked Loop (PLL) Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	250	900	MHz

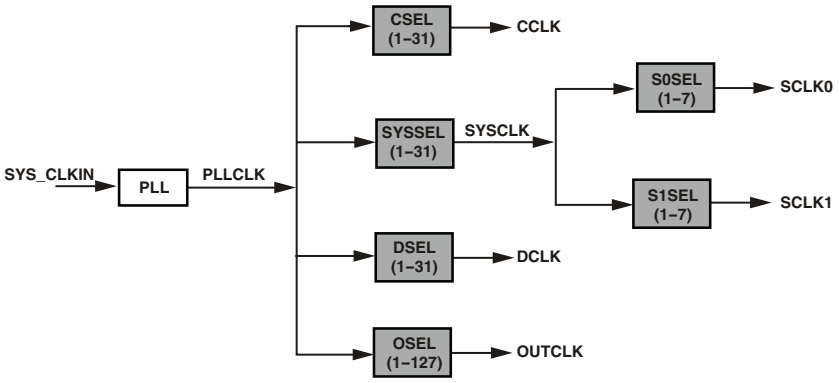


Figure 8. Clock Relationships and Divider Values

Table 34. Dynamic Current for Each SHARC+ Core (mA, with ASF = 1.00)

	Voltage (V_{DD_INT})		
f_{CCLK} (MHz)	1.05	1.10	1.15
450	321.3	336.6	351.9
400	285.6	299.2	312.8
350	249.9	261.8	273.7
300	214.2	224.4	234.6
250	178.5	187.0	195.5
200	142.8	149.6	156.4
150	107.1	112.2	117.3
100	71.4	74.8	78.2

Table 35. Dynamic Current for the ARM Cortex-A5 Core (mA, with ASF = 1.00)

	Voltage (V_{DD_INT})		
f_{CCLK} (MHz)	1.05	1.10	1.15
450	70.88	74.25	77.63
400	63.00	66.00	69.00
350	55.13	57.75	60.38
300	47.25	49.50	51.75
250	39.38	41.25	43.13
200	31.50	33.00	34.50
150	23.63	24.75	25.88
100	15.75	16.50	17.25

The following equation is used to compute the power dissipation when the FFT accelerator is used:

$I_{DD\_INT\_ACCL\_DYN}$ (mA) = $ASF_{ACCL} \times f_{SYSCLK}$ (MHz) × V_{DD_INT} (V)

Table 36. Activity Scaling Factors for the FFT Accelerator (ASF_{ACCL})

I_{DD_INT} Power Vector	ASF_{ACCL}
Unused	0.0
I_{DD-TYP}	0.32

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency, and a unique scaling factor.

$I_{DD\_INT\_SYSCLK\_DYN}$ (mA) = 0.78 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK0\_DYN}$ (mA) = 0.44 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK1\_DYN}$ (mA) = 0.06 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_DCLK\_DYN}$ (mA) = 0.14 × f_{DCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_OCLK\_DYN}$ (mA) = 0.02 × f_{OCLK} (MHz) × V_{DD_INT} (V)

Current from High-Speed Peripheral Operation

The following modules contribute significantly to power dissipation, and a single term is added when they are used.

$I_{DD\_INT\_USB\_DYN}$ = 20 mA (if both USBs are enabled in HS mode)

$I_{DD\_INT\_MLB\_DYN}$ = 10 mA (if MLB 6-pin interface is enabled)

$I_{DD\_INT\_GIGE\_DYN}$ = 10 mA (if gigabit EMAC is enabled)

$I_{DD\_INT\_PCIE\_DYN}$ = 240 mA (if PCIe is enabled in 5 Gbps mode)

Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via direct memory access (DMA). This current is proportional to the data rate. Refer to the power calculator available with "Estimating Power for ADSP-SC58x/2158x SHARC+ Processors" (EE-392) to estimate $I_{DD\_INT\_DMA\_DR\_DYN}$ based on the bandwidth of the data transfer.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

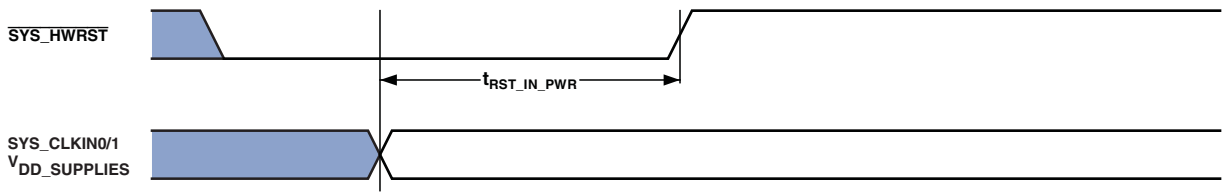
Power-Up Reset Timing

Table 43 and Figure 10 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU).

In Figure 10, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, and $V_{DD\_PCI\_CORE}$.

Table 43. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, $V_{DD\_PCI\_CORE}$) and SYS_CLKINx are Stable and Within Specification	$11 \times t_{CKIN}$		ns



NOTE: $V_{DD\_SUPPLIES}$ REFER TO V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}, V_{DD_RTC}, $V_{DD\_PCI\_TX}$, $V_{DD\_PCI\_RX}$, AND $V_{DD\_PCI\_CORE}$.

Figure 10. Power-Up Reset Timing

Clock and Reset Timing

Table 44 and Figure 11 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLK, DCLK, and OCLK timing specifications in Table 29, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 44. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKINx Frequency (Crystal)[1, 2, 3]	20	50	MHz
	SYS_CLKINx Frequency (External CLKIN)[1, 2, 3]	20	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 11) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 43 and Figure 10 for power-up reset timing.

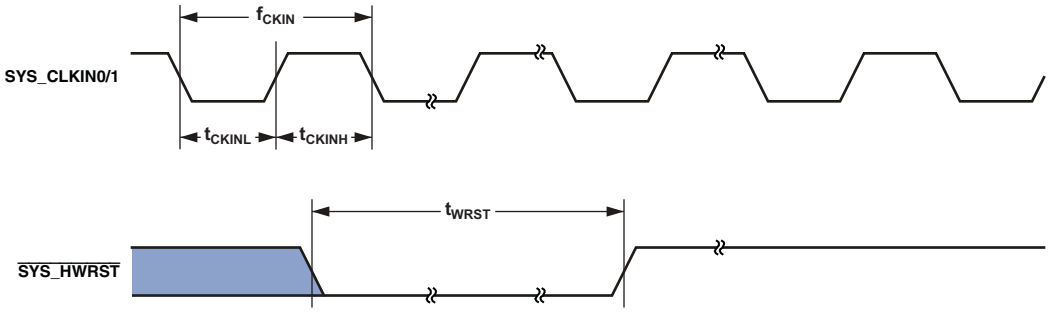


Figure 11. Clock and Reset Timing

Asynchronous Write

Table 48 and Figure 15 show asynchronous memory write timing, related to the SMC.

Table 48. Asynchronous Memory Write

Parameter		Min	Max	Unit
Timing Requirement				
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{\text{SMC0\_AWE}}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
t_{ENDAT}	DATA Enable After $\overline{\text{SMC0\_AMSx}}$ Assertion	–3.5		ns
t_{DDAT}	DATA Disable After $\overline{\text{SMC0\_AMSx}}$ Deassertion		2.5	ns
t_{AMSAWE}	ADDR/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AWE}}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]	WHT × t_{SCLK0} – 3.5		ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[2]	WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{\text{SMC0\_AWE}}$ High Delay After SMC0_ARDY Assertion	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

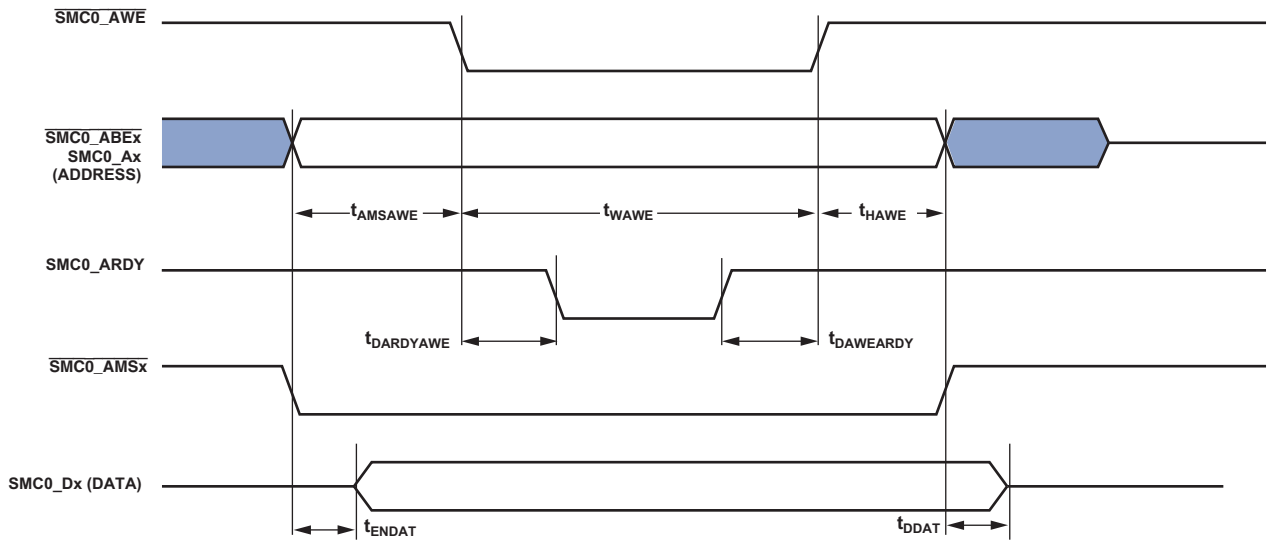


Figure 15. Asynchronous Write

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 96. Input signals are routed to the DAIx_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAIx_PINx pins.

Table 96. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

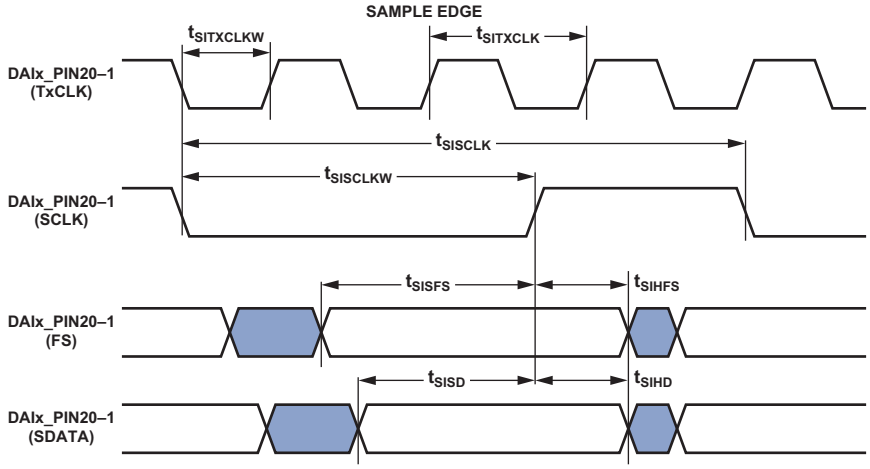


Figure 67. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 97. Oversampling Clock (TxCLK) Switching Characteristics

Parameter		Max	Unit
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital PLL mode, the internal digital PLL generates the 512 × FS clock.

Table 98. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns

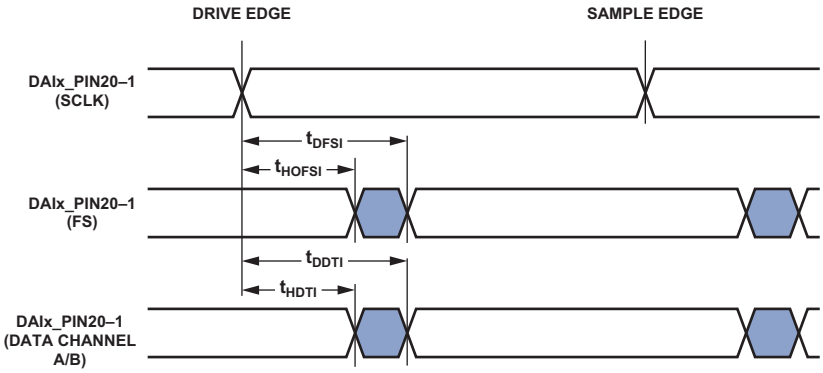


Figure 68. S/PDIF Receiver Internal Digital PLL Mode Timing

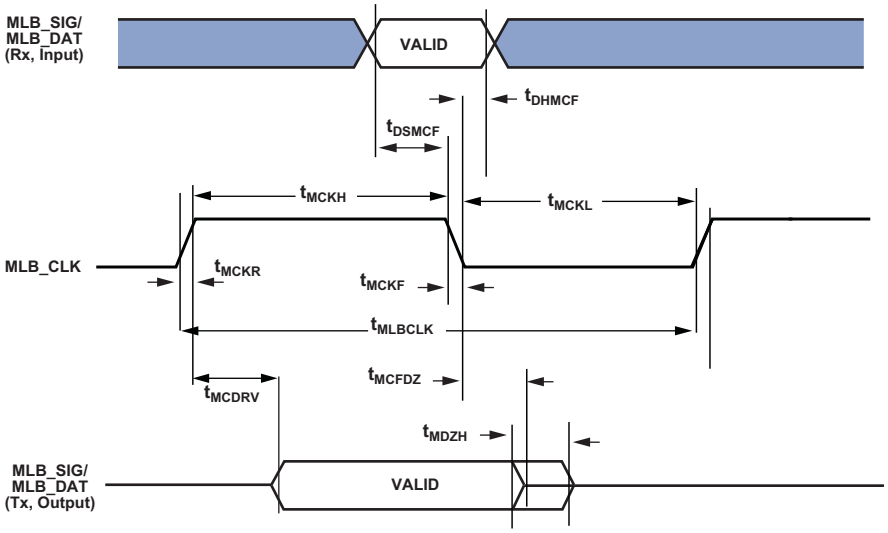


Figure 69. MLB Timing (3-Pin Interface)

The ac timing specifications of the 6-pin MLB interface is detailed in Table 100. Refer to the *Media Local Bus Specification version 4.2* for more details.

Table 100. 6-Pin MLB Interface Specifications

Parameter		Conditions	Min	Typ	Max	Unit
t_{MT}	Differential Transition Time at the Input Pin (See Figure 70)	20% to 80% $V_{IN}+/V_{IN}-$			1	ns
		80% to 20% $V_{IN}+/V_{IN}-$				
f_{MCKE}	MLBCP/N External Clock Operating Frequency (See Figure 71)[1]	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
f_{MCKR}	Recovered Clock Operating Frequency (Internal, not Observable at Pins, Only for Timing References) (See Figure 71)	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
t_{DELAY}	Transmitter MLBSP/N (MLBDP/N) Output Valid From Transition of MLBCP/N (Low to High) (See Figure 72)	f_{MCKR} = 2048 × FS	0.6		5	ns
t_{PHZ}	Disable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 73)	f_{MCKR} = 2048 × FS	0.6		7	ns
t_{PLZ}	Enable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 73)	f_{MCKR} = 2048 × FS	0.6		11.2	ns
t_{SU}	MLBSP/N (MLBDP/N) Valid to Transition of MLBCP/N (Low to High) (See Figure 72)	f_{MCKR} = 2048 × FS	1			ns
t_{HD}	MLBSP/N (MLBDP/N) Hold From Transition of MLBCP/N (Low to High) (See Figure 72)[2]		0.6			ns

[1] f_{MCKE} (maximum) and f_{MCKR} (maximum) include maximum cycle to cycle system jitter (t_{JITTER}) of 600 ps for a bit error rate of 10E-9.
[2] Receivers must latch MLBSP/N (MLBDP/N) data within t_{HD} (min) of the rising edge of MLBCP/N.

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
PA_14	AA17	PD_14	E22	VDD_DMC	G09	VDD_INT	J20
PA_15	Y19	PD_15	F21	VDD_DMC	G10	VDD_INT	K06
PB_00	Y15	PE_00	F22	VDD_DMC	G11	VDD_INT	K20
PB_01	Y17	PE_01	G21	VDD_DMC	G12	VDD_INT	L04
PB_02	AA16	PE_02	G22	VDD_DMC	G13	VDD_INT	L06
PB_03	AA18	PE_03	H21	VDD_DMC	G14	VDD_INT	L19
PB_04	Y16	PE_04	H22	VDD_DMC	G15	VDD_INT	M04
PB_05	AA15	PE_05	J21	VDD_DMC	G16	VDD_INT	M06
PB_06	Y14	PE_06	J22	VDD_DMC	G17	VDD_INT	M19
PB_07	U03	PE_07	K22	VDD_DMC	H06	VDD_INT	U09
PB_08	Y02	PE_08	K21	VDD_DMC	H07	VDD_INT	U10
PB_09	Y01	PE_09	L22	VDD_DMC	H17	VDD_INT	U11
PB_10	W01	PE_10	L21	VDD_DMC	J06	VDD_INT	U12
PB_11	W02	PE_11	L20	VDD_EXT	J17	VDD_INT	U13
PB_12	V02	PE_12	M22	VDD_EXT	K17	VDD_INT	W11
PB_13	V01	PE_13	M20	VDD_EXT	L17	VDD_INT	W12
PB_14	R03	PE_14	N22	VDD_EXT	M17	VDD_USB	U08
PB_15	R02	PE_15	M21	VDD_EXT	N06		
PC_00	N03	SYS_BMODE0	N02	VDD_EXT	N17		
PC_01	L01	SYS_BMODE1	P02	VDD_EXT	P06		
PC_02	K02	SYS_BMODE2	T02	VDD_EXT	P17		
PC_03	K01	SYS_CLKIN0	U01	VDD_EXT	R06		
PC_04	G03	SYS_CLKIN1	P01	VDD_EXT	R17		
PC_05	J01	SYS_CLKOUT	C17	VDD_EXT	T06		
PC_06	J02	SYS_FAULT	H03	VDD_EXT	T17		
PC_07	H02	$\overline{\text{SYS\_FAULT}}$	K03	VDD_EXT	U06		
PC_08	H01	$\overline{\text{SYS\_HWRST}}$	L02	VDD_EXT	U07		
PC_09	L03	$\overline{\text{SYS\_RESOUT}}$	U02	VDD_EXT	U14		
PC_10	G02	SYS_XTAL0	T01	VDD_EXT	U15		
PC_11	F02	SYS_XTAL1	N01	VDD_EXT	U16		
PC_12	G01	TWI0_SCL	Y09	VDD_EXT	U17		
PC_13	B18	TWI0_SDA	AA10	VDD_HADC	Y11		
PC_14	C16	TWI1_SCL	AB08	VDD_INT	D11		
PC_15	C18	TWI1_SDA	Y10	VDD_INT	D12		
PD_00	A19	TWI2_SCL	AA08	VDD_INT	E20		
PD_01	C15	TWI2_SDA	AA09	VDD_INT	F07		
PD_02	B19	USB0_DM	AB07	VDD_INT	F08		
PD_03	A20	USB0_DP	AB06	VDD_INT	F09		
PD_04	C19	USB0_ID	AA06	VDD_INT	F10		
PD_05	B20	USB0_VBC	Y08	VDD_INT	F12		
PD_06	A21	USB0_VBUS	AA07	VDD_INT	F13		
PD_07	C21	USB_CLKIN	AB04	VDD_INT	F14		
PD_08	B22	USB_XTAL	AB05	VDD_INT	F15		
PD_09	D21	VDD_DMC	F06	VDD_INT	F16		
PD_10	D20	VDD_DMC	F11	VDD_INT	F17		
PD_11	C22	VDD_DMC	G06	VDD_INT	F20		
PD_12	D22	VDD_DMC	G07	VDD_INT	G20		
PD_13	E21	VDD_DMC	G08	VDD_INT	H20		

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
T08	GND	V10	VDD_EXT	Y12	HADC0_VIN0	AB14	HADC0_VIN3
T09	GND	V11	VDD_EXT	Y13	HADC0_VIN7	AB15	RTC0_XTAL
T10	GND	V12	HADC0_VIN4	Y14	GND	AB16	MLB0_SIGN
T11	GND	V13	VDD_EXT	Y15	PB_05	AB17	MLB0_DATN
T12	GND	V14	VDD_EXT	Y16	PA_14	AB18	MLB0_CLKN
T13	GND	V15	VDD_EXT	Y17	PA_13	AB19	PA_15
T14	GND	V16	VDD_EXT	Y18	PA_12	AB20	PA_11
T15	GND	V17	VDD_EXT	Y19	PA_10	AB21	PA_06
T16	GND	V18	VDD_EXT	Y20	PA_00	AB22	PA_04
T17	GND	V19	VDD_INT	Y21	DAI1_PIN14	AB23	PA_02
T18	VDD_EXT	V20	DAI1_PIN16	Y22	DAI1_PIN17	AC01	GND
T19	VDD_INT	V21	DAI1_PIN06	Y23	DAI1_PIN15	AC02	PCIE0_RXP
T20	DAI1_PIN03	V22	DAI1_PIN12	AA01	PB_08	AC03	PCIE0_RXM
T21	PG_03	V23	DAI1_PIN09	AA02	PB_07	AC04	PCIE0_CLKM
T22	PG_02	W01	PB_12	AA03	DAI0_PIN16	AC05	PCIE0_CLKP
T23	DAI1_PIN01	W02	PB_09	AA04	DAI0_PIN07	AC06	PCIE0_TXP
U01	SYS_XTAL0	W03	DAI0_PIN18	AA05	DAI0_PIN06	AC07	PCIE0_TXM
U02	$\overline{\text{SYS\_RESOUT}}$	W04	DAI0_PIN11	AA06	DAI0_PIN01	AC08	USB1_DM
U03	PC_00	W05	VDD_INT	AA07	PCIE0_REF	AC09	USB1_DP
U04	DAI0_PIN20	W06	VDD_INT	AA08	USB1_VBUS	AC10	USB0_DP
U05	VDD_INT	W07	VDD_PCIE	AA09	USB0_VBUS	AC11	USB0_DM
U06	VDD_EXT	W08	VDD_INT	AA10	TWI1_SCL	AC12	HADC0_VREFP
U07	GND	W09	VDD_INT	AA11	TWI1_SDA	AC13	VDD_HADC
U08	GND	W10	VDD_INT	AA12	HADC0_VIN1	AC14	GND
U09	GND	W11	VDD_INT	AA13	HADC0_VIN5	AC15	RTC0_CLKIN
U10	GND	W12	HADC0_VIN6	AA14	PB_06	AC16	MLB0_SIGP
U11	GND	W13	VDD_INT	AA15	PB_02	AC17	MLB0_DATP
U12	GND	W14	VDD_RTC	AA16	PB_04	AC18	MLB0_CLKP
U13	GND	W15	VDD_INT	AA17	PB_03	AC19	PB_01
U14	GND	W16	VDD_INT	AA18	PB_00	AC20	PA_07
U15	GND	W17	VDD_INT	AA19	PA_09	AC21	PA_08
U16	GND	W18	VDD_INT	AA20	PA_05	AC22	PA_03
U17	GND	W19	VDD_INT	AA21	PA_01	AC23	GND
U18	VDD_EXT	W20	DAI1_PIN20	AA22	DAI1_PIN19		
U19	DAI1_PIN08	W21	DAI1_PIN11	AA23	DAI1_PIN18		
U20	DAI1_PIN07	W22	DAI1_PIN10	AB01	DAI0_PIN15		
U21	DAI1_PIN04	W23	DAI1_PIN13	AB02	DAI0_PIN14		
U22	DAI1_PIN05	Y01	PB_11	AB03	DAI0_PIN09		
U23	DAI1_PIN02	Y02	PB_10	AB04	DAI0_PIN13		
V01	SYS_CLKIN0	Y03	DAI0_PIN17	AB05	DAI0_PIN04		
V02	PB_13	Y04	DAI0_PIN08	AB06	DAI0_PIN02		
V03	DAI0_PIN19	Y05	DAI0_PIN05	AB07	DAI0_PIN03		
V04	DAI0_PIN12	Y06	DAI0_PIN10	AB08	USB_XTAL		
V05	VDD_INT	Y07	USB0_ID	AB09	USB_CLKIN		
V06	VDD_EXT	Y08	VDD_USB	AB10	TWI2_SCL		
V07	VDD_PCIE_RX	Y09	USB0_VBC	AB11	TWI0_SDA		
V08	VDD_PCIE_TX	Y10	TWI0_SCL	AB12	HADC0_VREFN		
V09	VDD_EXT	Y11	TWI2_SDA	AB13	HADC0_VIN2		

Dimensions for the 19 mm × 19 mm 529-ball CSP_BGA package in Figure 101 are shown in millimeters.

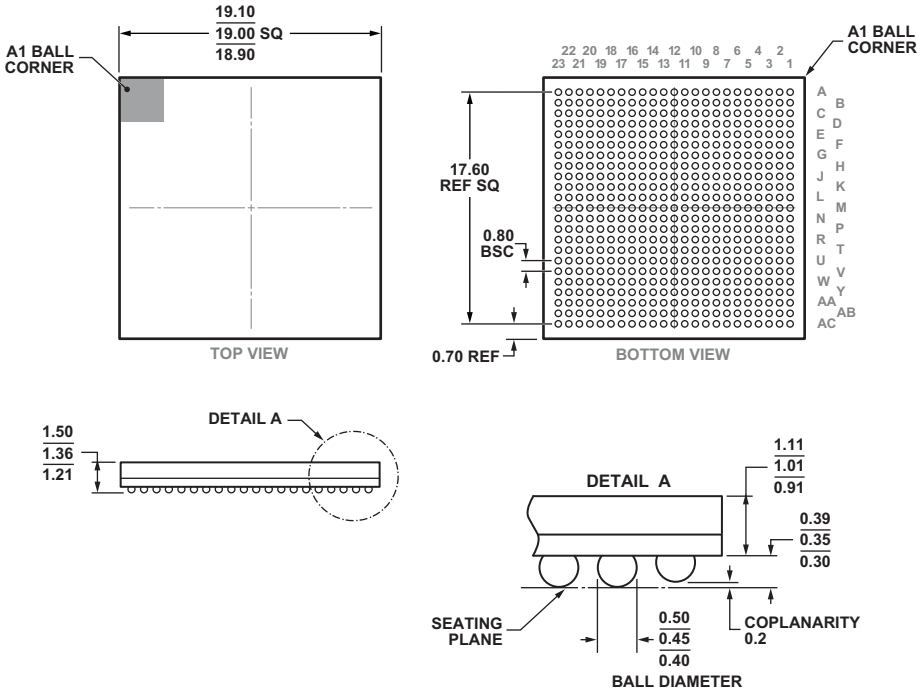


Figure 101. 529-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-529-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 106 is an aid for PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 106. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-349-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter
BC-529-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter