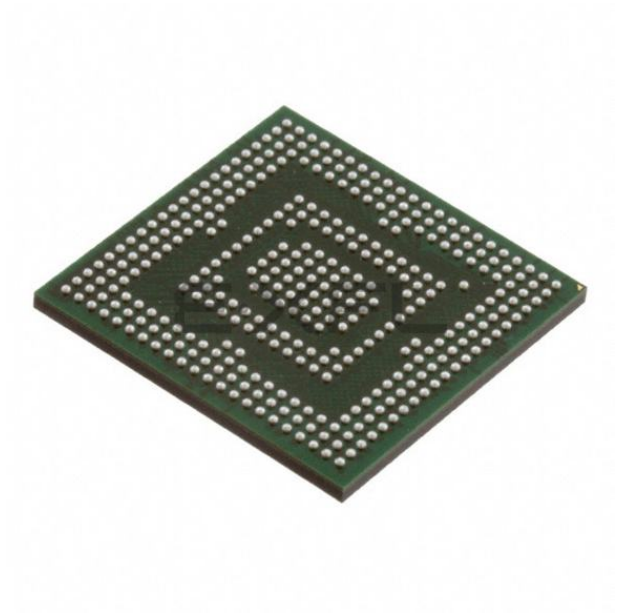

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc584bbcz-3a

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REVISION HISTORY

10/2016—Revision 0: Initial Version

Memory Direct Memory Access (MDMA)

The processor supports various MDMA operations, including,

- Standard bandwidth MDMA channels with CRC protection (32-bit bus width, runs on SCLK0)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channels (64-bit bus width, run on SYCLK, one channel can be assigned to the FFT accelerator)

Extended Memory DMA

Extended memory DMA supports various operating modes such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory) with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

Cyclic Redundant C ode (CRC) Protection

The cyclic redundant codes (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, every 100 ms the system software initiates the signature calculation of the entire memory contents and compares these contents with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit/byte mirroring option (endianness)
- Fault/error interrupt mechanisms
- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of a memory or an MMR block

Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for five different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exceptions event occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered on the one side by the SHARC+ core, such as data alignment (SIMD/long word) or compute violations (fixed or floating point), and illegal instructions cause core exceptions. Conditions triggered on the other side by the SEC, such as error correcting codes (ECC)/parity/watchdog/system clock, cause system exceptions.
- An interrupts event occurs asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

Both SHARC+ cores feature a system event controller. The SEC features include the following:

- Comprehensive system event source management including interrupt enable, fault enable, priority, core mapping, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A slave control port that provides access to all SEC registers for configuration, status, and interrupt/fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-SC58x/ADSP-2158x processors.

FFT/IFFT Accelerator

A high performance FFT/IFFT accelerator is available to improve the overall floating-point computation power of the ADSP-SC58x/ADSP-2158x processors.

The following features are available to improve the overall performance of the FFT/IFFT accelerator:

- Support for the IEEE-754/854 single-precision floating-point data format.
- Automatic twiddle factor generation to reduce system bandwidth.
- Support for a vector complex multiply for windowing and frequency domain filtering.
- Ability to pipeline the data flow. This allows the accelerator to bring in a new data set while the current data set is processed and the previous data set is sent out to memory. This can provide a significant system level performance improvement.
- Ability to output the result as the magnitude squared of the complex samples.
- Dedicated, high speed DMA controller with 64-bit buses that can read and write data from any memory space.

The FFT/IFFT accelerator can run concurrently with the other accelerators on the processor.

Finite Impulse Response (FIR) Accelerator

The finite impulse response (FIR) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency. The FIR accelerator can access all memory spaces and can run concurrently with the other accelerators on the processor.

Infinite Impulse Response (IIR) Accelerator

The infinite impulse response (IIR) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency. The IIR accelerator can access all memory spaces and run concurrently with the other accelerators on the processor.

Harmonic Analysis Engine (HAE)

The harmonic analysis engine (HAE) block receives 8 kHz input samples from two source signals whose frequencies are between 45 Hz and 65 Hz. The HAE processes the input samples and produces output results. The output results consist of power quality measurements of the fundamental and up to 12 additional harmonics.

Sinus Cardinalis (SINC) Filter

The sinus cardinalis (SINC) filter module processes four bit streams using a pair of configurable SINC filters for each bit stream. The purpose of the primary SINC filter of each pair is to produce the filtered and decimated output for the pair. The output can decimate any integer rate between 8 and 256 times lower than the input rate. Greater decimation allows greater removal of noise, and, therefore, greater effective number of bits (ENOB).

Optional additional filtering outside the SINC module can further increase ENOB. The primary SINC filter output is accessible through transfer to processor memory, or to another peripheral, via DMA.

Each of the four channels is also provided with a low latency secondary filter with programmable positive and negative overrange detection comparators. These limit detection events can interrupt the core, generate a trigger, or signal a system fault.

Digital Transmission Content Protection (DTCP)

Contact Analog Devices for more information on DTCP.

SYSTEM DESIGN

The following sections provide an introduction to system design features and power supply issues.

Clock Management

The processors provide three operating modes, each with a different performance and power profile. Control of clocking to each of the processor peripherals reduces power consumption. The processors do not support any low power operation modes. Control of clocking to each of the processor peripherals can reduce the power consumption.

Reset Control Unit (RCU)

Reset is the initial state of the whole processor, or the core, and is the result of a hardware or software triggered event. In this state, all control registers are set to default values and functional units are idle. Exiting a full system reset starts with the core ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions put the system into an undefined state or causes resources to stall. This is particularly important when the core resets (programs must ensure that there is no pending system activity involving the core when it is reset).

From a system perspective, reset is defined by both the reset target and the reset source.

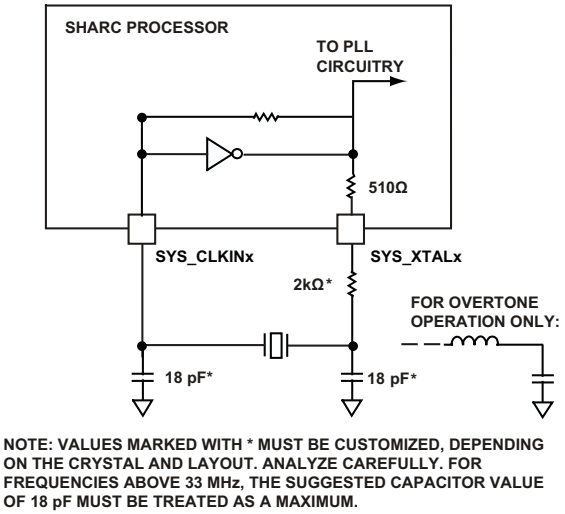

Figure 7. External Crystal Connection

A third overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit, shown in Figure 7. A design procedure for the third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168). The same recommendations can be used for the USB crystal oscillator.

Clock Distribution Unit (CDU)

The two CGUs each provide outputs which feed a clock distribution unit (CDU). The clock outputs CLKO0–CLKO9 are connected to various targets. For more information, refer to the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.

Power-Up

SYS_XTALx oscillations (SYS_CLKINx) start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ starts on-chip PLL locking (PLL lock counter). The deassertion must apply only if all voltage supplies and SYS_CLKINx oscillations are valid (refer to the Power-Up Reset Timing section).

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In master boot mode, the processors actively load data from serial memories. In slave boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 9. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

In the ADSP-SC58x processors, the ARM Cortex-A5 (Core 0) controls the boot process, including loading all internal and external memory. Likewise, in the ADSP-2158x processors, the SHARC+ (Core 1) controls the boot function. The option for secure boot is available on all models.

Table 9. Boot Modes

SYS_BMODE[n] Setting	Boot Mode
000	No boot
001	SPI2 master
010	SPI2 slave
011	Reserved
100	Reserved
101	Reserved
110	Link0 slave
111	UART0 slave

Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement which is important in applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Averaging feature available

Power Supplies

The processors have separate power supply connections for:

- Internal (VDD_INT)
- External (VDD_EXT)
- USB (VDD_USB)
- HADC (VDD_HADC)
- RTC (VDD_RTC)

Table 11. ADSP-SC58x/ADSP-2158x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SYS_FAULT	InOut	**Active-High Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_FAULT}}$	InOut	**Active-Low Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates the device is in the reset state.
SYS_XTAL0	Output	**Crystal Output.**
SYS_XTAL1	Output	**Crystal Output.**
TM_ACI[n]	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLK[n]	Input	**Alternate Clock n.** Provides an additional time base for an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for all GP timers.
TM_TMR[n]	InOut	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_D[nn]	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	InOut	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	InOut	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receives input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input.** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.
USB_DM	InOut	**Data –.** Bidirectional differential data line.
USB_DP	InOut	**Data +.** Bidirectional differential data line.
USB_ID	Input	**OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device).The input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. Can be configured as open-drain. Polarity is configurable as well.
USB_VBUS	InOut	**Bus Voltage.** Connects to bus voltage in host and device modes.
USB_XTAL	Output	**Crystal.** Drives an external crystal. Must be left unconnected if an external clock is driving USB_CLKIN.

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_CK	DMC0 Clock (complement)	Not Muxed	DMC0_CK
DMC0_CS0	DMC0 Chip Select 0	Not Muxed	DMC0_CS0
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
DMC0_LDQS	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	DMC0_LDQS
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
DMC0_RAS	DMC0 Row Address Strobe	Not Muxed	DMC0_RAS
DMC0_RESET	DMC0 Reset (DDR3 only)	Not Muxed	DMC0_RESET
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
DMC0_UDQS	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	DMC0_UDQS
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
DMC0_WE	DMC0 Write Enable	Not Muxed	DMC0_WE
DMC1_A00	DMC1 Address 0	Not Muxed	DMC1_A00
DMC1_A01	DMC1 Address 1	Not Muxed	DMC1_A01
DMC1_A02	DMC1 Address 2	Not Muxed	DMC1_A02
DMC1_A03	DMC1 Address 3	Not Muxed	DMC1_A03
DMC1_A04	DMC1 Address 4	Not Muxed	DMC1_A04
DMC1_A05	DMC1 Address 5	Not Muxed	DMC1_A05
DMC1_A06	DMC1 Address 6	Not Muxed	DMC1_A06
DMC1_A07	DMC1 Address 7	Not Muxed	DMC1_A07
DMC1_A08	DMC1 Address 8	Not Muxed	DMC1_A08
DMC1_A09	DMC1 Address 9	Not Muxed	DMC1_A09
DMC1_A10	DMC1 Address 10	Not Muxed	DMC1_A10
DMC1_A11	DMC1 Address 11	Not Muxed	DMC1_A11
DMC1_A12	DMC1 Address 12	Not Muxed	DMC1_A12
DMC1_A13	DMC1 Address 13	Not Muxed	DMC1_A13
DMC1_A14	DMC1 Address 14	Not Muxed	DMC1_A14
DMC1_A15	DMC1 Address 15	Not Muxed	DMC1_A15
DMC1_BA0	DMC1 Bank Address 0	Not Muxed	DMC1_BA0
DMC1_BA1	DMC1 Bank Address 1	Not Muxed	DMC1_BA1

Table 19. ADSP-SC58x/ADSP-2158x 529-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
VDD_PCIE	PCIE Supply Voltage	Not Muxed	VDD_PCIE
VDD_PCIE_RX	PCIE RX Supply Voltage	Not Muxed	VDD_PCIE_RX
VDD_PCIE_TX	PCIE TX Supply Voltage	Not Muxed	VDD_PCIE_TX
VDD_RTC	RTC VDD	Not Muxed	VDD_RTC
VDD_USB	USB VDD	Not Muxed	VDD_USB

Parameter		Conditions	450 MHz Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 450 MHz ASF_{SHARC1} = 0.31 ASF_{SHARC2} = 0.31 ASF_{A5} = 0.29 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 1.1 V		495		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 450 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.73 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) FFT accelerator operating at $f_{SYSCLK/4}$ DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.1 V		1112		mA
I_{DD_INT}[11]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, PCIe, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups including JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals JTAG_TRST, USB0_VBUS, USB1_VBUS.
[9] Applies to signals PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-15, PG0-5, DAI0_PINx, DAI1_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USBx_DM, USBx_DP, and USBx_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC58x/2158x SHARC+ Processors" (EE-392) for further information.

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC1\_DYN} + I_{DD\_INT\_CCLK\_SHARC2\_DYN} + I_{DD\_INT\_CCLK\_A5\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_USB\_DYN} + I_{DD\_INT\_MLB\_DYN} + I_{DD\_INT\_GIGE\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN} + I_{DD\_INT\_PCIE\_DYN}$$

$I_{DD\_INT\_STATIC}$ is the sole contributor to the static power dissipation component and is specified as a function of voltage (V_{DD_INT}) and junction temperature (T_J) in Table 31.

Table 31. Static Current—$I_{DD\_INT\_STATIC}$ (mA)

	Voltage (V_{DD_INT})		
T_J (°C)	**1.05**	**1.10**	**1.15**
–40	7	8	10
–20	12	14	17
–10	16	19	23
0	21	25	30
10	28	33	39
25	42	49	58
40	63	73	84
55	92	106	122
70	133	152	175
85	190	216	247
100	269	305	346
105	302	342	387
115	376	425	480
125	466	525	592
133	552	621	700

The other 14 addends in the $I_{DD\_INT\_TOT}$ equation comprise the dynamic power dissipation component and fall into four broad categories: application-dependent currents, clock currents, currents from high-speed peripheral operation, and data transmission currents.

Application Dependent Current

The application dependent currents include the dynamic current in the core clock domain of the two SHARC+ cores and the ARM Cortex-A5 core, as well as the dynamic current in the accelerator block.

Dynamic current consumed by the core is subject to an activity scaling factor (ASF) that represents application code running on the processor cores (see Table 32 and Table 33). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent dynamic current data in Table 34 and Table 35, respectively, to calculate this portion of the total dynamic power dissipation component.

$I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ = Table 34 × ASF_{SHARC1}
$I_{DD\_INT\_CCLK\_SHARC2\_DYN}$ = Table 34 × ASF_{SHARC2}
$I_{DD\_INT\_CCLK\_A5\_DYN}$ = Table 35 × ASF_{A5}

Table 32. Activity Scaling Factors for the SHARC+ Core1 and Core2 (ASF_{SHARC1} and ASF_{SHARC2})

I_{DD_INT} Power Vector	**ASF**
$I_{DD\text{-}IDLE}$	0.31
$I_{DD\text{-}NOP}$	0.53
$I_{DD\text{-}TYP\_3070}$	0.74
$I_{DD\text{-}TYP\_5050}$	0.87
$I_{DD\text{-}TYP\_7030}$	1.00
$I_{DD\text{-}PEAK\_100}$	1.14

Table 33. Activity Scaling Factors for the ARM Cortex-A5 Core (ASF_{A5})

I_{DD_INT} Power Vector	**ASF**
$I_{DD\text{-}IDLE}$	0.29
$I_{DD\text{-}DHRYSTONE}$	0.73
$I_{DD\text{-}TYP\_2575}$	0.57
$I_{DD\text{-}TYP\_5050}$	0.80
$I_{DD\text{-}TYP\_7525}$	1.00
$I_{DD\text{-}PEAK\_100}$	1.21

HADC

HADC Electrical Characteristics

Table 37. HADC Electrical Characteristics

Parameter	Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down.	10	µA

HADC DC Accuracy

Table 38. HADC DC Accuracy[1]

Parameter	Typ	Unit[2]
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±8	LSB
Offset Error Matching	±10	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 4096.

HADC Timing Specifications

Table 39. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

TMU

TMU Characteristics

Table 40. TMU Characteristics

Parameter	Typ	Unit
Resolution	1	°C
Accuracy	±6	°C

Asynchronous Read

Table 45 and Figure 12 show asynchronous memory read timing, related to the SMC.

Table 45. Asynchronous Read

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	5.1		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0.7		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
t_{AMSARE}	ADDR/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK0} – 2		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	(RST + PREAT) × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	RHT × t_{SCLK0} –2		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	RAT × t_{SCLK0} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$, $\overline{SMC0\_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

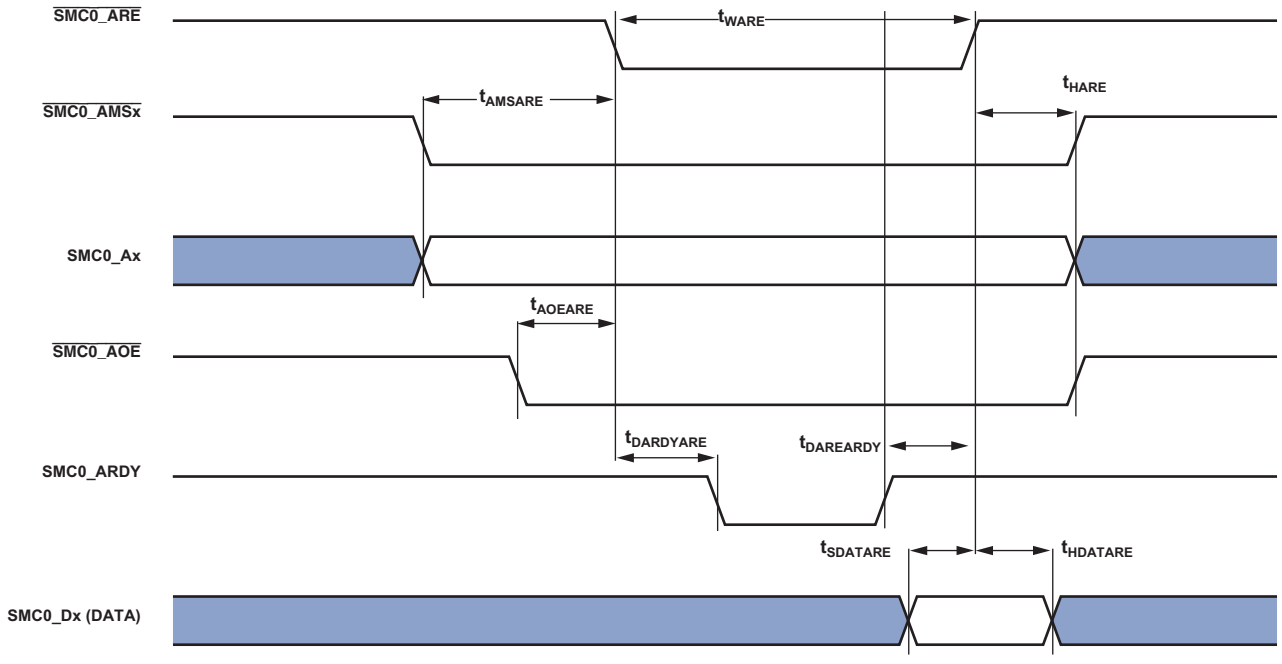

Figure 12. Asynchronous Read

DDR2 SDRAM Clock and Control Cycle Timing

Table 51 and Figure 17 show DDR2 SDRAM clock and control cycle timing, related to the DMC.

Table 51. DDR2 SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		400 MHz[2] Min	400 MHz[2] Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.5		ns
$t_{CH\ (abs)}$[3]	Minimum Clock Pulse Width	0.44	0.56	t_{CK}
$t_{CL\ (abs)}$[3]	Maximum Clock Pulse Width	0.44	0.56	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	175		ps
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	250		ps

[1] Specifications apply to both DMC0 and DMC1.
[2] In order to ensure proper operation of the DDR2, all the DDR2 guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[3] As per JESD79-2E definition.

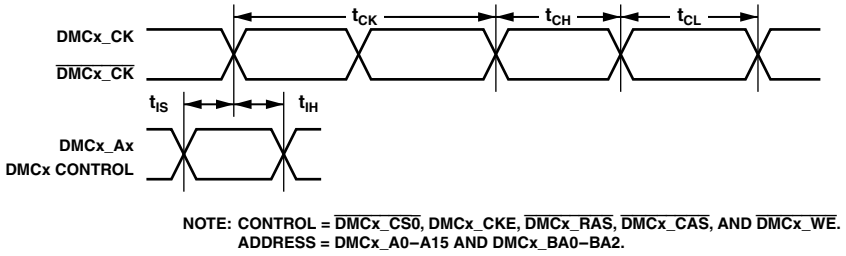

Figure 17. DDR2 SDRAM Clock and Control Cycle Timing

Table 65. Serial Ports—Internal Clock[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	Frame Sync Setup Before SPTx_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[2]	12		ns
t_{HFSI}	Frame Sync Hold After SPTx_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[2]	–0.5		ns
t_{SDRI}	Receive Data Setup Before SPTx_CLK[2]	3.4		ns
t_{HDRI}	Receive Data Hold After SPTx_CLK[2]	1.5		ns
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		3.5	ns
t_{HOFSI}	Frame Sync Hold After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	–2.5		ns
t_{DDTI}	Transmit Data Delay After SPTx_CLK[3]		3.5	ns
t_{HDTI}	Transmit Data Hold After SPTx_CLK[3]	–2.5		ns
t_{SCLKIW}	SPTx_CLK Width[4]	$0.5 \times t_{SPTCLKPROG} - 1.5$		ns
t_{SPTCLK}	SPTx_CLK Period[4]	$t_{SPTCLKPROG} - 1.5$		ns

[1] Specifications apply to all eight SPORTs.
[2] Referenced to the sample edge.
[3] Referenced to drive edge.
[4] See Table 29 for details on the minimum period that can be programmed for $t_{SPTCLKPROG}$.

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 76. SPI Port—SPIx_RDY Master Timing[1]

Parameter		Conditions	Min	Max	Unit
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	Baud = 0, CPHA = 0	$4.5 \times t_{SCLK1}$	$5.5 \times t_{SCLK1} + 10$	ns
		Baud = 0, CPHA = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 0	$(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns
		Baud > 0, CPHA = 1	$(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

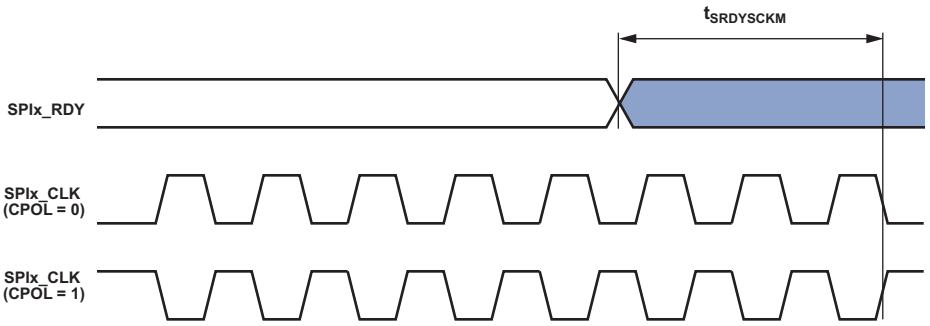

Figure 48. SPIx_RDY Setup Before SPIx_CLK

PWM — Heightened Precision (HP) Mode Timing

Table 84 and Table 85 and Figure 56 and Figure 57 describe heightened precision (HP) PWM operations.

Table 84. PWM—HP Mode, Output Pulse

Parameter		Min	Max	Unit
Switching Characteristics				
t_{HPWMW}	HP PWM Output Pulse Width[1, 2]	$(N + m \times 0.25) \times t_{SCLK} - 0.5$	$(N + m \times 0.25) \times t_{SCLK} + 0.5$	ns

[1] N is the DUTY bit field (coarse duty) from the duty register. m is the ENHDIV (Enhanced Precision Divider bits) value from the HP duty register.
[2] Applies to individual PWM channel with 50% duty cycle. Other PWM channels within the same unit are toggling at the same time. No other GPIO pins toggle.

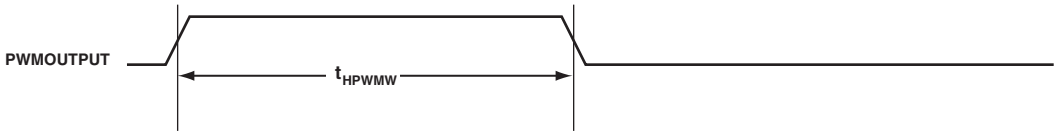

Figure 56. PWM HP Mode Timing, Output Pulse

Table 85. PWM—HP Mode, Output Skew

Parameter		Min	Max	Unit
Switching Characteristics				
t_{HPWMS}	HP PWM Output Skew [1]		1.0	ns

[1] Output edge difference between any two PWM channels (AH, AL, BH, BL, CH, CL, DH and DL) in the same PWM unit (a unit is PWMx where x = 0, 1, 2), with the same HP edge placement.

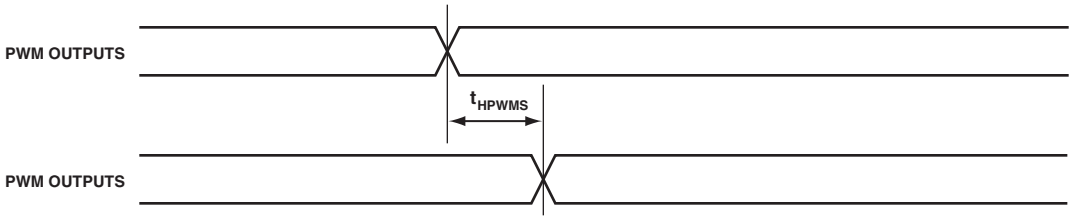

Figure 57. PWM HP Mode Timing, Output Skew

Table 90. 10/100 EMAC Timing—RMII Station Management[1]

Parameter[2]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	10.8		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK0} + 2	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK0} –2.9		ns

[1] These specifications apply to ETH0 and ETH1.
[2] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock with a minimum period that is programmable as a multiple of the system clock SCLK0. ETHx_MDIO is a bidirectional data line.

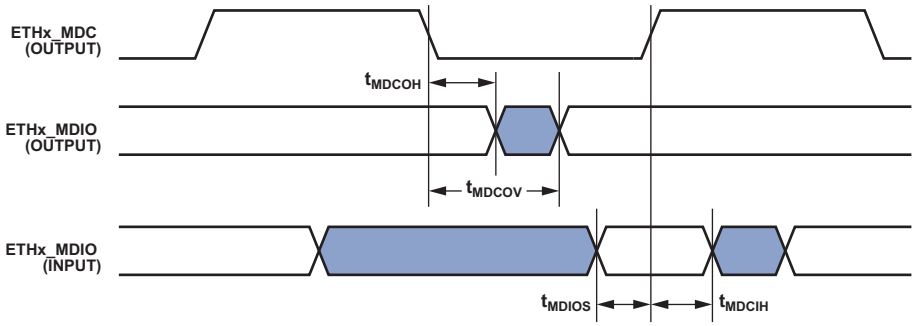

Figure 61. 10/100 Ethernet MAC Controller Timing—RMII Station Management

Sony/Philips Digital Interface (S/PDIF) Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter Serial Input Waveforms

Figure 64 and Table 93 show the right justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right justified to the next frame sync transition.

Table 93. S/PDIF Transmitter Right Justified Mode

Parameter		Conditions	Nominal	Unit
Timing Requirement				
t_{RJD}	Frame Sync to MSB Delay in Right Justified Mode	16-bit word mode	16	SCLK
		18-bit word mode	14	SCLK
		20-bit word mode	12	SCLK
		24-bit word mode	8	SCLK

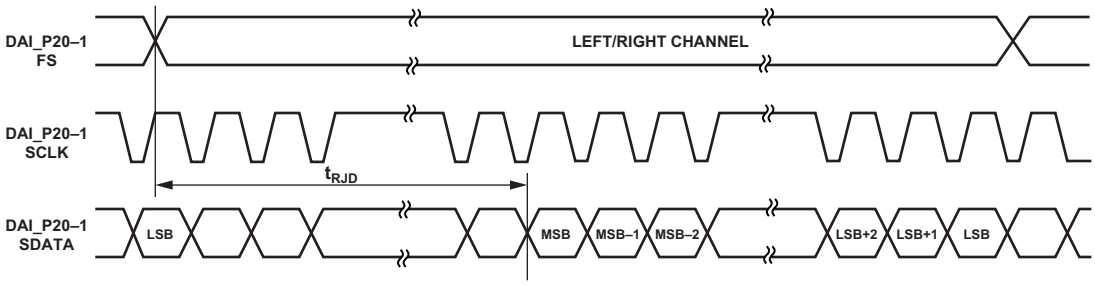

Figure 64. Right Justified Mode

Mobile Storage Interface (MSI) Controller Timing

Table 101 and Figure 74 show I/O timing related to the MSI.

Table 101. MSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	4.8		ns
t_{IH}	Input Hold Time	–0.5		ns
Switching Characteristics				
f_{PP}	Clock Frequency Data Transfer Mode[1]		50	MHz
t_{WL}	Clock Low Time	8		ns
t_{WH}	Clock High Time	8		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		2	ns
t_{OH}	Output Hold Time	–1.8		ns

[1] $t_{PP} = 1/f_{PP}$.

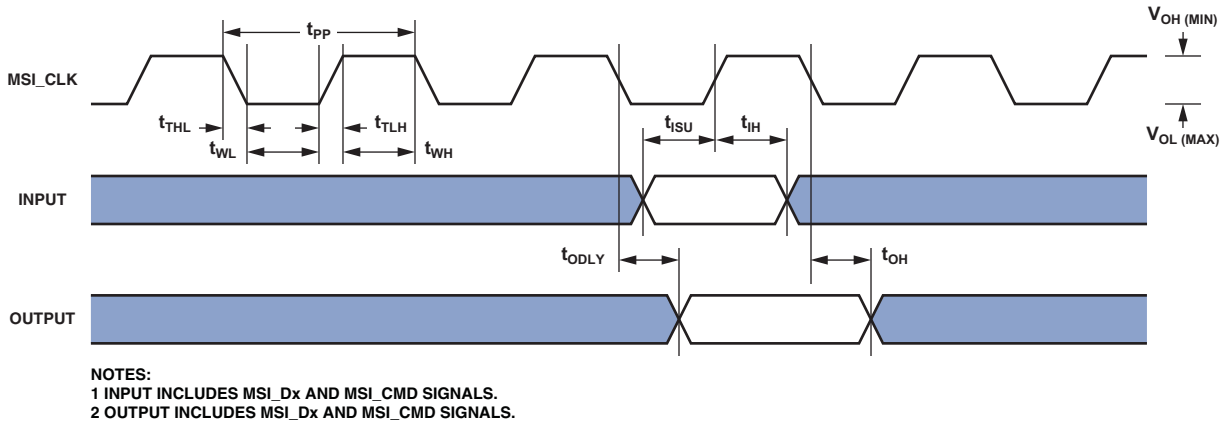

Figure 74. MSI Controller Timing

ADSP-SC58x/ADSP-2158x 529-BALL BGA BALL ASSIGNMENTS

The ADSP-SC58x/ADSP-2158x 529-Ball BGA Ball Assignments (Numerical by Ball Number) table lists the 529-ball BGA package by ball number.

The ADSP-SC58x/ADSP-2158x 529-Ball BGA Ball Assignments (Alphabetical by Pin Name) table lists the 529-ball BGA package by pin name.

ADSP-SC58x/ADSP-2158x 529-BALL BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	B19	DMC1_DQ11	D14	DMC1_BA2	F09	GND
A02	DMC0_UDQS	B20	DMC1_DQ12	D15	DMC1_CAS	F10	VDD_INT
A03	DMC0_CK	B21	DMC1_DQ14	D16	DMC1_RAS	F11	VDD_INT
A04	DMC0_CK	B22	PD_00	D17	DMC1_A09	F12	VDD_INT
A05	DMC0_DQ09	B23	PD_04	D18	DMC1_A15	F13	VDD_INT
A06	DMC0_LDQS	C01	DMC0_DQ14	D19	DMC1_A10	F14	VDD_INT
A07	DMC0_LDQS	C02	DMC0_DQ13	D20	DMC1_A11	F15	VDD_INT
A08	DMC0_DQ05	C03	DMC0_CS0	D21	PC_14	F16	GND
A09	DMC0_DQ03	C04	DMC0_CKE	D22	PD_10	F17	VDD_INT
A10	DMC0_DQ01	C05	DMC0_LDM	D23	PD_09	F18	VDD_INT
A11	DMC1_DQ03	C06	DMC1_RESET	E01	DMC0_A04	F19	VDD_INT
A12	DMC1_DQ00	C07	DMC1_A03	E02	DMC0_RAS	F20	PE_06
A13	DMC1_LDQS	C08	DMC1_A00	E03	DMC0_BA1	F21	PD_02
A14	DMC1_LDQS	C09	DMC1_A01	E04	DMC0_WE	F22	PD_13
A15	DMC1_VREF	C10	DMC1_A04	E05	DMC0_RZQ	F23	PD_12
A16	DMC1_CK	C11	DMC1_A06	E06	GND	G01	DMC0_A13
A17	DMC1_CK	C12	DMC1_BA1	E07	GND	G02	DMC0_A09
A18	DMC1_DQ09	C13	DMC1_ODT	E08	GND	G03	DMC0_A03
A19	DMC1_UDQS	C14	DMC1_CS0	E09	GND	G04	DMC0_A11
A20	DMC1_UDQS	C15	DMC1_LDM	E10	VDD_INT	G05	VDD_INT
A21	DMC1_DQ13	C16	DMC1_UDM	E11	VDD_INT	G06	VDD_DMC
A22	DMC1_DQ15	C17	DMC1_A14	E12	VDD_INT	G07	VDD_DMC
A23	GND	C18	DMC1_A12	E13	VDD_INT	G08	VDD_DMC
B01	DMC0_UDQS	C19	DMC1_A13	E14	VDD_INT	G09	VDD_DMC
B02	DMC0_DQ12	C20	PC_13	E15	VDD_INT	G10	VDD_DMC
B03	DMC0_DQ11	C21	PD_01	E16	VDD_INT	G11	VDD_DMC
B04	DMC0_DQ10	C22	PD_06	E17	VDD_INT	G12	VDD_DMC
B05	DMC0_DQ08	C23	PD_05	E18	VDD_INT	G13	VDD_DMC
B06	DMC0_DQ06	D01	DMC0_VREF	E19	DMC1_RZQ	G14	VDD_DMC
B07	DMC0_DQ07	D02	DMC0_DQ15	E20	PC_15	G15	VDD_DMC
B08	DMC0_DQ04	D03	DMC0_BA0	E21	PD_08	G16	VDD_DMC
B09	DMC0_DQ02	D04	DMC0_BA2	E22	PD_14	G17	VDD_DMC
B10	DMC0_DQ00	D05	DMC0_ODT	E23	PD_11	G18	VDD_DMC
B11	DMC1_DQ01	D06	DMC0_UDM	F01	DMC0_A01	G19	VDD_INT
B12	DMC1_DQ02	D07	DMC1_A05	F02	DMC0_A06	G20	PE_04
B13	DMC1_DQ04	D08	DMC1_WE	F03	DMC0_CAS	G21	PE_13
B14	DMC1_DQ05	D09	DMC1_A07	F04	DMC0_A02	G22	PE_01
B15	DMC1_DQ06	D10	DMC1_A02	F05	DMC0_A07	G23	PE_00
B16	DMC1_DQ07	D11	DMC1_BA0	F06	GND	H01	DMC0_A14
B17	DMC1_DQ08	D12	DMC1_A08	F07	VDD_INT	H02	DMC0_A12
B18	DMC1_DQ10	D13	DMC1_CKE	F08	VDD_INT	H03	DMC0_A05

ORDERING GUIDE

Model[1]	Processor Instruction Rate (Max)	Temperature Range[2]	ARM Cores[3]	SHARC+ Cores	SHARC+ SRAM	PCIe Lanes[3]	Package Description	Package Option
ADSP-21583KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21583CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584KBCZ-4A	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584BBCZ-4A	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21584CBCZ-4A	450 MHz	–40°C to +95°C	N/A	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-21587KBCZ-4B	450 MHz	0°C to +70°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-21587BBCZ-4B	450 MHz	–40°C to +85°C	N/A	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC582KBCZ-4A	450 MHz	0°C to +70°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582BBCZ-4A	450 MHz	–40°C to +85°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC582CBCZ-4A	450 MHz	–40°C to +95°C	1	1	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-3A	300 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-3A	300 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-3A	300 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583KBCZ-4A	450 MHz	0°C to +70°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583BBCZ-4A	450 MHz	–40°C to +85°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC583CBCZ-4A	450 MHz	–40°C to +95°C	1	2	384 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-3A	300 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-3A	300 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-3A	300 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584KBCZ-4A	450 MHz	0°C to +70°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584BBCZ-4A	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC584CBCZ-4A	450 MHz	–40°C to +95°C	1	2	640 kB	N/A	349-Ball cspBGA	BC-349-1
ADSP-SC587KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC587BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	N/A	529-Ball cspBGA	BC-529-1
ADSP-SC589KBCZ-4B	450 MHz	0°C to +70°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1
ADSP-SC589BBCZ-4B	450 MHz	–40°C to +85°C	1	2	640 kB	1	529-Ball cspBGA	BC-529-1

[1] Z =RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.

[3] N/A means not applicable.