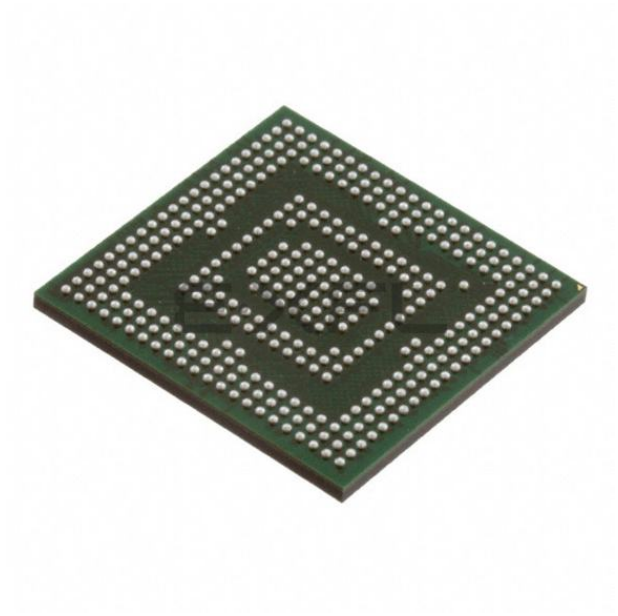

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	640kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc584kbcz-5a

ADC Control Module (ACM) Interface

The ADC control module (ACM) provides an interface that synchronizes the controls between the processors and an ADC. The analog-to-digital conversions are initiated by the processors, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process, generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by an internal DAI routing of the ACM with the SPORT0 block.

The processors interface directly to many ADCs without any glue logic required.

3-Phase Pulse Width Modulator (PWM) Units

The pulse width modulator (PWM) module is a flexible and programmable waveform generator. With minimal CPU intervention, the PWM generates complex waveforms for motor control, pulse coded modulation (PCM), DAC conversions, power switching, and power conversion. The PWM module has four PWM pairs capable of 3-phase PWM generation for source inverters for ac induction and dc brushless motors.

Each of the three 3-phase PWM generation units features the following:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single update mode with an option for asymmetric duty
- Programmable dead time and switching frequency
- Programmable dead time per channel
- Twos complement implementation which permits smooth transition to full on and full off states
- Dedicated asynchronous PWM shutdown signal

Ethernet Media Access Controller (EMAC)

The processor features two ethernet media access controllers (EMACs): 10/100 Ethernet and 10/100/1000/AVB Ethernet with precision time protocol IEEE 1588.

The processors can directly connect to a network through embedded fast EMAC that supports 10-BaseT (10 Mb/sec), 100-BaseT (100 Mb/sec) and 1000-BaseT (1 Gb/sec) operations. The 10/100 EMAC peripheral on the processors is fully compliant to the IEEE 802.3-2002 standard. The peripheral provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features of the EMAC are as follows:

- Support and RMII/RGMII protocols for external PHYs
- Full-duplex and half-duplex modes
- Media access management (in half-duplex operation)
- Flow control
- Station management, including the generation of MDC/MDIO frames for read/write access to PHY registers

Some advanced features of the EMAC are as follows:

- Automatic checksum computation of IP header and IP payload fields of receive frames
- Independent 32-bit descriptor driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Transmit DMA support for separate descriptors for MAC header and payload fields to eliminate buffer copy operations
- Convenient frame alignment modes
- 47 MAC management statistics counters with selectable clear on read behavior and programmable interrupts on half maximum value
- Advanced power management
- Magic packet detection and wakeup frame filtering
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression

Audio Video Bridging (AVB) Support (10/100/1000 EMAC Only)

The 10/100/1000 EMAC supports the following audio video (AVB) features:

- Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes
- IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Configuring up to two additional channels (Channel 1 and Channel 2) on the transmit and receive paths for AV traffic. Channel 0 is available by default and carries the legacy best effort Ethernet traffic on the transmit side.
- Separate DMA, transmit and receive FIFO for AVB latency class
- Programmable control to route received VLAN tagged non AV packets to channels or queues

Precision Time Protocol (PTP) IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC).

This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the engine are as follows:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D02	SMC0 Data 2	E	PE_10
SMC0_D03	SMC0 Data 3	E	PE_09
SMC0_D04	SMC0 Data 4	E	PE_00
SMC0_D05	SMC0 Data 5	D	PD_15
SMC0_D06	SMC0 Data 6	D	PD_14
SMC0_D07	SMC0 Data 7	D	PD_00
SMC0_D08	SMC0 Data 8	B	PB_14
SMC0_D09	SMC0 Data 9	B	PB_13
SMC0_D10	SMC0 Data 10	B	PB_12
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_10
SMC0_D13	SMC0 Data 13	B	PB_09
SMC0_D14	SMC0 Data 14	B	PB_08
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_10
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_11
SPI0_RDY	SPI0 Ready	C	PC_12
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_07
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	D	PD_01
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	C	PC_12
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	C	PC_00
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	E	PE_01
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	E	PE_02
$\overline{\text{SPI0\_SEL7}}$	SPI0 Slave Select Output 7	E	PE_03
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	D	PD_01
SPI1_CLK	SPI1 Clock	E	PE_13
SPI1_MISO	SPI1 Master In, Slave Out	E	PE_14
SPI1_MOSI	SPI1 Master Out, Slave In	E	PE_15
SPI1_RDY	SPI1 Ready	E	PE_08
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_13
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	E	PE_07
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	E	PE_11
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	E	PE_12
$\overline{\text{SPI1\_SEL5}}$	SPI1 Slave Select Output 5	E	PE_08
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	E	PE_11
SPI2_CLK	SPI2 Clock	C	PC_01
SPI2_D2	SPI2 Data 2	C	PC_04
SPI2_D3	SPI2 Data 3	C	PC_05
SPI2_MISO	SPI2 Master In, Slave Out	C	PC_02
SPI2_MOSI	SPI2 Master Out, Slave In	C	PC_03
SPI2_RDY	SPI2 Ready	E	PE_12
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	C	PC_06
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	E	PE_03
$\overline{\text{SPI2\_SEL3}}$	SPI2 Slave Select Output 3	E	PE_04
$\overline{\text{SPI2\_SEL4}}$	SPI2 Slave Select Output 4	E	PE_05
$\overline{\text{SPI2\_SEL5}}$	SPI2 Slave Select Output 5	E	PE_06
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	C	PC_06

Table 12. ADSP-SC58x/ADSP-2158x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART1_RTS	UART1 Request to Send	E	PE_02
UART1_RX	UART1 Receive	B	PB_03
UART1_TX	UART1 Transmit	B	PB_02
UART2_CTS	UART2 Clear to Send	E	PE_11
UART2_RTS	UART2 Request to Send	E	PE_10
UART2_RX	UART2 Receive	D	PD_13
UART2_TX	UART2 Transmit	D	PD_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Negative Data (–)	Not Muxed	USB0_DM
USB0_DP	USB0 Positive Data (+)	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

GPIO MULTIPLEXING FOR THE 349-BALL CSP_BGA PACKAGE

Table 13 through Table 17 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 349-ball CSP_BGA package.

Table 13. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	ETH0_TXD0			SMC0_A21	
PA_01	ETH0_TXD1			SMC0_A20	
PA_02	ETH0_MDC			SMC0_A24	
PA_03	ETH0_MDIO			SMC0_A23	
PA_04	ETH0_RXD0			SMC0_A19	
PA_05	ETH0_RXD1			SMC0_A18	
PA_06	ETH0_RXCLK_REFCLK			SMC0_A17	
PA_07	ETH0_CRS			SMC0_A16	
PA_08	ETH0_RXD2			SMC0_A12	
PA_09	ETH0_RXD3			SMC0_A11	
PA_10	ETH0_TXEN			SMC0_A22	
PA_11	ETH0_TXCLK			SMC0_A15	
PA_12	ETH0_TXD2			SMC0_A14	
PA_13	ETH0_TXD3			SMC0_A13	
PA_14	ETH0_PTPPPS3	SINC0_D0		SMC0_A10	
PA_15	ETH0_PTPPPS2	SINC0_D1		SMC0_A09	

Table 14. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_PTPPPS1	SINC0_D2	PPI0_D14	SMC0_A08	TM0_ACLK3
PB_01	ETH0_PTPPPS0	SINC0_CLK0	PPI0_D15	SMC0_A07	TM0_ACLK4
PB_02	ETH0_PTPCLKIN0	$\overline{\text{UART1\_TX}}$	PPI0_D16	SMC0_A04	
PB_03	ETH0_PTPAUXIN0	$\overline{\text{UART1\_RX}}$	PPI0_D17	SMC0_A03	TM0_ACI1
PB_04	MLB0_CLK	SINC0_D3	PPI0_D12	SMC0_ARDY	ETH0_PTPAUXIN1
PB_05	MLB0_SIG		PPI0_D13	SMC0_A01	ETH0_PTPAUXIN2
PB_06	MLB0_DAT		PWM0_BH	SMC0_A02	ETH0_PTPAUXIN3
PB_07	LP1_D0	PWM0_AH	TM0_TMR3	SMC0_D15	
PB_08	LP1_D1	PWM0_AL	TM0_TMR4	SMC0_D14	
PB_09	LP1_D2		CAN1_TX	SMC0_D13	
PB_10	LP1_D3	TM0_TMR2	CAN1_RX	SMC0_D12	TM0_ACI4
PB_11	LP1_D4		PWM0_DH	SMC0_D11	CNT0_ZM
PB_12	LP1_D5		PWM0_DL	SMC0_D10	CNT0_UD
PB_13	LP1_D6		PWM0_CH	SMC0_D09	
PB_14	LP1_D7	TM0_TMR5	PWM0_CL	SMC0_D08	CNT0_DG
PB_15	LP1_ACK	$\overline{\text{PWM0\_TRIP0}}$	TM0_TMR1	$\overline{\text{SMC0\_AWE}}$	

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
DMC1_BA2	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Bank Address Input 2 Notes: No notes
$\overline{\text{DMC1\_CAS}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Column Address Strobe Notes: No notes
DMC1_CK	Output	C	none	none	L	VDD_DMC	Desc: DMC1 Clock Notes: No notes
DMC1_CKE	Output	B	none	none	L	VDD_DMC	Desc: DMC1 Clock enable Notes: No notes
$\overline{\text{DMC1\_CK}}$	Output	C	none	none	L	VDD_DMC	Desc: DMC1 Clock (complement) Notes: No notes
$\overline{\text{DMC1\_CS0}}$	Output	B	none	none	none	VDD_DMC	Desc: DMC1 Chip Select 0 Notes: No notes
DMC1_DQ00	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 0 Notes: No notes
DMC1_DQ01	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 1 Notes: No notes
DMC1_DQ02	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 2 Notes: No notes
DMC1_DQ03	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 3 Notes: No notes
DMC1_DQ04	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 4 Notes: No notes
DMC1_DQ05	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 5 Notes: No notes
DMC1_DQ06	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 6 Notes: No notes
DMC1_DQ07	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 7 Notes: No notes
DMC1_DQ08	InOut	B	Internal logic ensures that input signal does not float	none	none	VDD_DMC	Desc: DMC1 Data 8 Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PD_08	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 8 | LP0 Data 6 | PWM1 Channel C Low Side | TRACE0 Trace Data 6 | TIMER0 Alternate Clock 1 Notes: No notes
PD_09	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 9 | LP0 Data 7 | PWM1 Channel D High Side | TRACE0 Trace Data 7 | TIMER0 Alternate Clock 2 Notes: No notes
PD_10	InOut	H	PullDown	none	none	VDD_EXT	Desc: PORTD Position 10 | LP0 Clock | PWM1 Channel D Low Side | TRACE0 Trace Clock Notes: No notes
PD_11	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 11 | LP0 Acknowledge | PWM1 PWMTMR Grouped Notes: No notes
PD_12	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 12 | EPPI0 Data 19|SMC0 Address 6|UART2 Transmit Notes: No notes
PD_13	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 13 | EPPI0 Data 18|SMC0 Address 5|UART2 Receive | TIMER0 Alternate Capture Input 2 Notes: No notes
PD_14	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 14 | EPPI0 Data 11 | MLB0 Single-Ended Clock Out | PWM2 Shutdown Input 0 | SMC0 Data 6 Notes: No notes
PD_15	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTD Position 15 | EPPI0 Data 10 | PWM2 Channel C High Side | SMC0 Data 5 Notes: No notes
PE_00	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 0 | EPPI0 Data 9 | PWM2 Channel C Low Side | SMC0 Data 4 Notes: No notes
PE_01	InOut	A	PullDown	none	none	VDD_EXT	Desc: PORTE Position 1 | EPPI0 Frame Sync 2 (VSYNC) | SPI0 Slave Select Output 5 | SHARC Core 1 Flag Pin | UART1 Clear to Send Notes: No notes

Table 27. ADSP-SC58x/ADSP-2158x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
TWI0_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
TWI1_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI1 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.
TWI1_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI1 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
TWI2_SCL	InOut	D	none	none	none	VDD_EXT	Desc: TWI2 Serial Clock Notes: Add external pull-up if used. Can be pulled low when not used.
TWI2_SDA	InOut	D	none	none	none	VDD_EXT	Desc: TWI2 Serial Data Notes: Add external pull-up if used. Can be pulled low when not used.
USB0_DM	InOut	F	none	none	none	VDD_USB	Desc: USB0 Data - Notes: Add external pull-down if not used[1]
USB0_DP	InOut	F	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Add external pull-down if not used[1]
USB0_ID	InOut		none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: Connect to GND when USB is not used[1]
USB0_VBC	InOut	E	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: Add external pull-down if not used[1]
USB0_VBUS	InOut	G	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: Connect to GND if not used[1]
USB1_DM	InOut	F	none	none	none	VDD_USB	Desc: USB1 Data - Notes: Add external pull-down if not used[1]
USB1_DP	InOut	F	none	none	none	VDD_USB	Desc: USB1 Data + Notes: Add external pull-down if not used[1]
USB1_VBUS	InOut	G	none	none	none	VDD_USB	Desc: USB1 Bus Voltage Notes: Connect to GND if not used[1]
USB_CLKIN	a		none	none	none		Desc: USB0/USB1 Clock/Crystal Input Notes: Services both USB0 and USB1. Connect to GND if not used.[1]

Table 30. Phase-Locked Loop (PLL) Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	250	900	MHz

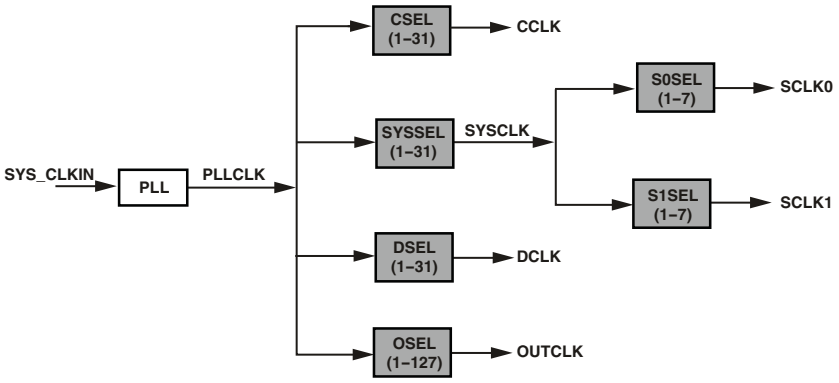


Figure 8. Clock Relationships and Divider Values

HADC

HADC Electrical Characteristics

Table 37. HADC Electrical Characteristics

Parameter	Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down.	10	µA

HADC DC Accuracy

Table 38. HADC DC Accuracy[1]

Parameter	Typ	Unit[2]
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±8	LSB
Offset Error Matching	±10	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 4096.

HADC Timing Specifications

Table 39. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

TMU

TMU Characteristics

Table 40. TMU Characteristics

Parameter	Typ	Unit
Resolution	1	°C
Accuracy	±6	°C

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 41 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 41. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.33 V to +1.26 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2/LPDDR Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
DDR3 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.60 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
Real Time Clock Supply Voltage (V_{DD_RTC})	–0.33 V to +3.60 V
PCIe Transmit Supply Voltage ($V_{DD\_PCIE\_TX}$)	–0.33 V to +1.20 V
PCIe Receive Supply Voltage ($V_{DD\_PCIE\_RX}$)	–0.33 V to +1.20 V
PCIe Supply Voltage (V_{DD_PCIE})	–0.33 V to +3.60 V
HADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V
DDR2/LPDDR Input Voltage[1]	–0.33 V to +1.90 V
DDR3 Input Voltage[1]	–0.33 V to +1.60 V
Digital Input Voltage[2, 3]	–0.33 V to +3.60 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} +0.5 V
Analog Input Voltage	–0.2 V to V_{DD_HADC} +0.2 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	133°C

[1] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.
[2] Applies to 100% transient duty cycle.
[3] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 42 provides details about the package branding for the processors. For a complete listing of product availability, see the Ordering Guide section.

Figure 9. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 42. Package Brand Information

Brand Key	Field Description
ADSP-SC589	Product name
t	Temperature range
pp	Package type
Z	RoHS compliant option
ccc	See the Ordering Guide section
vvvvvv.x	Assembly lot code
n.n	Silicon revision
#	RoHS compliant designation
yyww	Date code

Clock and Reset Timing

Table 44 and Figure 11 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLK, DCLK, and OCLK timing specifications in Table 29, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 44. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKINx Frequency (Crystal)[1, 2, 3]	20	50	MHz
	SYS_CLKINx Frequency (External CLKIN)[1, 2, 3]	20	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 11) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 43 and Figure 10 for power-up reset timing.

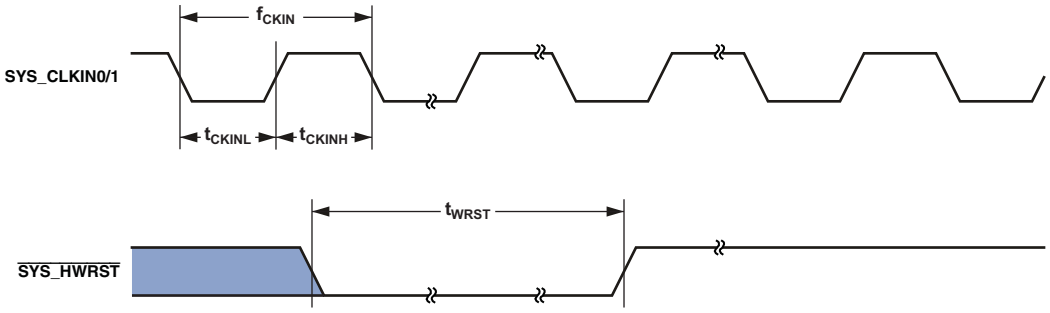


Figure 11. Clock and Reset Timing

Mobile DDR (LPDDR) SDRAM Clock and Control Cycle Timing

Table 54 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the DMC.

Table 54. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMCx} Nominal 1.8 V[1]

Parameter		200 MHz[2] Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMCx_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMCx_CK Rise	1		ns

[1] Specifications apply to both DMC0 and DMC1.
[2] To ensure proper operation of LPDDR, all the LPDDR guidelines must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

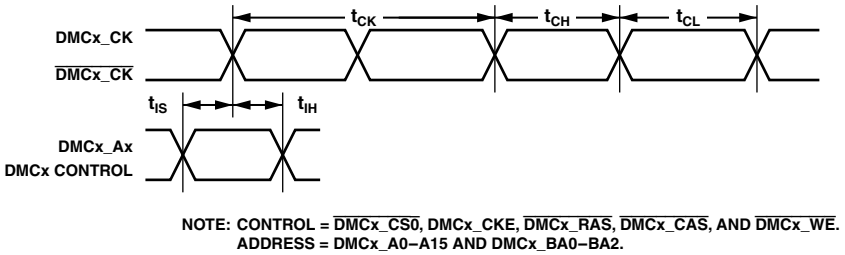


Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

Enhanced Parallel Peripheral Interface (EPPI) Timing

Table 60 and Table 61 and Figure 26 through Figure 34 describe enhanced parallel peripheral interface (EPPI) timing operations. In Figure 26 through Figure 34, POLC[1:0] represents the setting of the EPPI_CTL register, which sets the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated, the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 60. Enhanced Parallel Peripheral Interface (EPPI)—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	0		ns
Switching Characteristics				
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 1.5$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 1.5$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		3.5	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–0.5		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		3.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–0.5		ns

[1] See Table 29 for details on the minimum period that can be programmed for $t_{PCLKPROG}$.

SPI Port—Slave Timing

Table 72 and Figure 44 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 72. SPI Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLK} - 1$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

[1] All specifications apply to all three SPIs.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in Table 29.

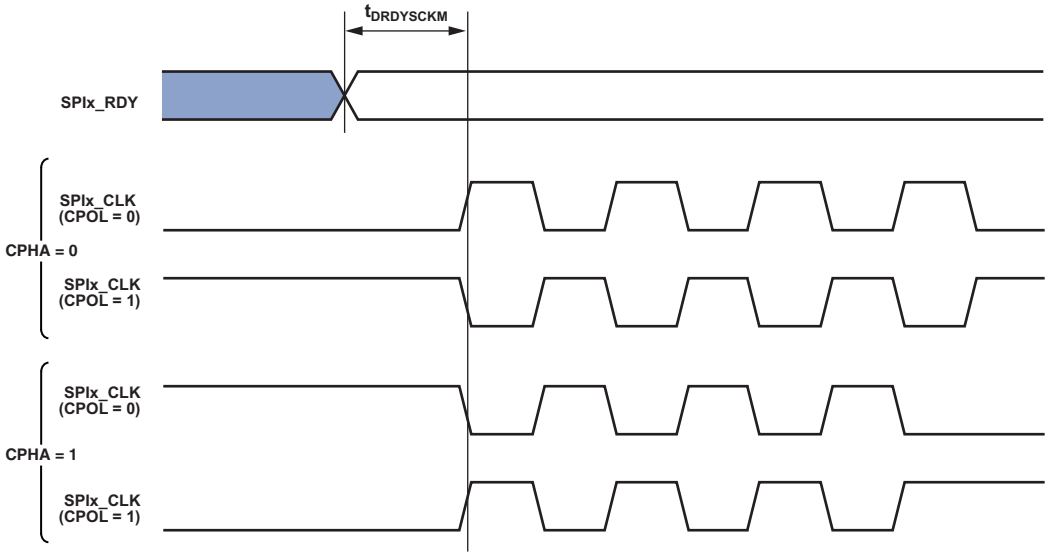


Figure 49. SPIx_CLK Switching Diagram After SPIx_RDY Assertion

General-Purpose I/O Port Timing

Table 78 and Figure 51 describe I/O timing, related to the general-purpose I/O port (PORT).

Table 78. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

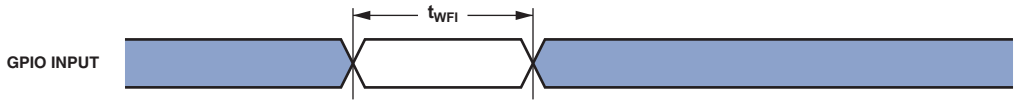


Figure 51. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 79, Table 80, and Figure 52 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of $f_{SCLK}/4$ MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 79. Timer Cycle Timing (Internal Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)[2]	$t_{SCLK} \times WIDTH - 1.5$	$t_{SCLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Table 80. Timer Cycle Timing (External Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times WIDTH - 1.5$	$t_{EXT\_CLK} \times WIDTH + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency see the $f_{TMRCLKEXT}$ specification in Table 29.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.

Controller Area Network (CAN) Interface

The CAN interface timing is described in the ADSP-SC58x/ADSP-2158x SHARC+ Processor Hardware Reference.

Universal Serial Bus (USB) OTG—Receive and Transmit Timing

Table 87 describes the USB OTG receive and transmit operations.

Table 87. USB OTG—Receive and Transmit Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
f_{USBS}	USB_XI Frequency	24	24	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

[1] This specification is supported by USB0.

PCI Express (PCIe)

The PCIe interface complies with the Gen1 and Gen2 x1 lane data rate specification and supports up to 3.0 PCIe base functionality.

For more information about PCIe, see the following standards:

- *PCI Express Base 3.0 Specification*, Revision 1.0, PCI-SIG
- *PCI Express 2.0 Card Electromechanical Specification*, Revision 2.0, PCI-SIG
- *PHY Interface for the PCI Express Architecture*, Revision 2.0, Intel Corporation
- *PCI-SIG Engineering Change Request: L1 Substates*, February 1, 2012, PCI-SIG
- *IEEE Standard 1149.1-2001*, IEEE
- *IEEE Standard 1149.6-2003*, IEEE

10/100 EMAC Timing (ETH0 and ETH1)

Table 88 through Table 90 and Figure 59 through Figure 61 describe the 10/100 EMAC operations.

Table 88. 10/100 EMAC Timing—RMII Receive Signal[1]

Parameter[2]		Min	Max	Unit
Timing Requirements				
$t_{REFCLKF}$	ETHx_REFCLK Frequency (f_{SCLK0} = SCLK0 Frequency)		50 + 1%	MHz
$t_{REFCLKW}$	ETHx_REFCLK Width ($t_{REFCLKF}$ = ETHx_REFCLK Period)	$t_{REFCLKF} \times 35\%$	$t_{REFCLKF} \times 65\%$	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETHx_REFCLK Rising Edge (Data In Setup)	1.75		ns
$t_{REFCLKIH}$	RMII ETHx_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	1.6		ns

[1] These specifications apply to ETH0 and ETH1.
[2] RMII inputs synchronous to RMII ETHx_REFCLK are ETHx_RXD1–0, RMII ETHx_CRS, and ERxER.

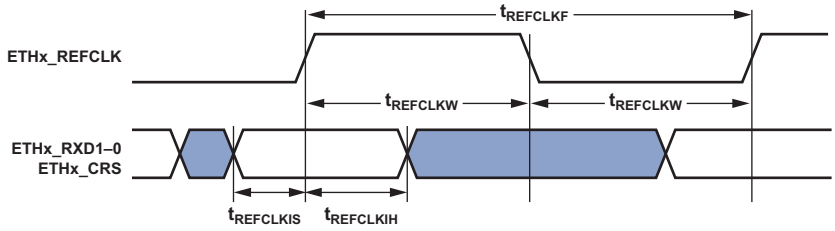


Figure 59. 10/100 EMAC Controller Timing—RMII Receive Signal

Table 89. 10/100 EMAC Timing—RMII Transmit Signal[1]

Parameter[2]		Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		11.9	ns
$t_{REFCLKOH}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] These specifications apply to ETH0 and ETH1.
[2] RMII outputs synchronous to RMII ETHx_REFCLK are ETHx_TXD1–0.

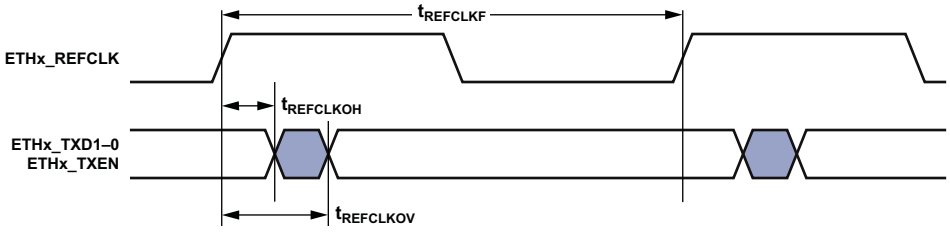


Figure 60. 10/100 EMAC Controller Timing—RMII Transmit Signal

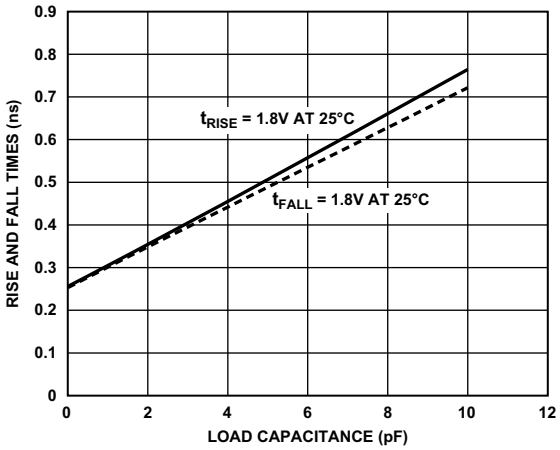


Figure 96. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for DDR2

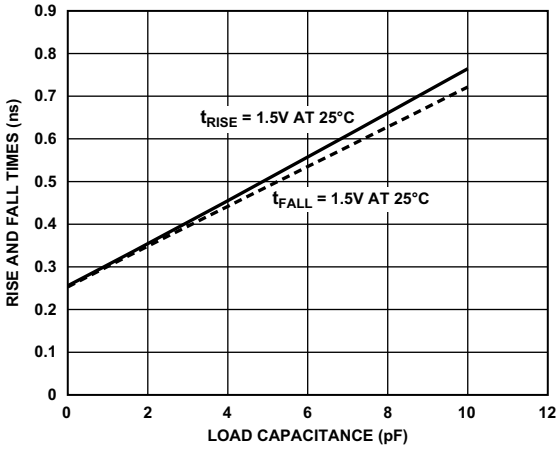


Figure 97. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.5 V) for DDR3

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured at top center of package.
Ψ_{JT} = from Table 104 and Table 105.
P_D = power dissipation (see the Total Internal Power Dissipation section for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 104 and Table 105, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 6-layer PCB with 101.6 mm × 152.4 mm dimensions.

Table 104. Thermal Characteristics for 349 CSP_BGA

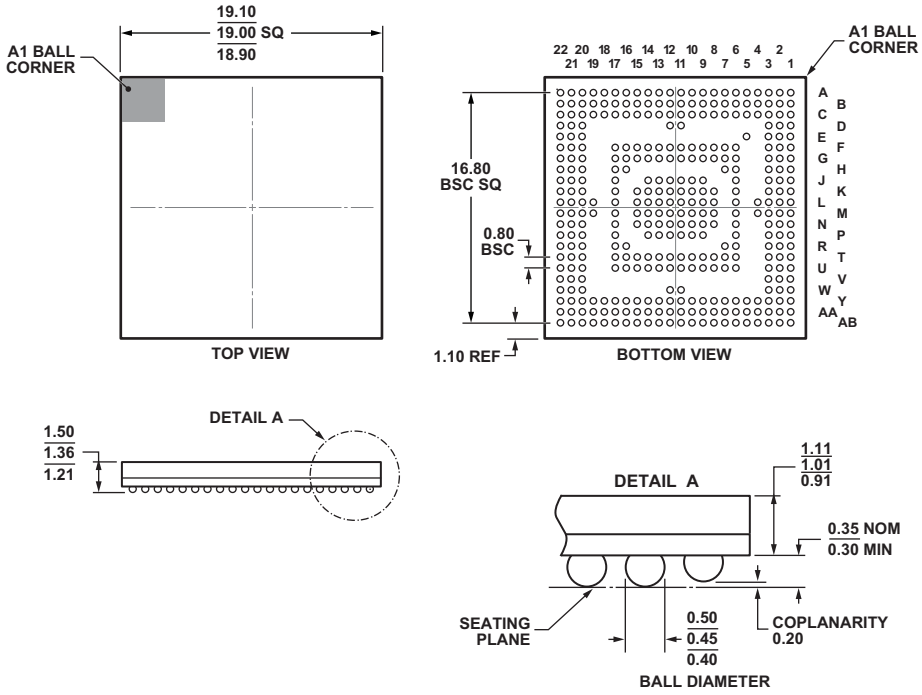
Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.3	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.65	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.12	°C/W
Ψ_{JT}	2 linear m/s air flow	0.14	°C/W

Table 105. Thermal Characteristics for 529 CSP_BGA

Parameter	Conditions	Typ	Unit
θ_{JA}	0 linear m/s air flow	13.4	°C/W
θ_{JA}	1 linear m/s air flow	12.1	°C/W
θ_{JA}	2 linear m/s air flow	11.6	°C/W
θ_{JC}		3.63	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.11	°C/W
Ψ_{JT}	2 linear m/s air flow	0.13	°C/W

OUTLINE DIMENSIONS

Dimensions for the 19 mm × 19 mm 349-ball CSP_BGA package in Figure 100 are shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MO-275-PPAB-2.

Figure 100. 349-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-349-1)
Dimensions shown in millimeters