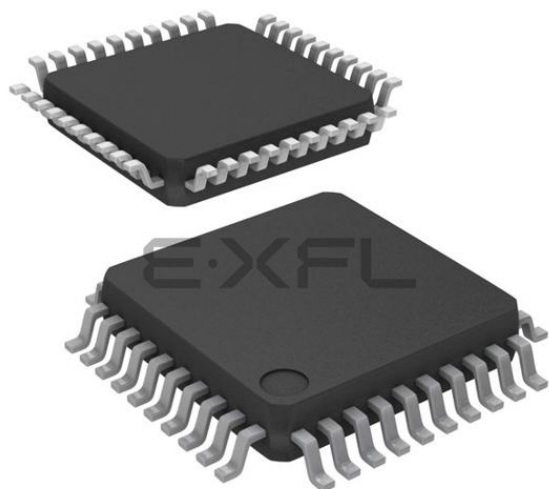




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21264jfp-u0

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/26 Group and Table 1.2 outlines the Functions and Specifications for R8C/27 Group.

Table 1.1 Functions and Specifications for R8C/26 Group

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) (other than K version) 62.5 ns ($f(XIN) = 16$ MHz, $VCC = 3.0$ to 5.5 V) (K version) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/26 Group
Peripheral Functions	Ports	I/O ports: 25 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits $\times$ 1 channel Timer RB: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits $\times$ 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Start-on-reset selectable
	Interrupts	Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation-stopped detector	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) (other than K version) $VCC = 3.0$ to 5.5 V ($f(XIN) = 16$ MHz) (K version) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz) $VCC = 2.2$ to 5.5 V ($f(XIN) = 5$ MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 μ A ($VCC = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾
Package		32-pin molded-plastic LQFP

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

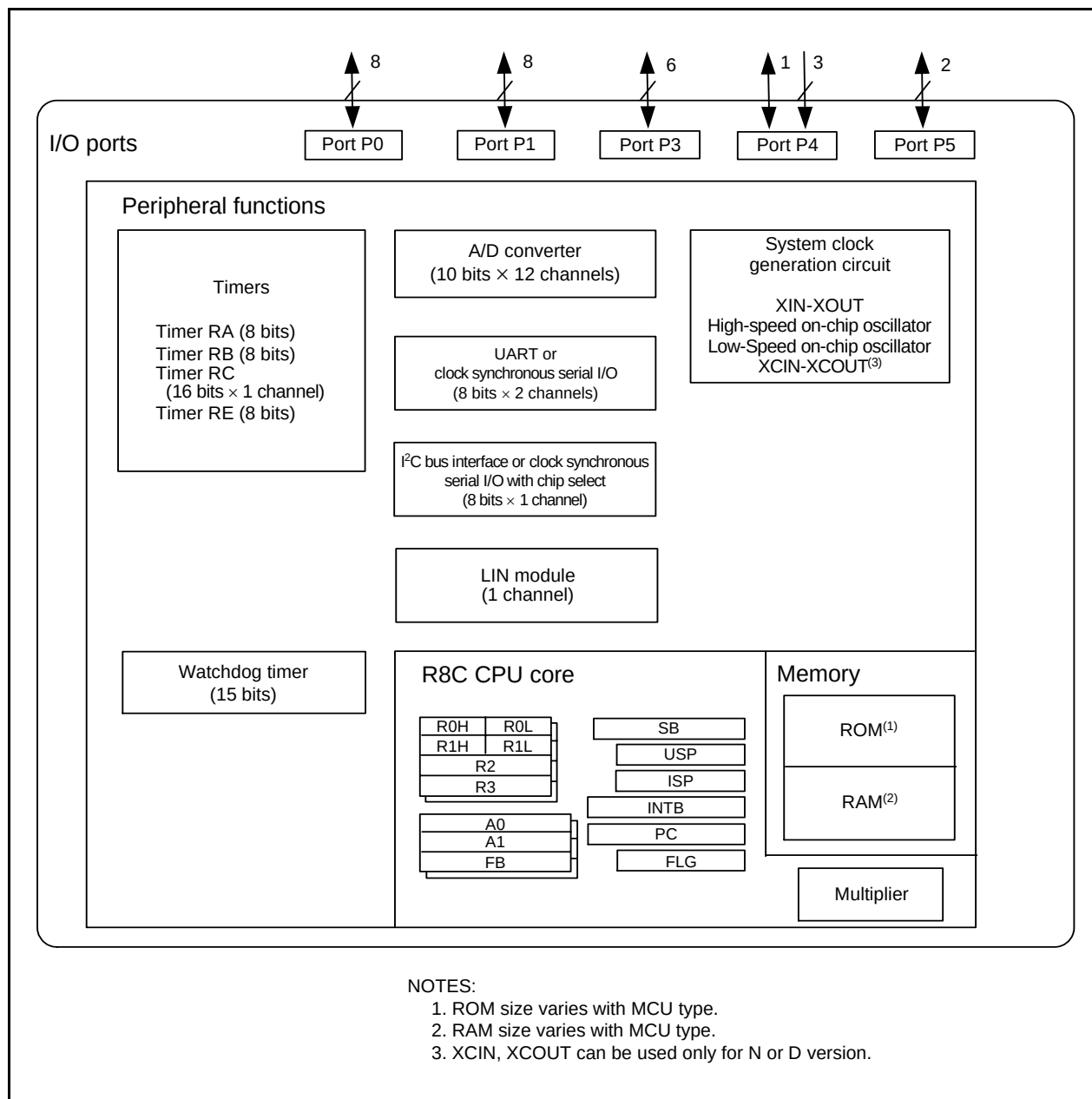


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/26 Group and Table 1.4 lists the Product Information for R8C/27 Group.

Table 1.3 Product Information for R8C/26 Group

Current of Sep. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F21262SNFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version		
R5F21264SNFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SNXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version	Factory programming product ⁽¹⁾	
R5F21264SNXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			

NOTE:

1. The user ROM is programmed before shipment.

Table 1.4 Product Information for R8C/27 Group

Current of Sep. 2008

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21272SNFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version	
R5F21274SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A		
R5F21275SNFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21276SNFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21272SDFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version	
R5F21274SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A		
R5F21275SDFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21276SDFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21274JFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	J version	
R5F21276JFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21274KFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	K version	
R5F21276KFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21272SNXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version	Factory programming product ⁽¹⁾
R5F21274SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A		
R5F21275SNXXXFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21276SNXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21272SDXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version	
R5F21274SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A		
R5F21275SDXXXFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21276SDXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21274JXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	J version	
R5F21276JXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		
R5F21274KXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	K version	
R5F21276KXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A		

NOTE:

1. The user ROM is programmed before shipment.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

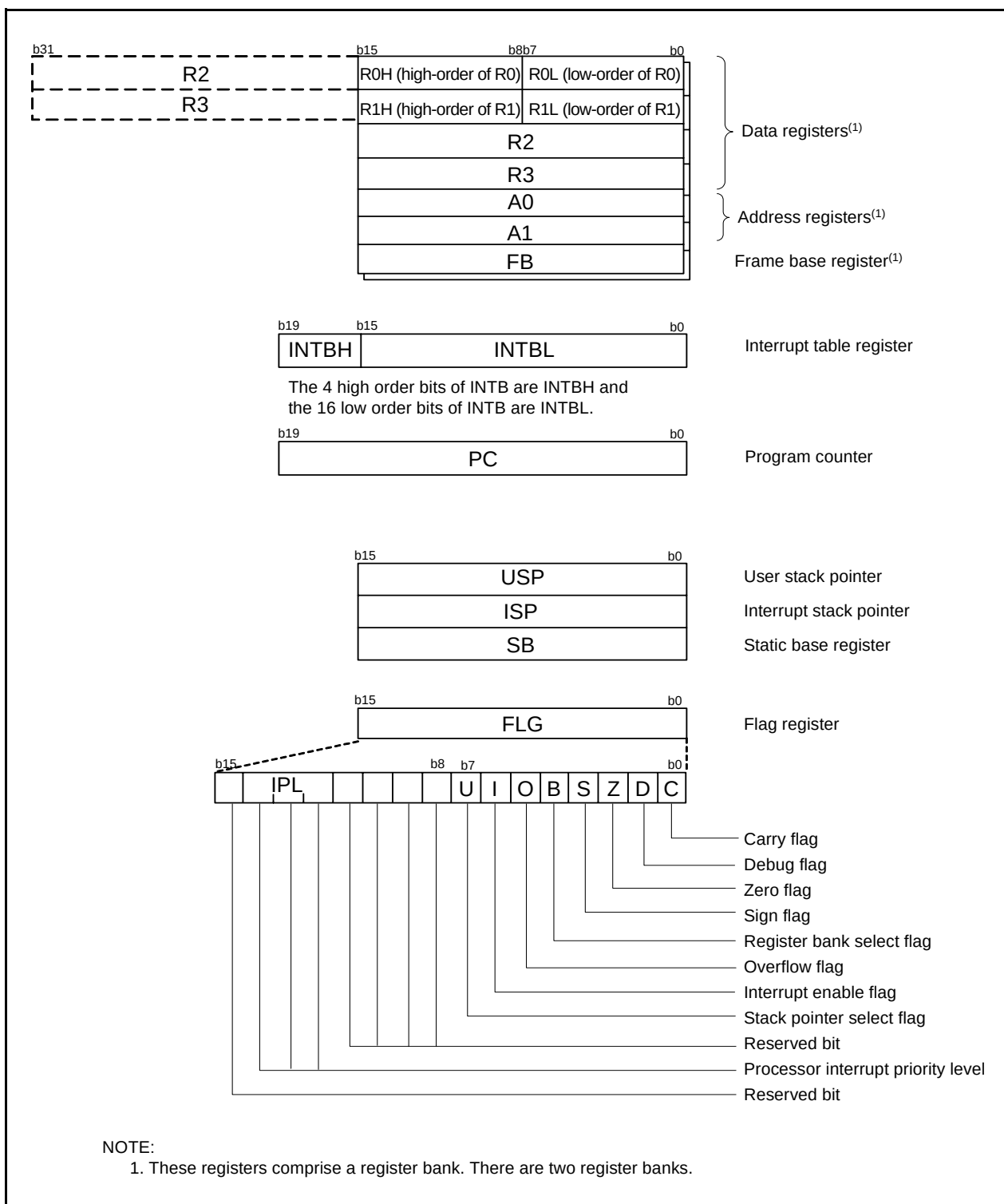


Figure 2.1 CPU Registers

3. Memory

3.1 R8C/26 Group

Figure 3.1 is a Memory Map of R8C/26 Group. The R8C/26 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

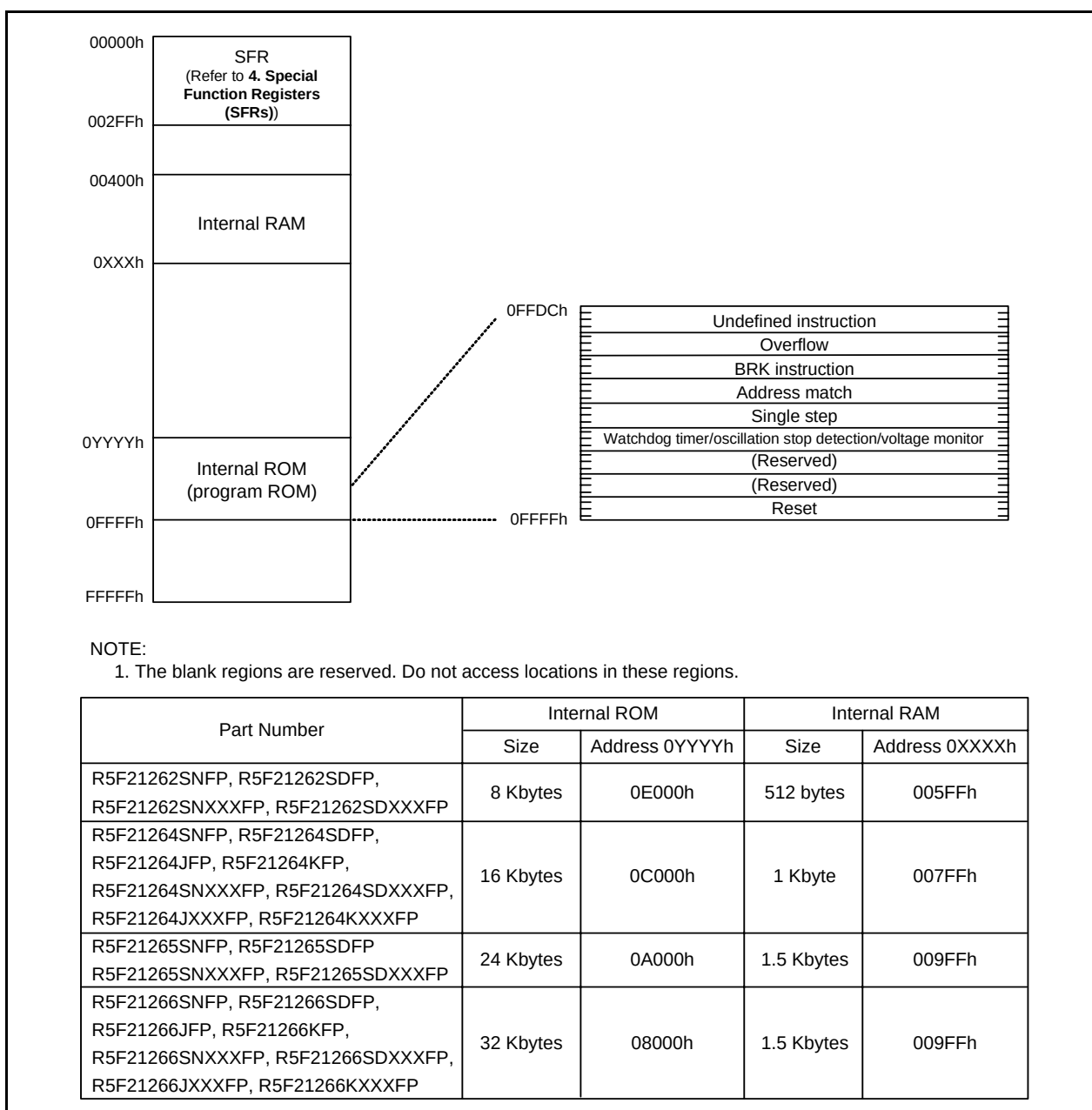


Figure 3.1 Memory Map of R8C/26 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽²⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4 ⁽³⁾	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6 ⁽³⁾	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7 ⁽³⁾	FRA7	When shipping
002Dh			
002Eh			
002Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register ⁽²⁾	TREHR	00h
011Bh	Timer RE Day of Week Data Register ⁽²⁾	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bits
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency	Without sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	0.25	—	10	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	1	—	10	MHz
		Without sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	0.25	—	5	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	1	—	5	MHz

NOTES:

1. $AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

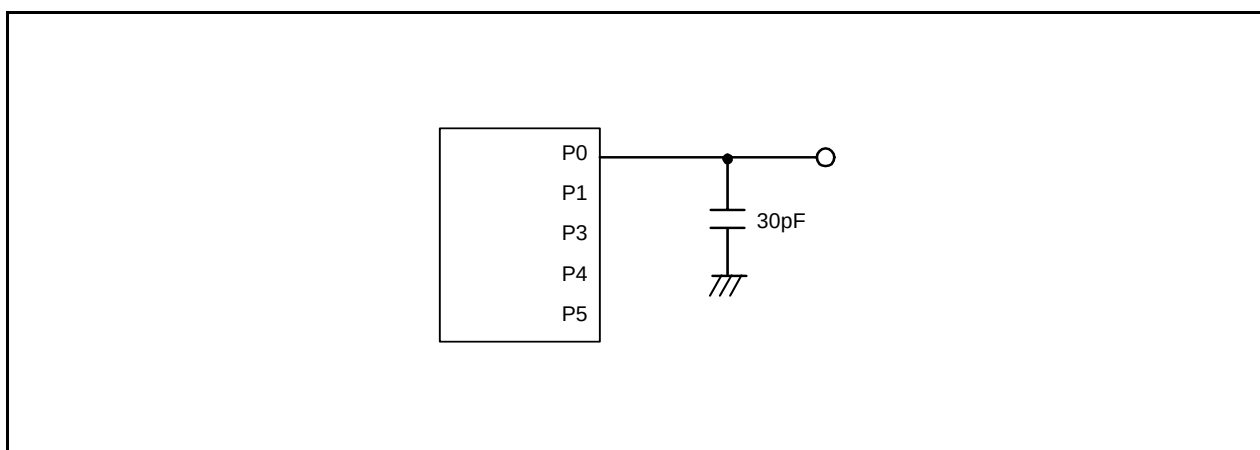
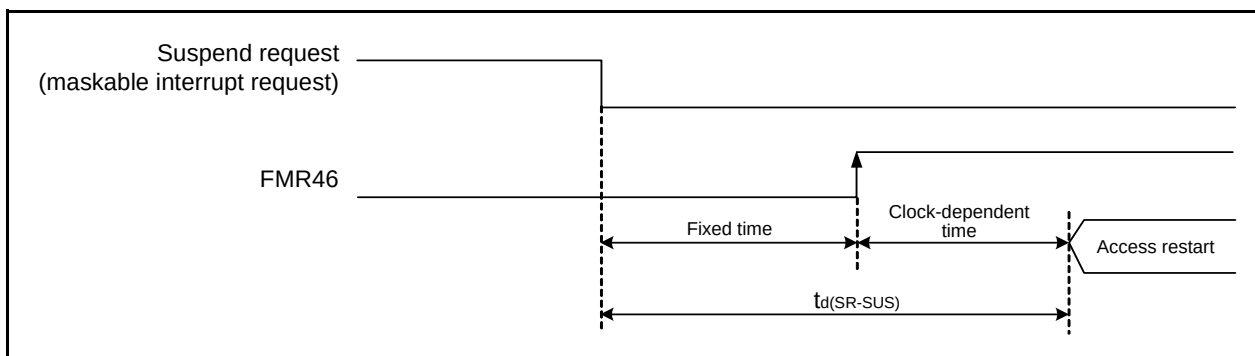
**Figure 5.1 Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	50	400	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	65	—	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	9	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	97 + CPU clock × 6 cycles	μs
—	Interval from erase start/restart until following suspend request		650	—	—	μs
—	Interval from program start/restart until following suspend request		0	—	—	ns
—	Time from suspend until program/erase restart		—	—	3 + CPU clock × 4 cycles	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.2	—	5.5	V
—	Program, erase temperature		-20 ⁽⁸⁾	—	85	°C
—	Data hold time ⁽⁹⁾	Ambient temperature = 55°C	20	—	—	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 5.2 Time delay until Suspend****Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	0.9	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	300	μs
V _{ccmin}	MCU operating voltage minimum value		2.2	—	—	V

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
tsa	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

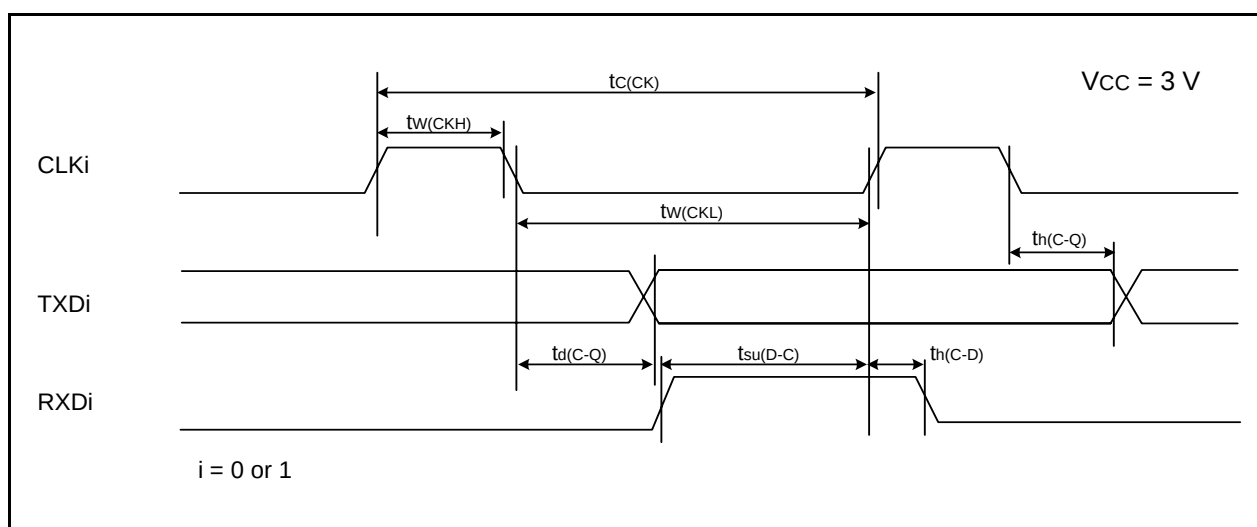
Table 5.17 Electrical Characteristics (3) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	μA

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.14 Serial Interface Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

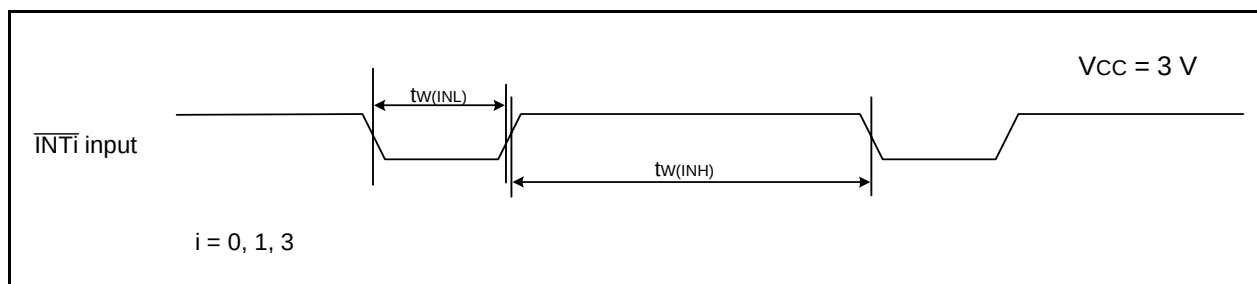
**Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.36 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bits
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.7	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency	Without sample and hold		0.25	—	10	MHz
		With sample and hold		1	—	10	MHz

NOTES:

1. $AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -40$ to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

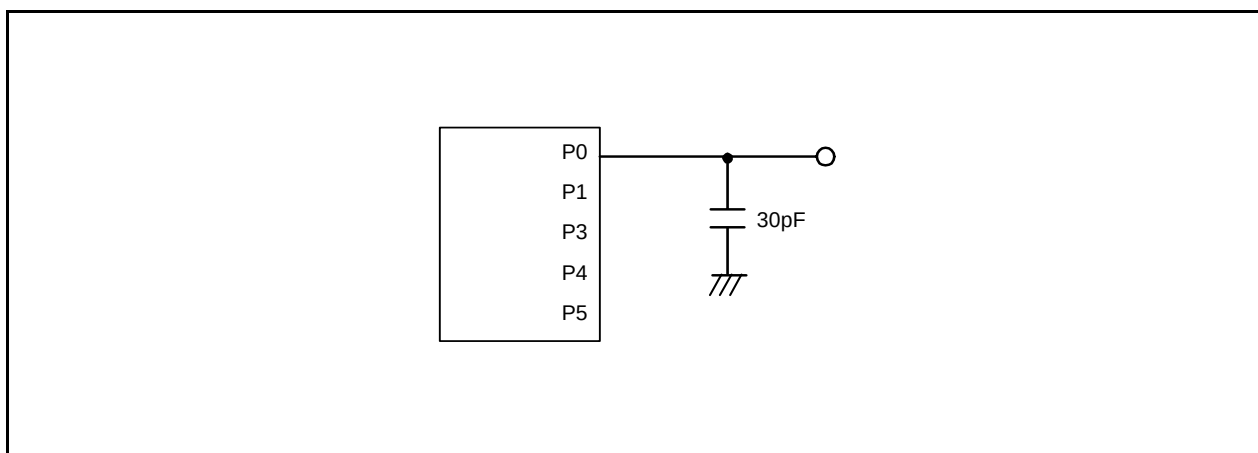
**Figure 5.20 Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

Table 5.47 Electrical Characteristics (1) [V_{CC} = 5 V]

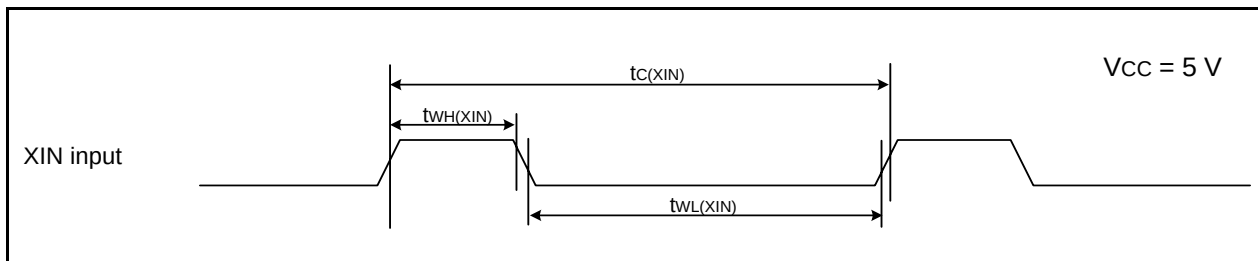
Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA	V _{CC} - 0.3	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μA	—	—	0.45	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}},$ KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO		0.1	0.5	—	V
		$\overline{\text{RESET}}$		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5V	—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5V	—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	XIN		—	1.0	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode	2.0	—	—	V

NOTE:

1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.49 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

**Figure 5.27 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

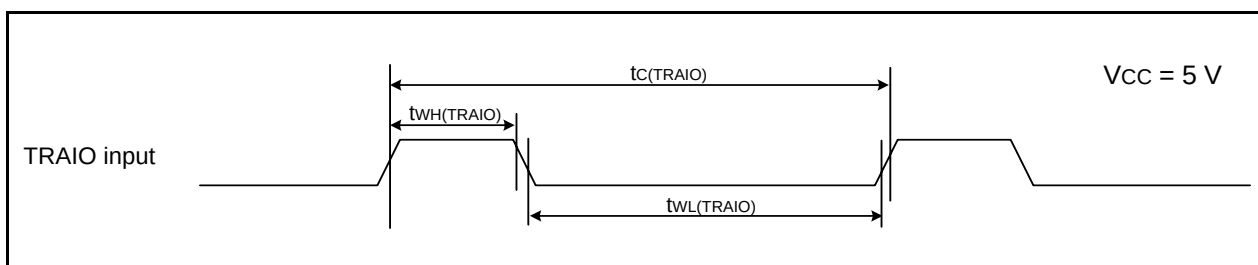
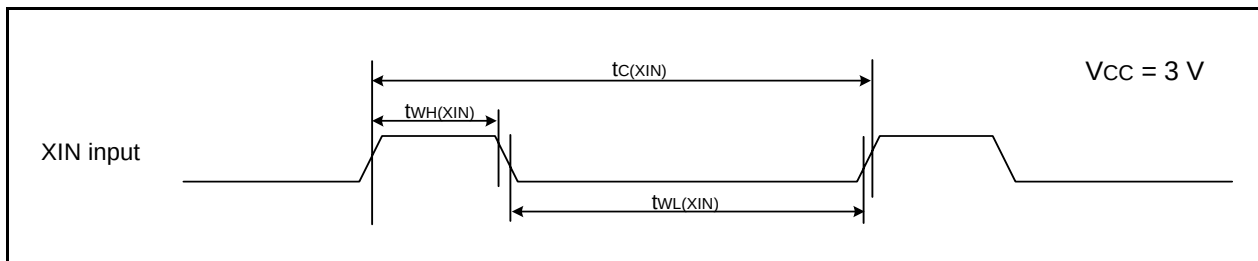
**Figure 5.28 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.54 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

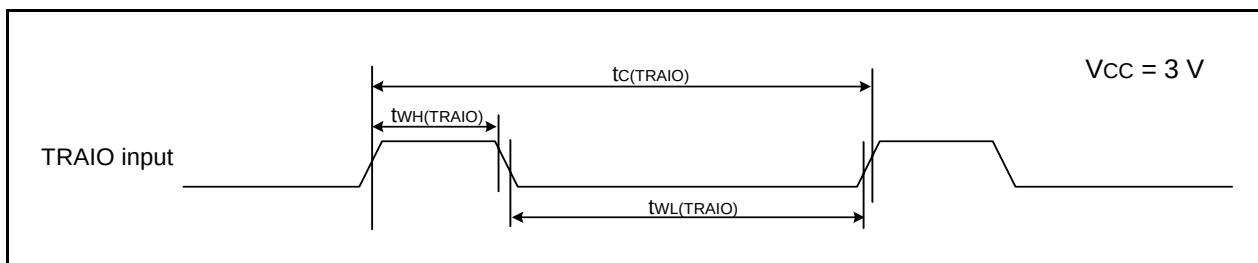
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	6	—	mA
		High-speed on-chip oscillator mode	—	2	—	mA
		High-speed on-chip oscillator mode	—	5	9	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Wait mode	—	25	70	μA
		Stop mode	—	0.7	3.0	μA
		Stop mode	—	1.1	—	μA
		Stop mode	—	3.8	—	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.55 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

**Figure 5.31 XIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.56 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

**Figure 5.32 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

