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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21266jfp-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 32-pin molded-plastic LQFP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/27 Group has on-chip data flash (1 KB $\times$ 2 blocks).

The difference between the R8C/26 Group and R8C/27 Group is only the presence or absence of data flash.

Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

1.4 Product Information

Table 1.3 lists the Product Information for R8C/26 Group and Table 1.4 lists the Product Information for R8C/27 Group.

Table 1.3 Product Information for R8C/26 Group

Current of Sep. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F21262SNFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version		
R5F21264SNFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SNXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version	Factory programming product ⁽¹⁾	
R5F21264SNXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			

NOTE:

1. The user ROM is programmed before shipment.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 (2)	VCA1	00001000b
0032h	Voltage Detection Register 2 (2)	VCA2	• N, D version 00h⁽³⁾ 00100000b⁽⁴⁾ • J, K version 00h⁽⁷⁾ 01000000b⁽⁸⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register (5)	VW1C	• N, D version 00001000b • J, K version 0000X000b⁽⁷⁾ 0100X001b⁽⁸⁾
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register (6)	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register ⁽⁹⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- The LVD00N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset or the LVD00N bit in the OFS register is set to 0, and hardware reset.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) These regions are reserved. Do not access locations in these regions.
- The LVD10N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 1 reset, or the LVD10N bit in the OFS register is set to 0 and hardware reset.
- Selected by the IICSEL bit in the PMR register.

Table 4.7 SFR Information (7)⁽¹⁾

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

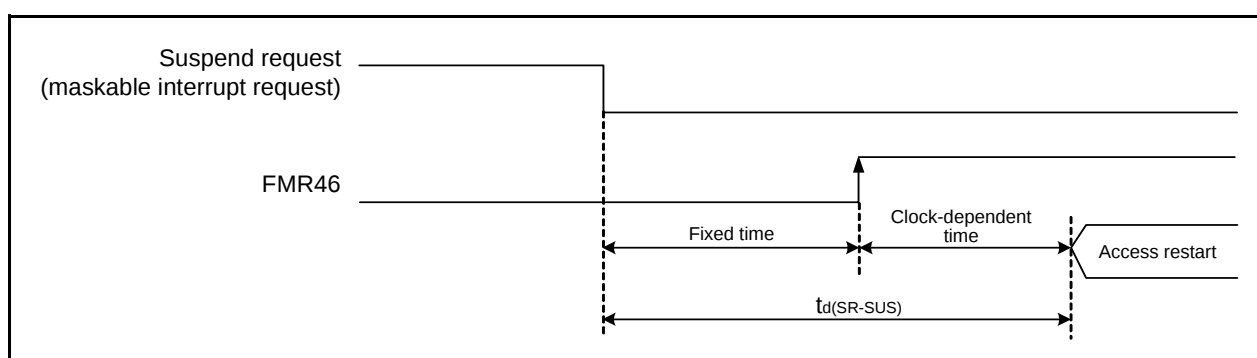


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	0.9	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	300	μs
Vccmin	MCU operating voltage minimum value		2.2	—	—	V

NOTES:

1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

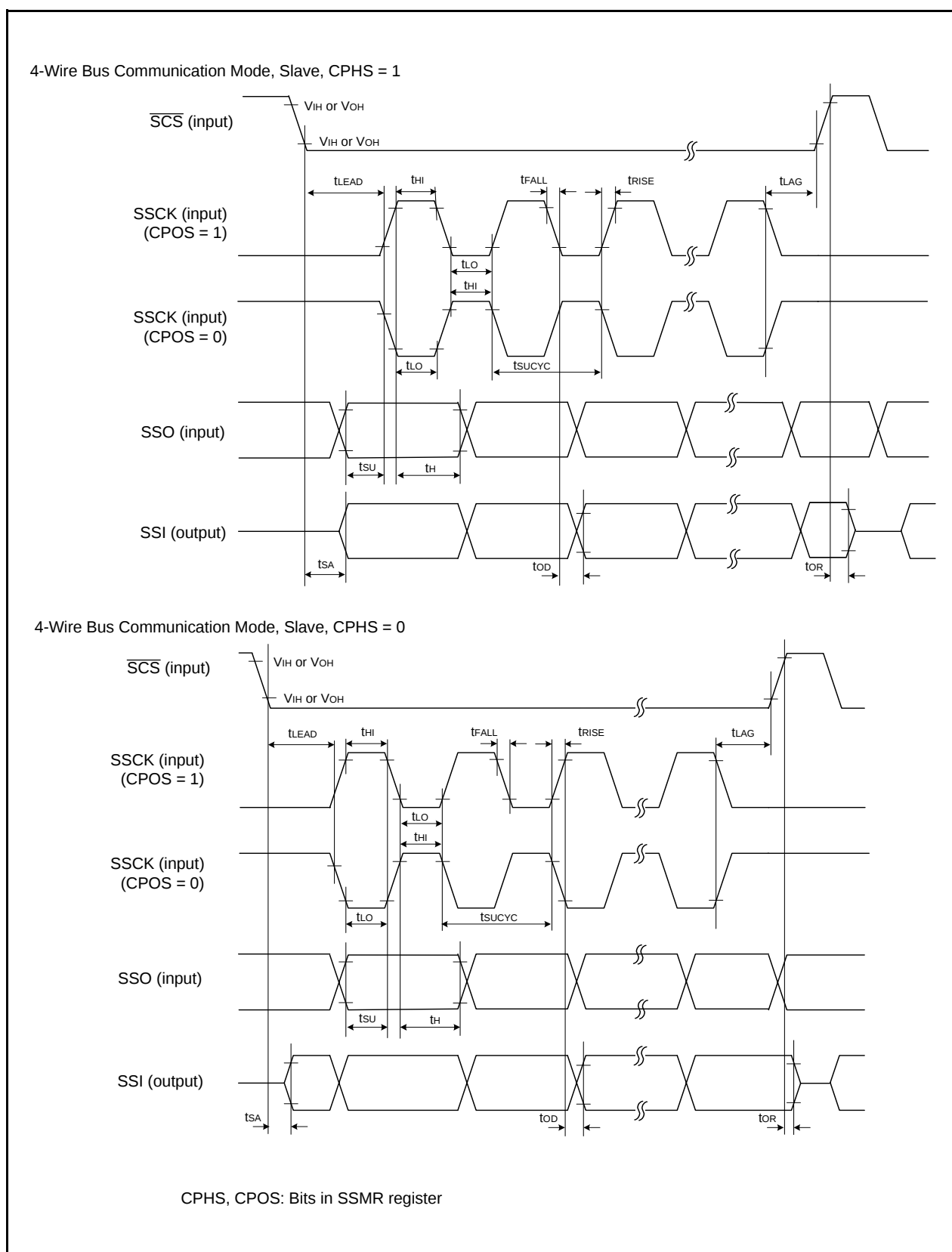
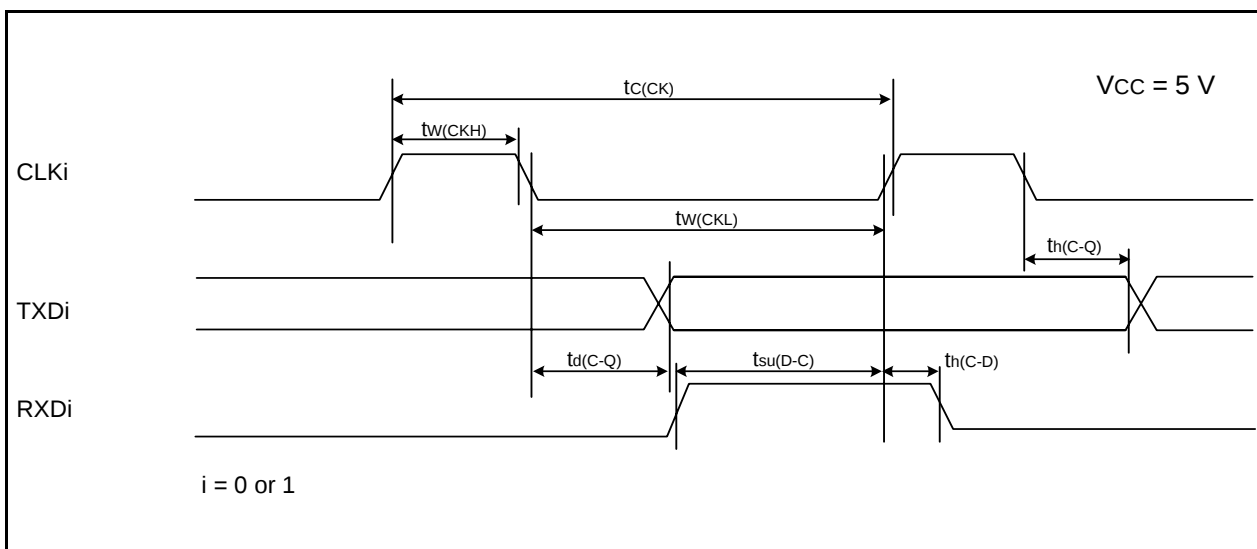


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ or } 1$ **Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt $\overline{INTi}$ ($i = 0, 1, 3$) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

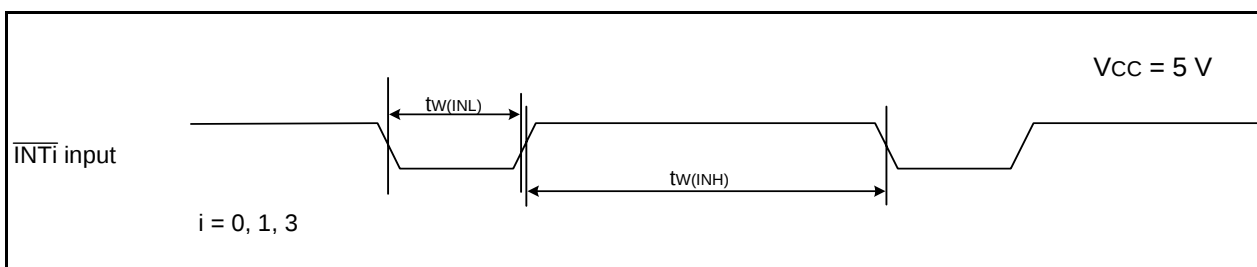
**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.22 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

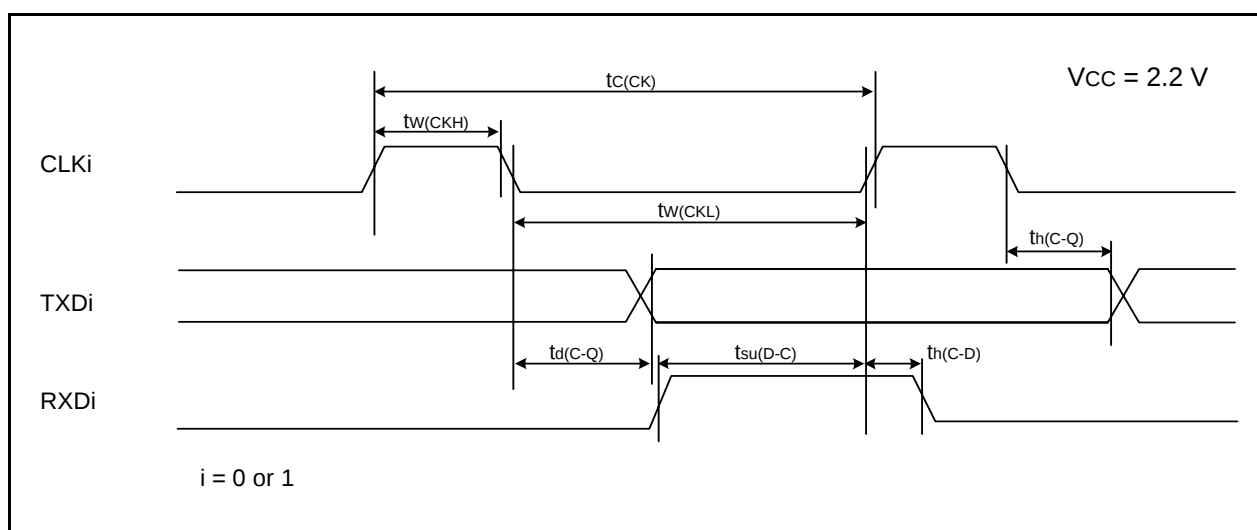
Table 5.23 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1			μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1			μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA
		Stop mode	XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

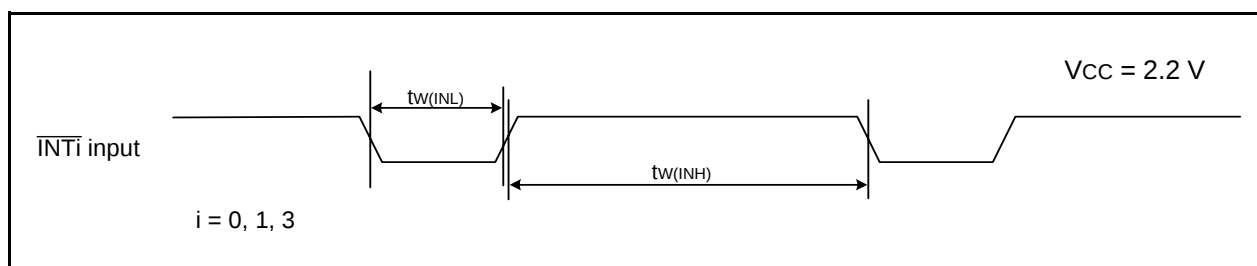
i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 2.2 V**

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} + 0.3	V
V _O	Output voltage		-0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	-40 °C ≤ T _{opr} ≤ 85 °C	300	mW
		85 °C ≤ T _{opr} ≤ 125 °C	125	mW
T _{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.35 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage			2.7	—	5.5	V
V _{SS} /AV _{SS}	Supply voltage			—	0	—	V
V _{IH}	Input "H" voltage			0.8 V _{CC}	—	V _{CC}	V
V _{IL}	Input "L" voltage			0	—	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output "H" current	Sum of all pins I _{OH} (peak)		—	—	-60	mA
I _{OH} (peak)	Peak output "H" current			—	—	-10	mA
I _{OH} (avg)	Average output "H" current			—	—	-5	mA
I _{OL} (sum)	Peak sum output "L" currents	Sum of all pins I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	Peak output "L" currents			—	—	10	mA
I _{OL} (avg)	Average output "L" current			—	—	5	mA
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
—	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	—	125	—	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	—	—	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected	—	—	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.45 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time			–	–	1.5tcyc + 100	ns
t _{OR}	SSI slave out open time			–	–	1.5tcyc + 100	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

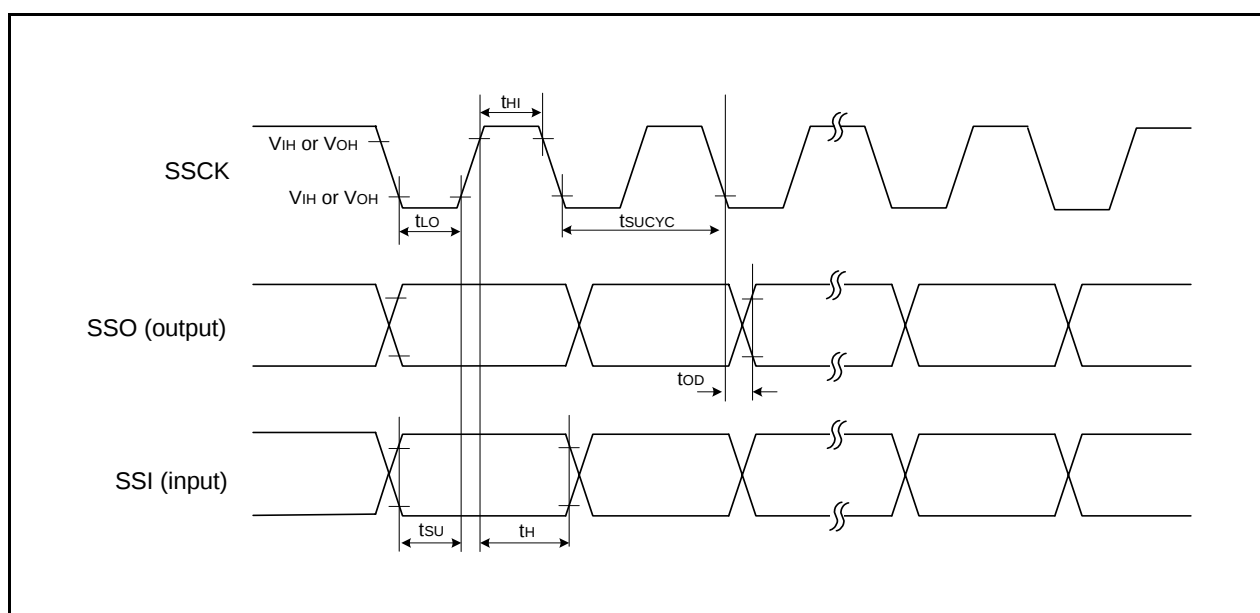


Figure 5.25 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.46 Timing Requirements of I²C bus Interface⁽¹⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cy} c + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cy} c + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cy} c + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cy} c ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cy} c ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cy} c ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cy} c ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cy} c ⁽²⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cy} c + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{cy}c = 1/f₁(s)

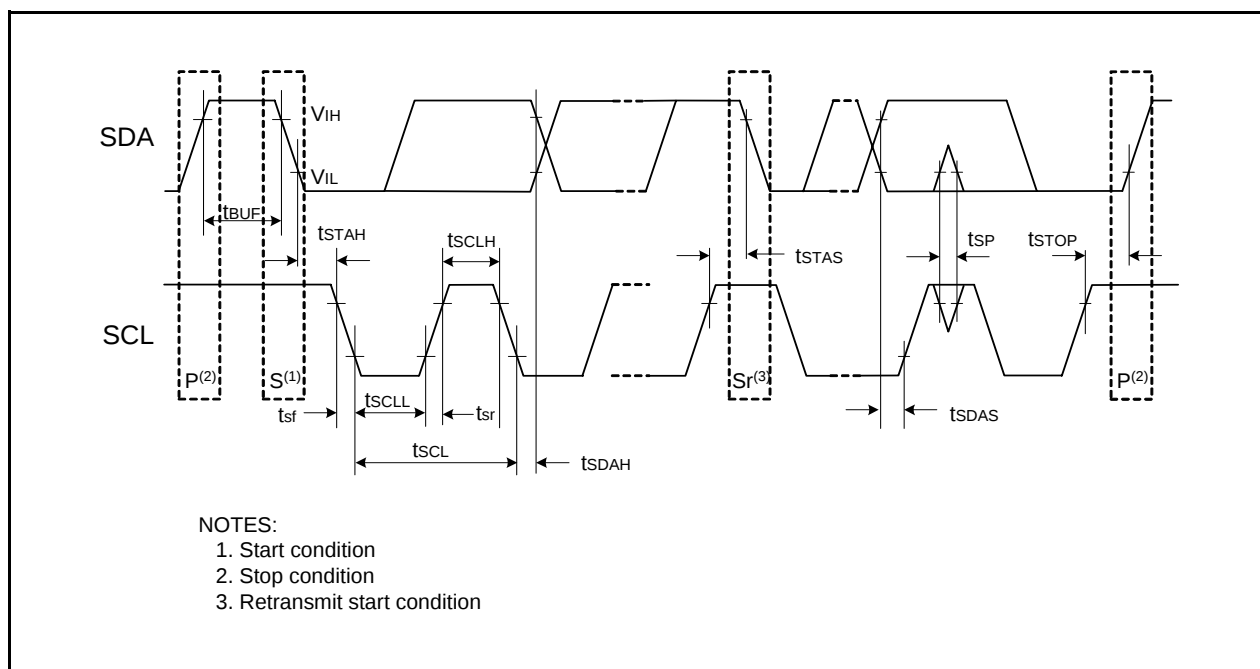
**Figure 5.26 I/O Timing of I²C bus Interface**

Table 5.47 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μ A	V _{CC} - 0.3	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μ A	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μ A	—	—	0.45	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μ A	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, $\overline{\text{TRAIO}}$, $\overline{\text{RXD0}}$, $\overline{\text{RXD1}}$, $\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{SSI}}$, $\overline{\text{SCL}}$, $\overline{\text{SDA}}$, $\overline{\text{SSO}}$		0.1	0.5	—	V
		$\overline{\text{RESET}}$		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5V	—	—	5.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5V	—	—	-5.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5V	30	50	167	k Ω
R _{fXIN}	Feedback resistance	XIN		—	1.0	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode	2.0	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

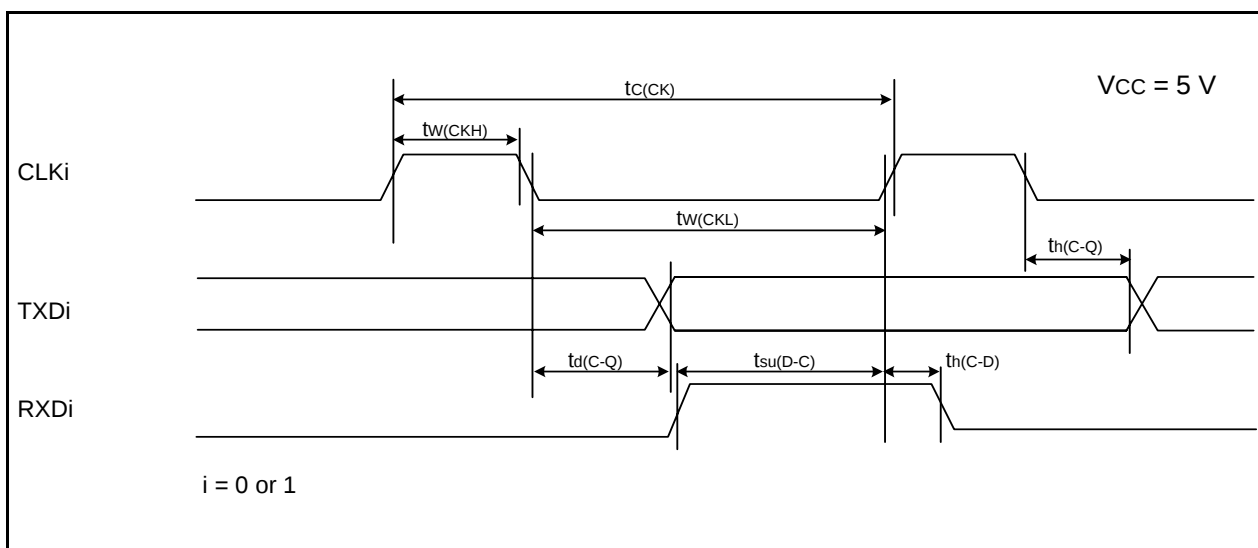
Table 5.48 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	μA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	4.0	–	μA

Table 5.51 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.29 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.52 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

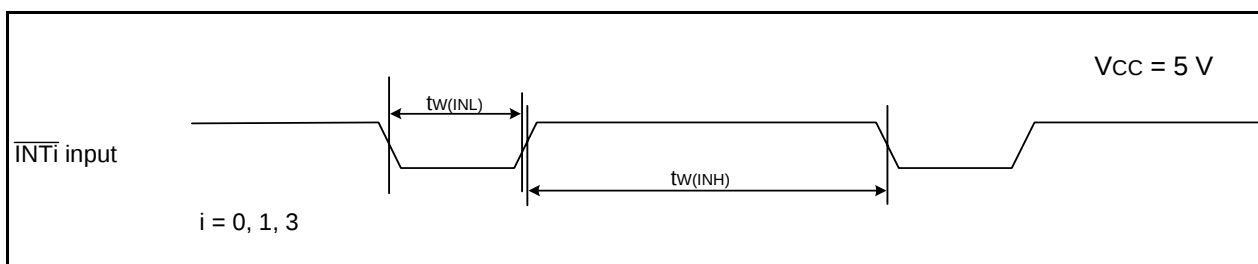
**Figure 5.30 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.53 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	–	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	–	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	–	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	–	–	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		RESET			0.1	0.4	–	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3V		–	–	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3V		–	–	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V _{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:

1. V_{CC} = 2.7 to 3.3 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.54 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	6	—	mA
		High-speed on-chip oscillator mode	—	2	—	mA
		High-speed on-chip oscillator mode	—	5	9	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Wait mode	—	25	70	μA
		Stop mode	—	0.7	3.0	μA
		Stop mode	—	1.1	—	μA
		Stop mode	—	3.8	—	μA

REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	May 25, 2007	16	Figure 3.2 part number revised
		30	Table 5.10 revised
		53	Table 5.39 NOTE4 added
		55	Table 5.42 revised
1.40a	Jun 14, 2007	5, 7	Table 1.3 and Table 1.4 revised
2.00	Mar 01, 2008	1, 49	1.1, 5.2 "J and K versions are ..." deleted
		5, 7	Table 1.3, Table 1.4 revised
		11	Table 1.6 NOTE3 added
		15, 16	Figure 3.1, Figure 3.2; "Expanded area" deleted
		17	Table 4.1 "002Ch" added
		18	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"
		24, 49	Table 5.2, Table 5.35; NOTE2 revised
2.10	Sep 26, 2008	30	Table 5.10 revised, NOTE4 added
		–	"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E
		26, 51	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		27, 52	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		53	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added
			Table 5.40 revised
		54	Table 5.41 revised
			Figure 5.22 revised

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