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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21272syfp-x6

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

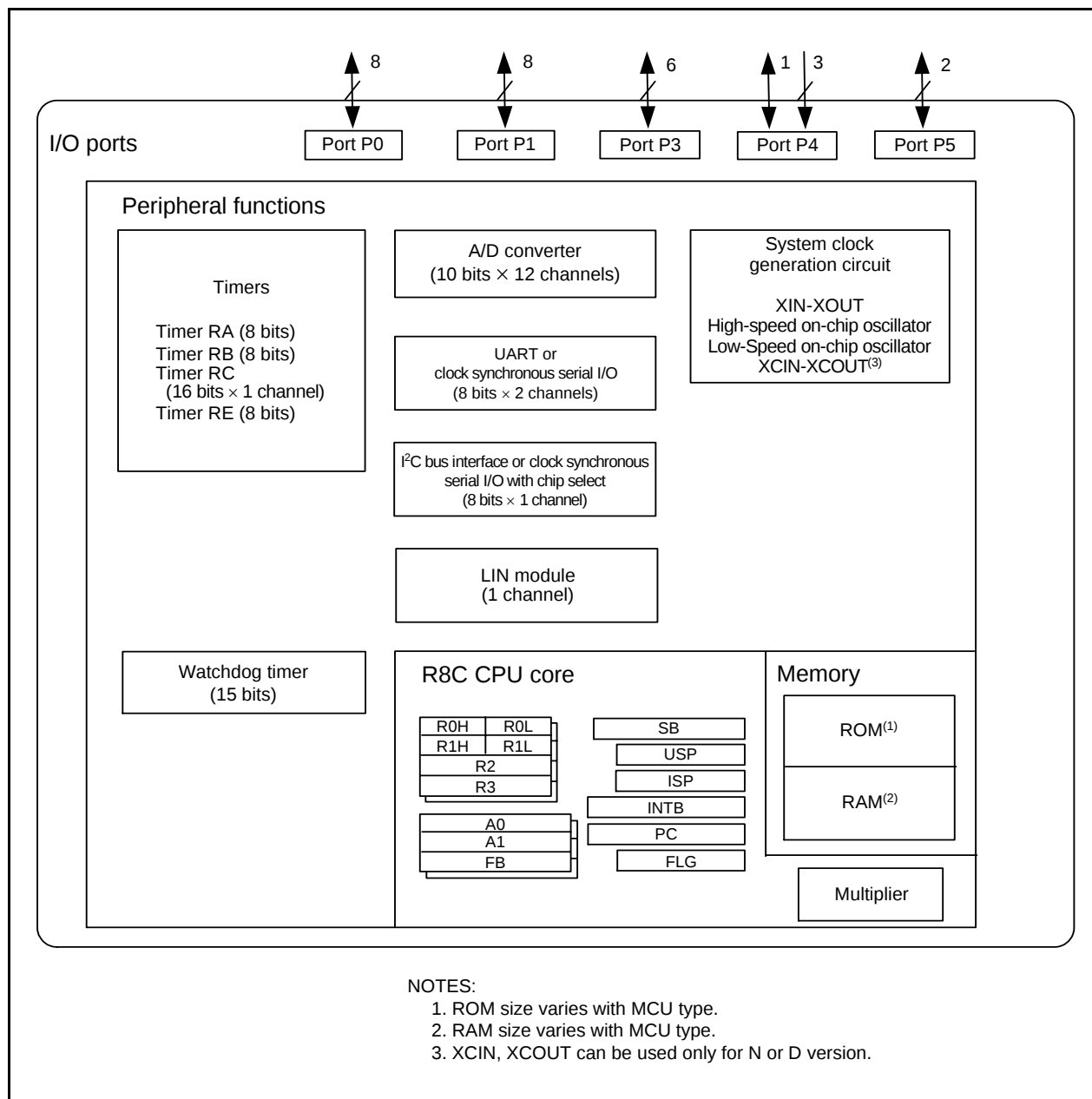


Figure 1.1 Block Diagram

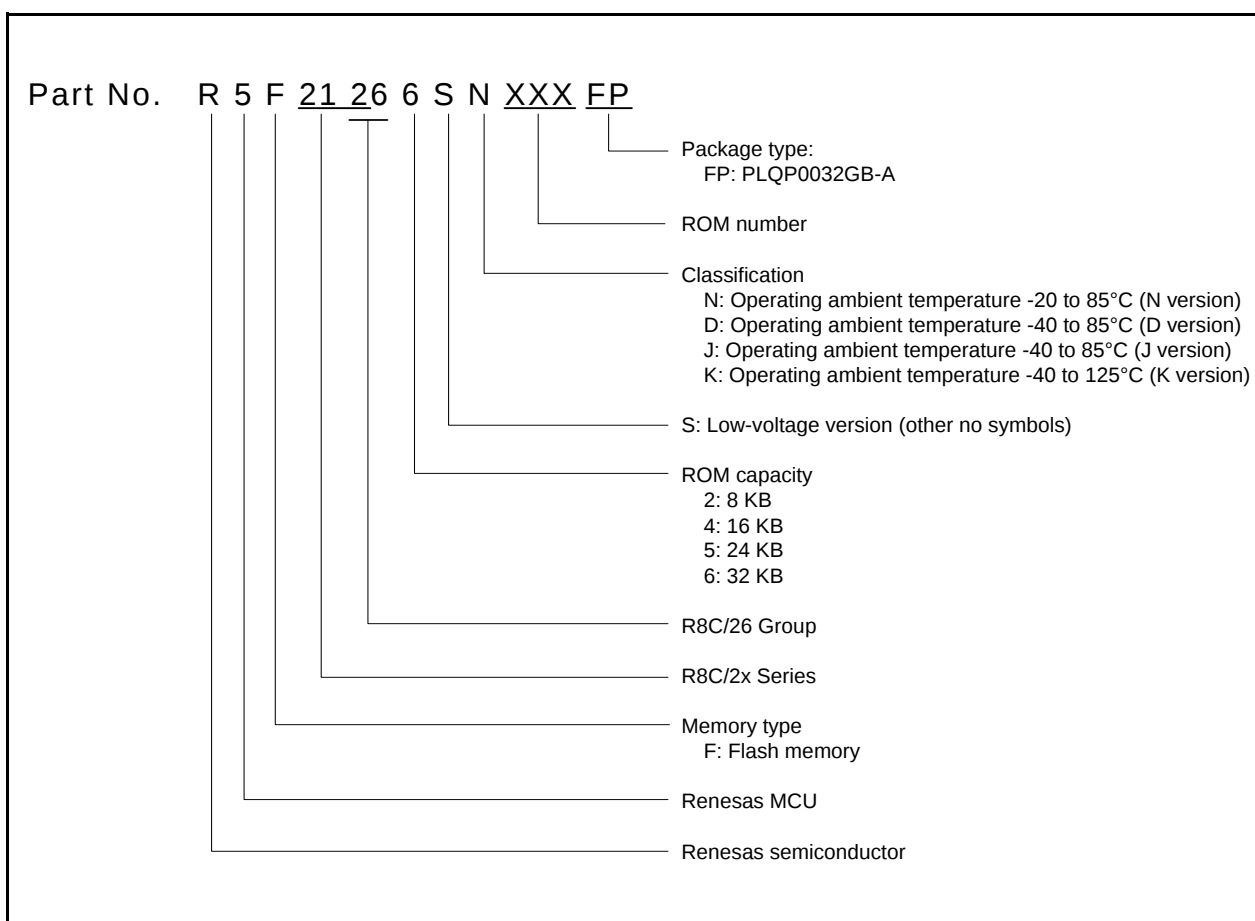


Figure 1.2 Part Number, Memory Size, and Package of R8C/26 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

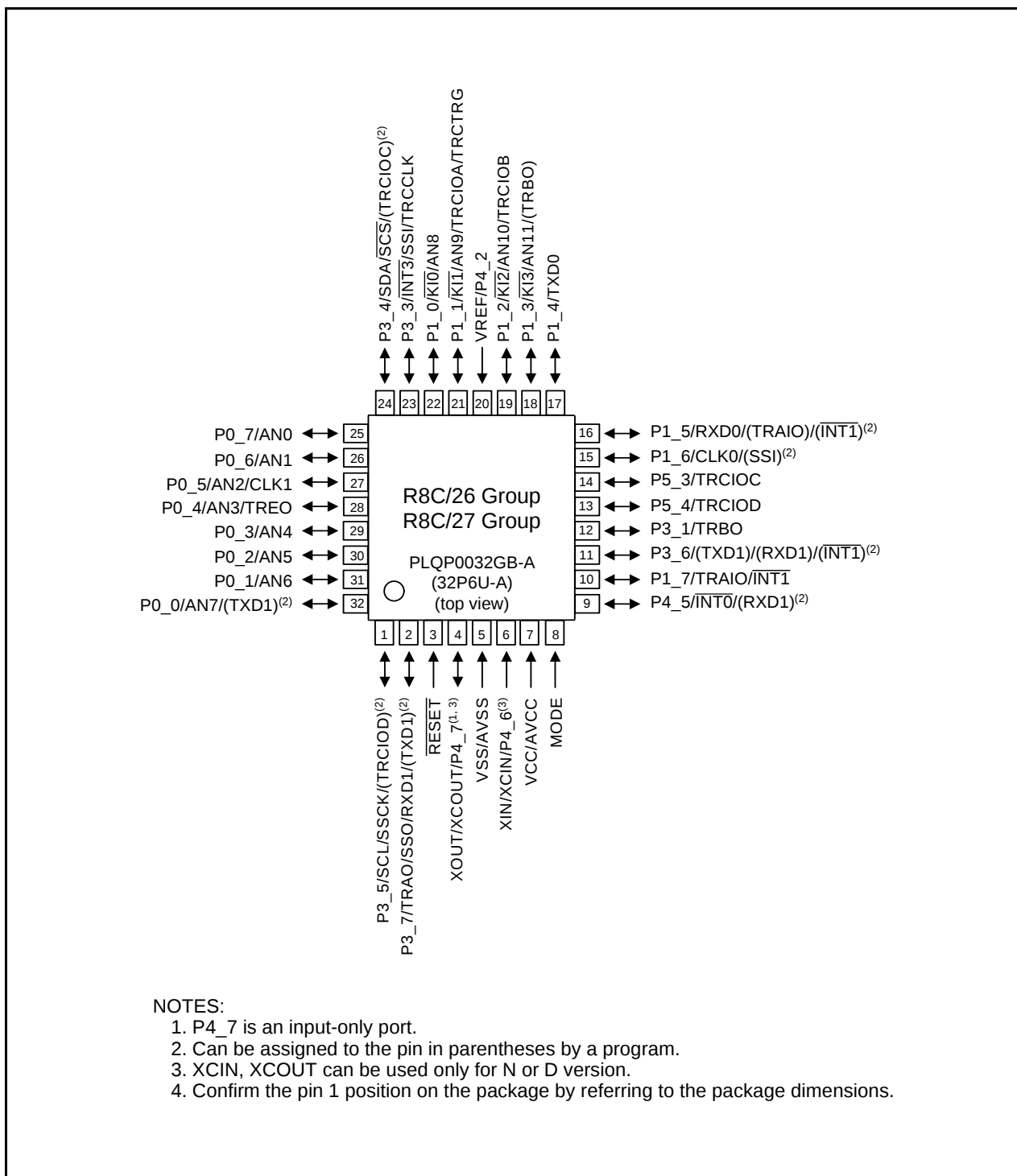


Figure 1.4 Pin Assignments (Top View)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

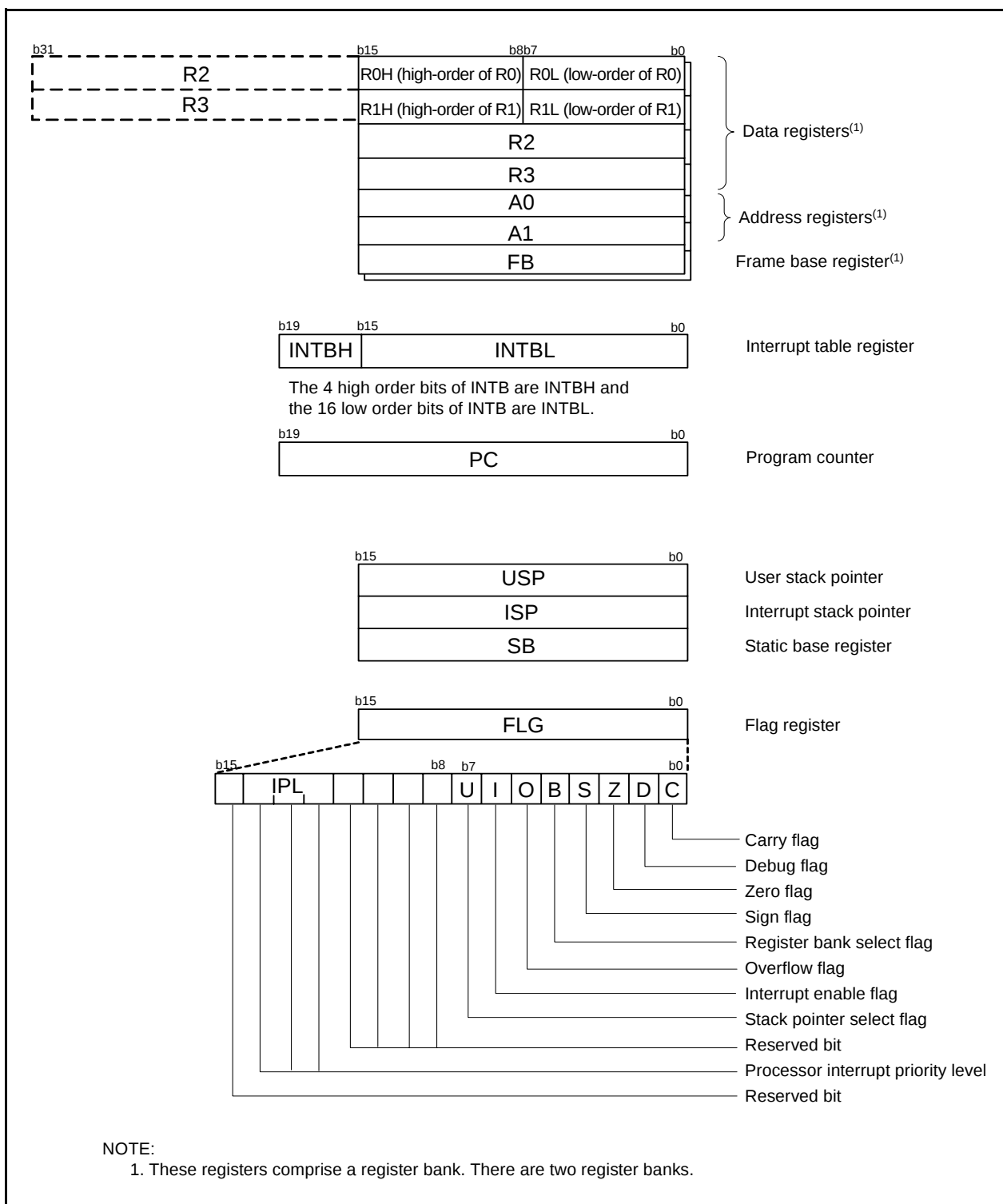


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽²⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4 ⁽³⁾	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6 ⁽³⁾	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7 ⁽³⁾	FRA7	When shipping
002Dh			
002Eh			
002Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 (2)	VCA1	00001000b
0032h	Voltage Detection Register 2 (2)	VCA2	• N, D version 00h(3) 00100000b(4) • J, K version 00h(7) 01000000b(8)
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register (5)	VW1C	• N, D version 00001000b • J, K version 0000X000b(7) 0100X001b(8)
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register (6)	VW0C	0000X000b(3) 0100X001b(4)
0039h			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register(9)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- The LVD00N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset or the LVD00N bit in the OFS register is set to 0, and hardware reset.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) These regions are reserved. Do not access locations in these regions.
- The LVD10N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 1 reset, or the LVD10N bit in the OFS register is set to 0 and hardware reset.
- Selected by the IICSEL bit in the PMR register.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
t _{rth}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

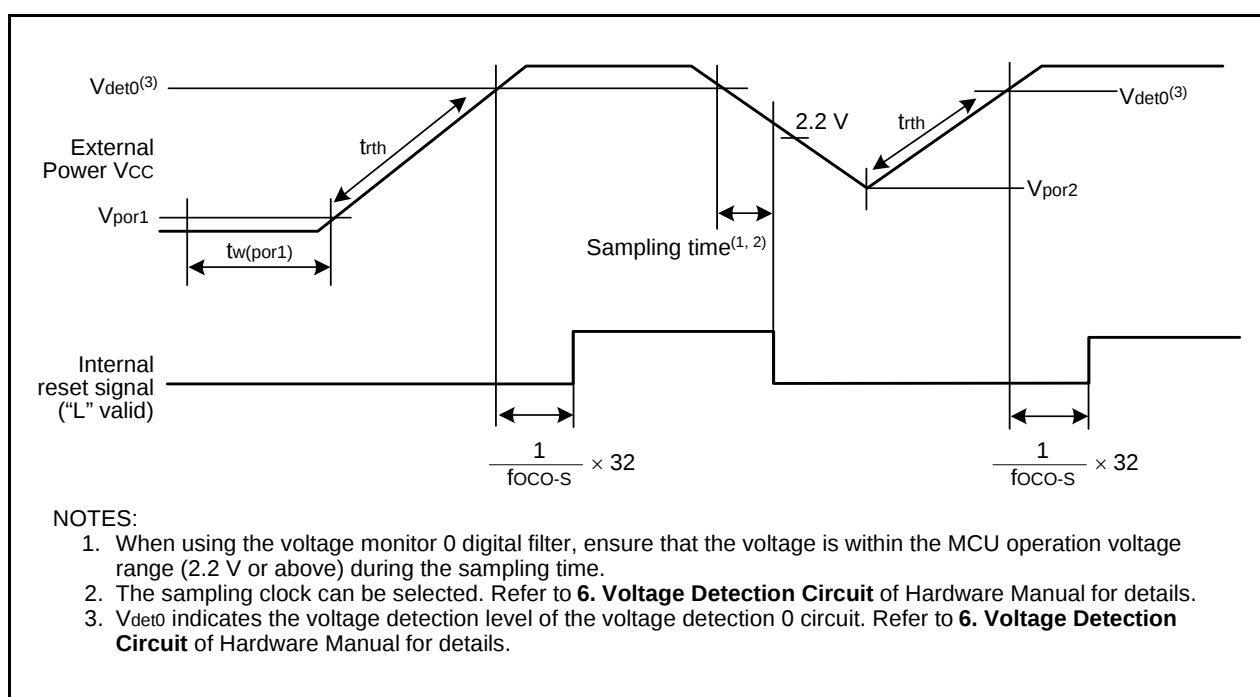
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.15 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I _{OH} = -5 mA		V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA		V _{CC} - 0.5	—	V _{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I _{OL} = 5 mA		—	—	2.0	V
			I _{OL} = 200 μA		—	—	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH	I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	—	V
		RESET			0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5 V		30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN			—	1.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.16 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	10	17	mA
		High-speed on-chip oscillator mode	—	10	15	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Low-speed clock mode	—	130	300	μA
		Low-speed clock mode	—	30	—	μA

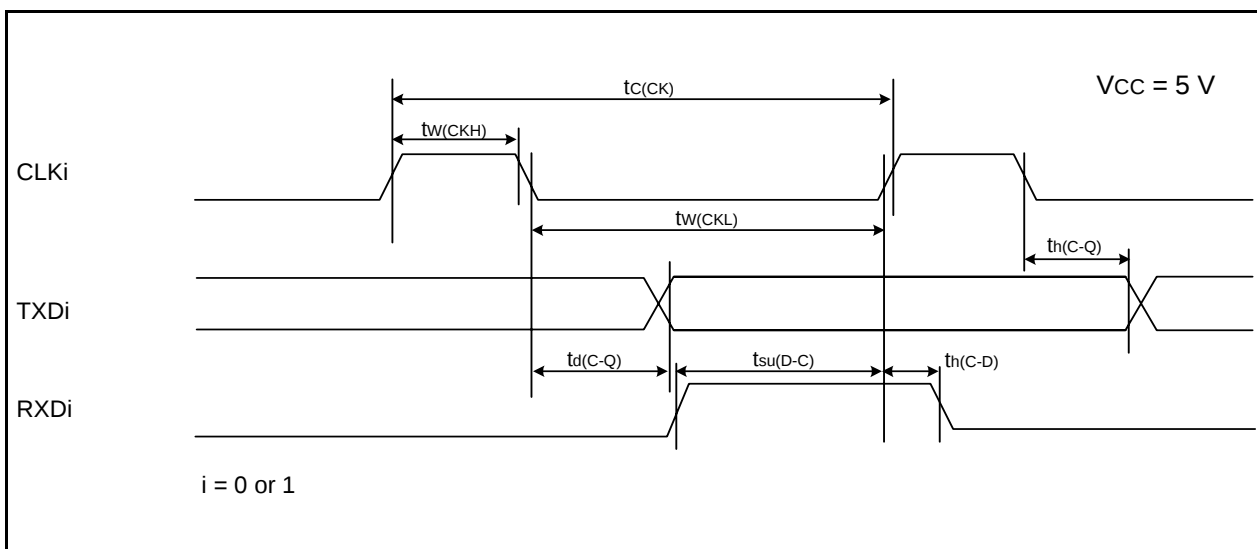
Table 5.17 Electrical Characteristics (3) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS}	Wait mode	—	25	75	μA
		Stop mode	—	0.8	3.0	μA

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

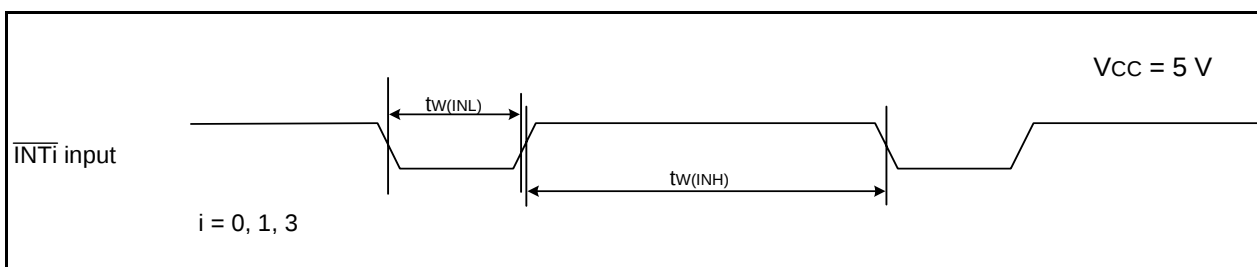
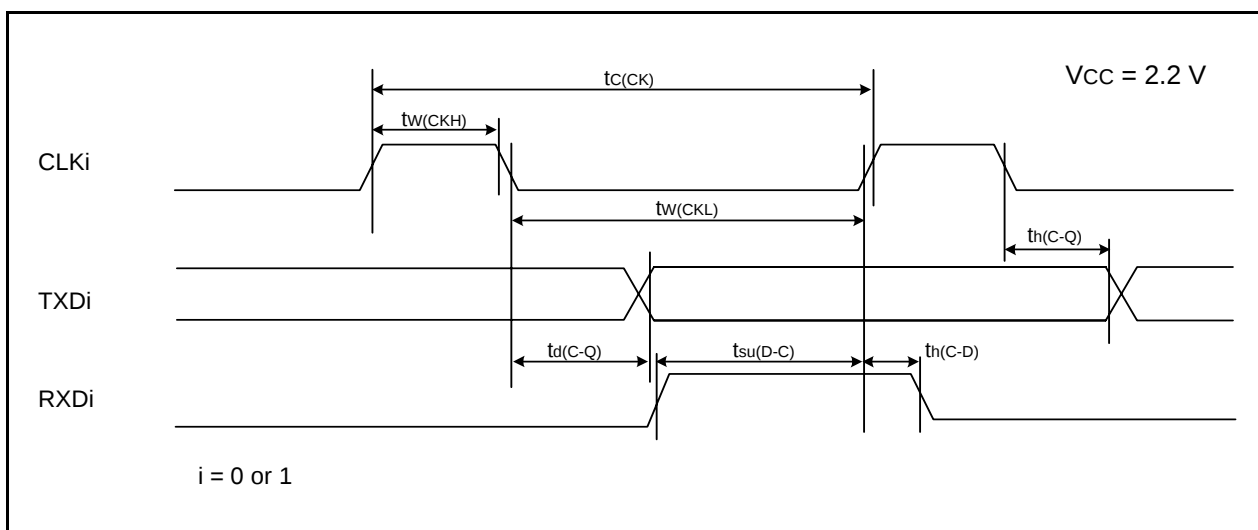
**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

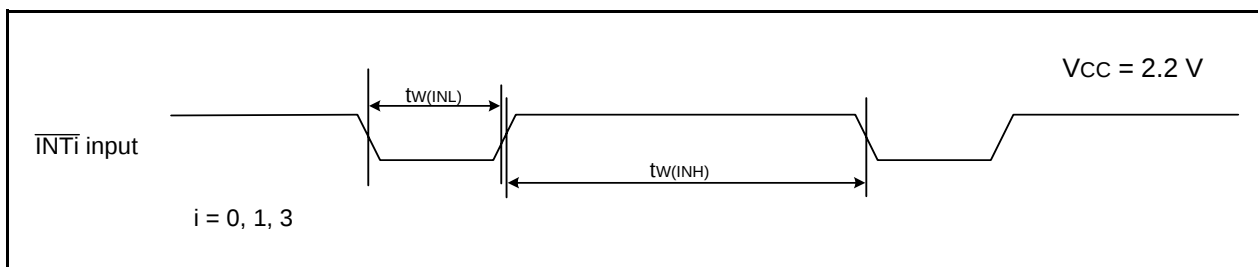
i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 2.2 V**

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} + 0.3	V
V _O	Output voltage		-0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	-40 °C ≤ T _{opr} ≤ 85 °C	300	mW
		85 °C ≤ T _{opr} ≤ 125 °C	125	mW
T _{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.35 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage			2.7	—	5.5	V
V _{SS} /AV _{SS}	Supply voltage			—	0	—	V
V _{IH}	Input "H" voltage			0.8 V _{CC}	—	V _{CC}	V
V _{IL}	Input "L" voltage			0	—	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output "H" current	Sum of all pins I _{OH} (peak)		—	—	-60	mA
I _{OH} (peak)	Peak output "H" current			—	—	-10	mA
I _{OH} (avg)	Average output "H" current			—	—	-5	mA
I _{OL} (sum)	Peak sum output "L" currents	Sum of all pins I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	Peak output "L" currents			—	—	10	mA
I _{OL} (avg)	Average output "L" current			—	—	5	mA
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
—	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	—	125	—	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	—	—	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected	—	—	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.42 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature · supply voltage dependence	V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾	38	40	42	MHz
		V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾	37.6	40	42.4	MHz
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	400	–	μA

NOTES:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

Table 5.43 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

Table 5.44 Power Supply Circuit Timing Characteristics

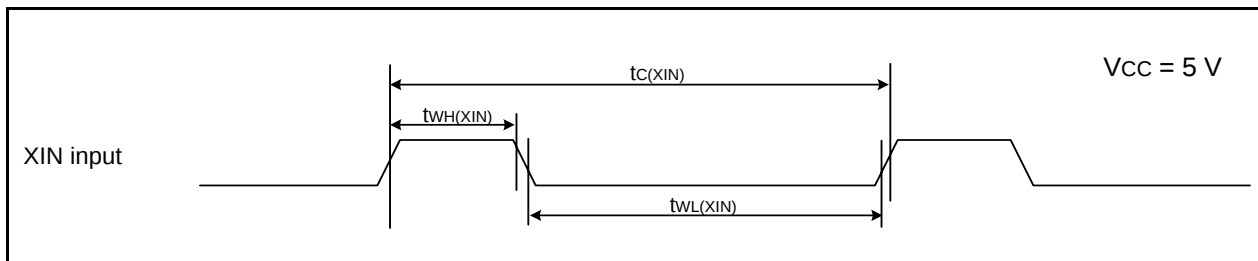
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.49 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

**Figure 5.27 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

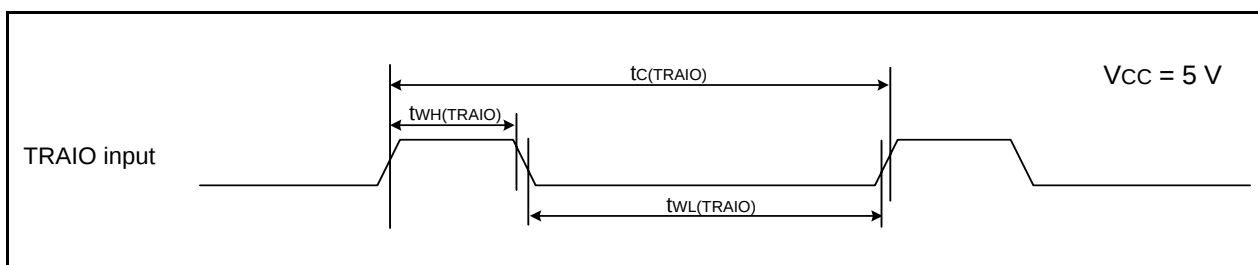
**Figure 5.28 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.53 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	–	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	–	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	–	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	–	–	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		RESET			0.1	0.4	–	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3V		–	–	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3V		–	–	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V _{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

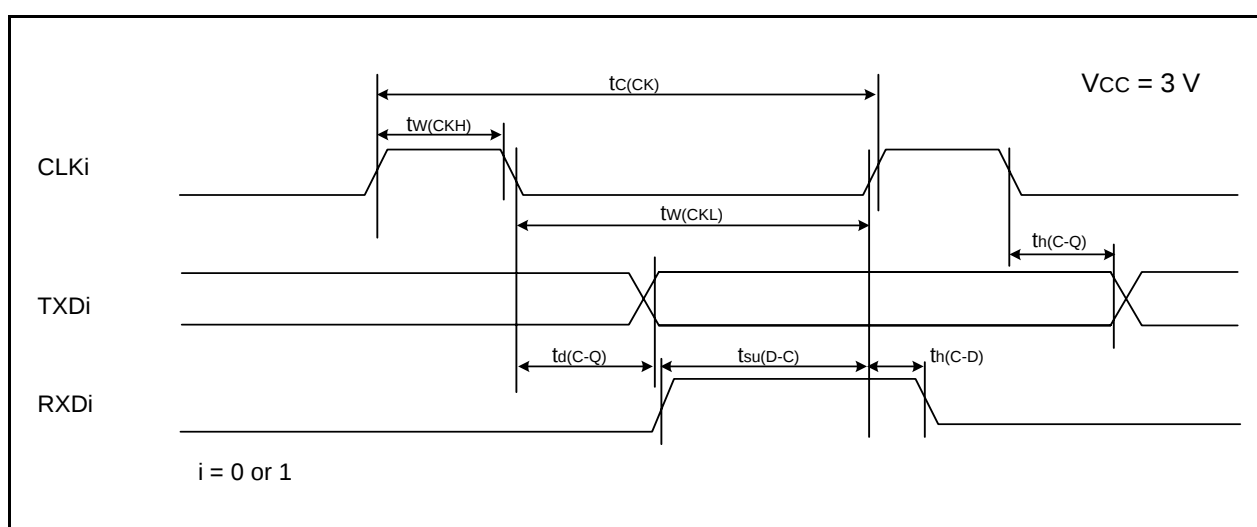
NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.57 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{w(CKH)}$	CLKi input “H” width	150	–	ns
$t_{w(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

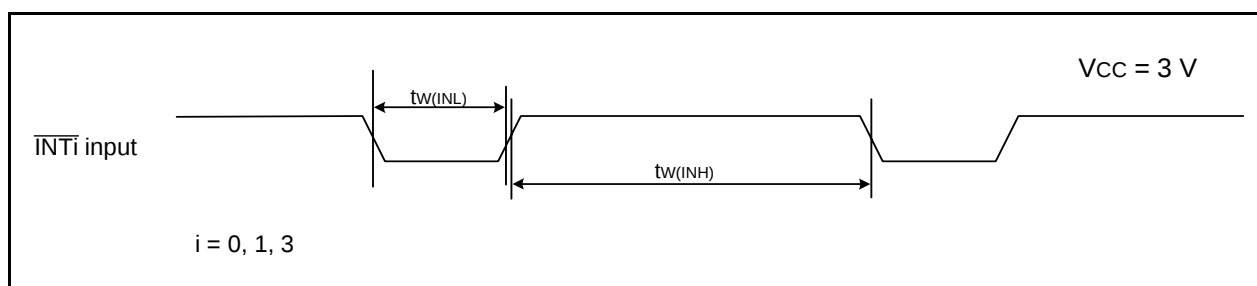
i = 0 or 1

**Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.58 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input “H” width	380 ⁽¹⁾	–	ns
$t_{w(INL)}$	$\overline{INTi}$ input “L” width	380 ⁽²⁾	–	ns

NOTES:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.34 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	May 25, 2007	16	Figure 3.2 part number revised
		30	Table 5.10 revised
		53	Table 5.39 NOTE4 added
		55	Table 5.42 revised
1.40a	Jun 14, 2007	5, 7	Table 1.3 and Table 1.4 revised
2.00	Mar 01, 2008	1, 49	1.1, 5.2 "J and K versions are ..." deleted
		5, 7	Table 1.3, Table 1.4 revised
		11	Table 1.6 NOTE3 added
		15, 16	Figure 3.1, Figure 3.2; "Expanded area" deleted
		17	Table 4.1 "002Ch" added
		18	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"
		24, 49	Table 5.2, Table 5.35; NOTE2 revised
2.10	Sep 26, 2008	30	Table 5.10 revised, NOTE4 added
		–	"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E
		26, 51	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		27, 52	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		53	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added
			Table 5.40 revised
		54	Table 5.41 revised
			Figure 5.22 revised

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