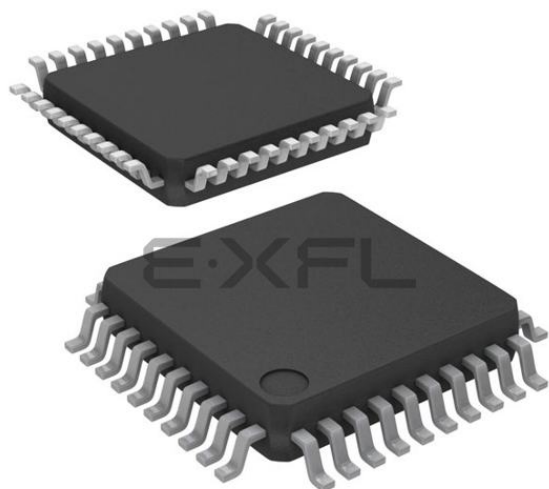




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Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21274kfp-w4

Table 1.4 Product Information for R8C/27 Group

Current of Sep. 2008

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks		
	Program ROM	Data flash					
R5F21272SNFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version		
R5F21274SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A			
R5F21275SNFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21276SNFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21272SDFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version		
R5F21274SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A			
R5F21275SDFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21276SDFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21274JFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	J version		
R5F21276JFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21274KFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	K version		
R5F21276KFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21272SNXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version	Factory programming product ⁽¹⁾	
R5F21274SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A			
R5F21275SNXXXFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21276SNXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21272SDXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version		
R5F21274SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A			
R5F21275SDXXXFP	24 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21276SDXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21274JXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	J version		
R5F21276JXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			
R5F21274KXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	K version		
R5F21276KXXXFP	32 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A			

NOTE:

1. The user ROM is programmed before shipment.

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

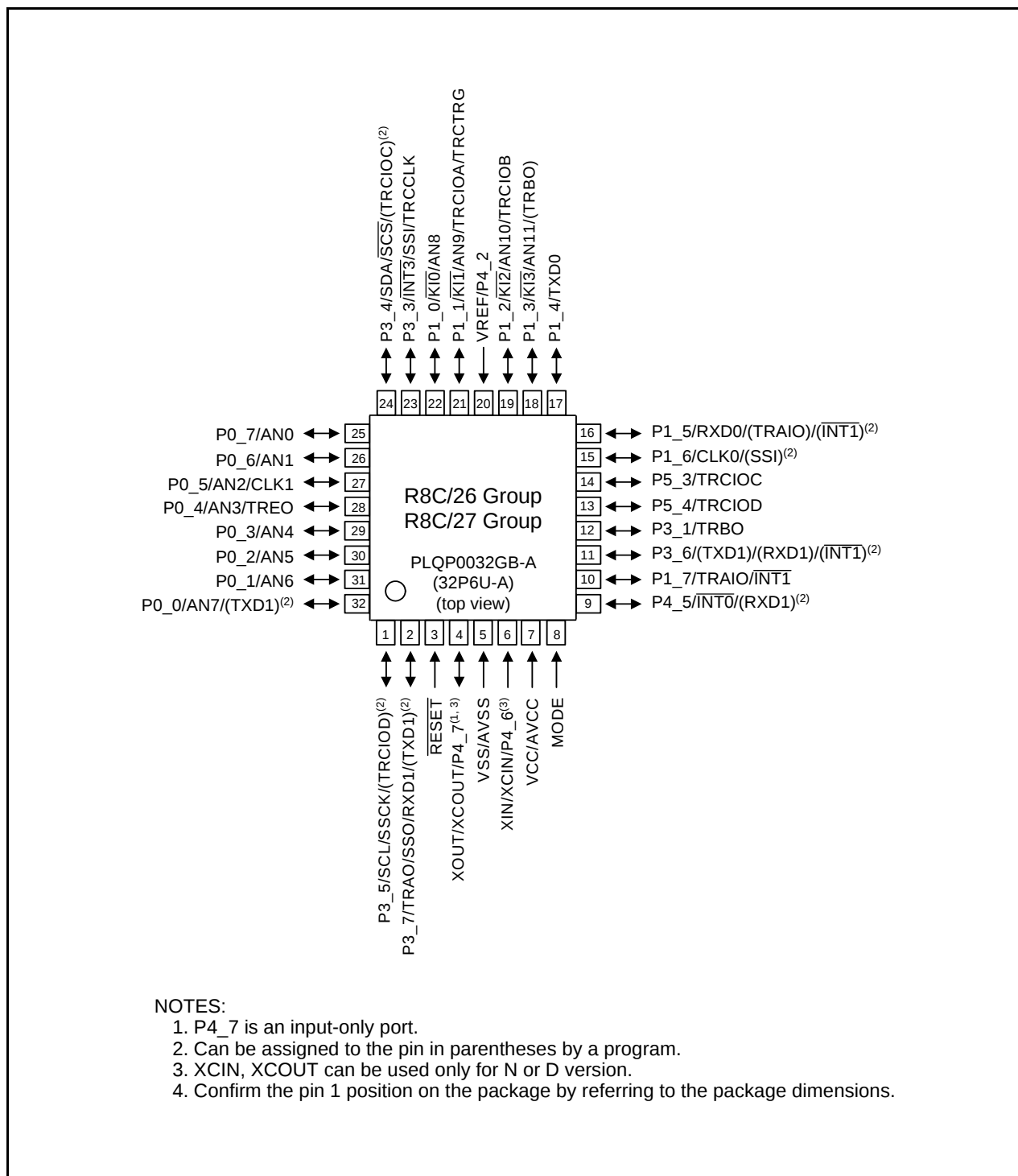


Figure 1.4 Pin Assignments (Top View)

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/26 Group

Figure 3.1 is a Memory Map of R8C/26 Group. The R8C/26 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

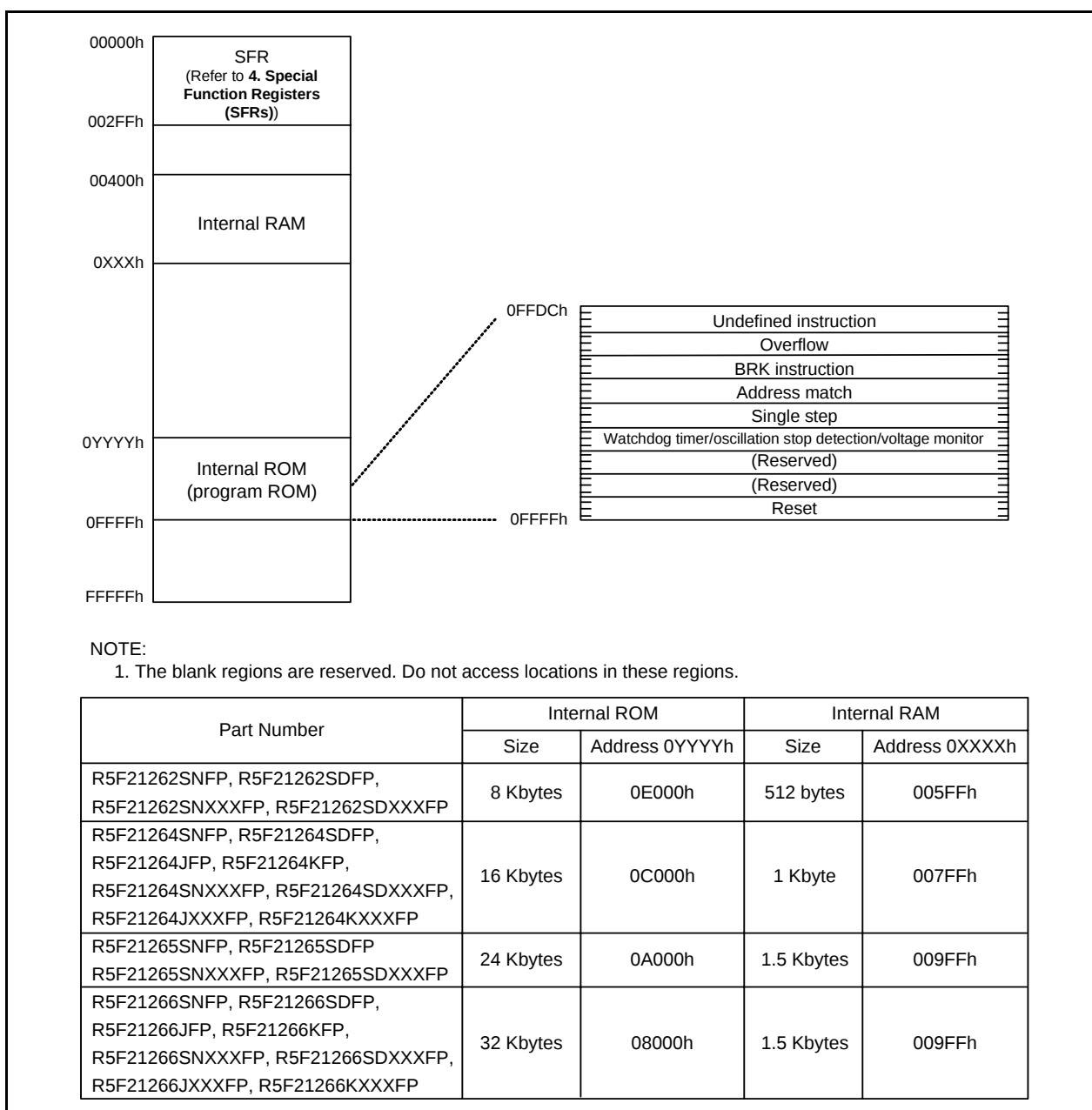


Figure 3.1 Memory Map of R8C/26 Group

Table 4.3 SFR Information (3)⁽¹⁾

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register ⁽²⁾	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register ⁽²⁾	SSRDR / ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾	R8C/26 Group	100 ⁽³⁾	–	–	times
		R8C/27 Group	1,000 ⁽³⁾	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
t _{rth}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

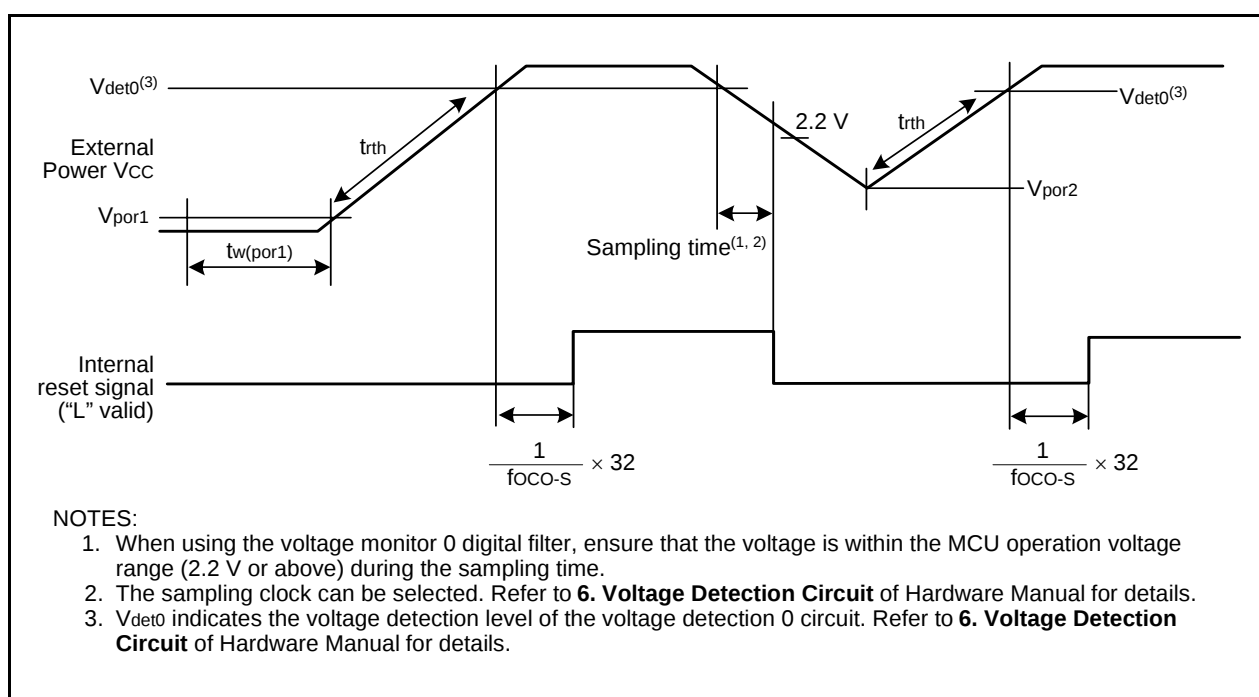
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 2.7 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38	40	42	MHz
		V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	37.6	40	42.4	MHz
		V _{CC} = 2.2 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34	40	46	MHz
		V _{CC} = 5.0 V ± 10% -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	40.8	MHz
		V _{CC} = 5.0 V ± 10% -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	40.8	MHz
		V _{CC} = 5.0 V, T _{opr} = 25°C	—	36.864	—	MHz
—	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register ⁽⁴⁾	V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	—	3%	%
—	Value in FRA1 register after reset		08h ⁽³⁾	—	F7h ⁽³⁾	—
—	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	—	+0.3	—	MHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	400	—	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	15	—	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	—	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		—	—	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
t _{OR}	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Table 5.15 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I _{OH} = -5 mA		V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA		V _{CC} - 0.5	—	V _{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I _{OL} = 5 mA		—	—	2.0	V
			I _{OL} = 200 μA		—	—	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH	I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	—	V
		RESET			0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5 V		30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN			—	1.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

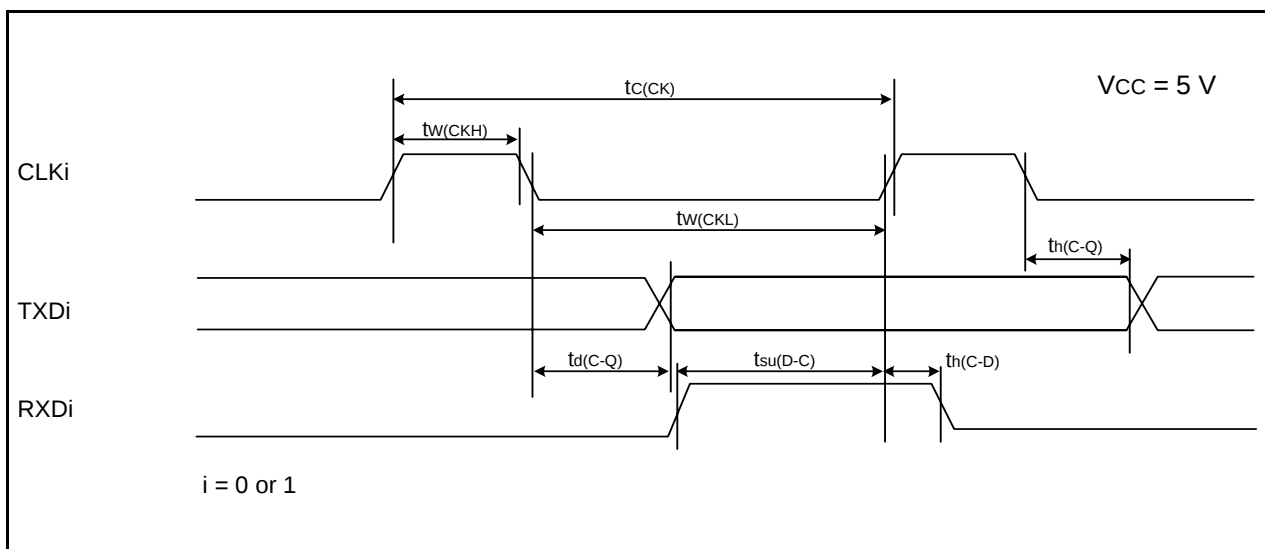
NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

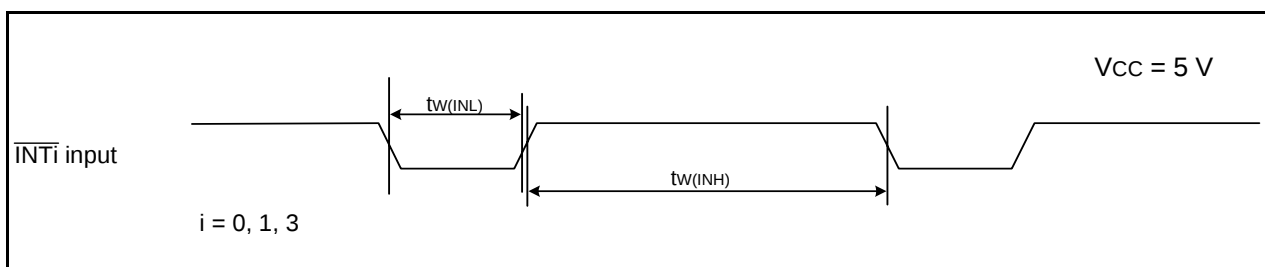
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

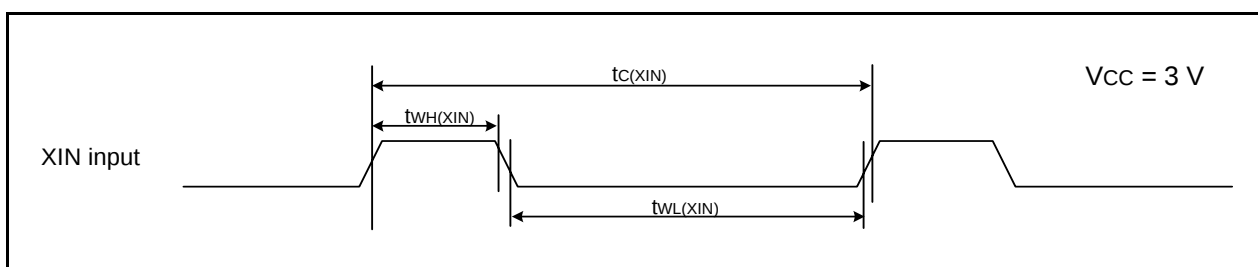
NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.24 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.25 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

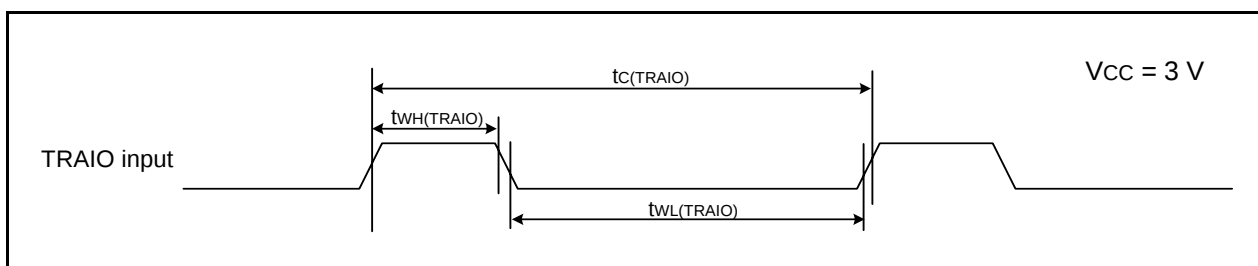
**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.28 Electrical Characteristics (5) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}, \overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{TRAIO}}, \overline{\text{RXD0}}, \overline{\text{RXD1}}, \overline{\text{CLK0}}, \overline{\text{CLK1}}, \overline{\text{SSI}}, \overline{\text{SCL}}, \overline{\text{SDA}}, \overline{\text{SSO}}$			0.05	0.3	—	V
		$\overline{\text{RESET}}$			0.05	0.15	—	V
I _{IH}	Input "H" current		V _I = 2.2 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		100	200	600	kΩ
R _{FXIN}	Feedback resistance	XIN			—	5	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	35	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Table 5.29 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	3.5	—	mA
		High-speed on-chip oscillator mode	—	3.5	—	mA
		Low-speed on-chip oscillator mode	—	100	230	μA
		Low-speed clock mode	—	100	230	μA
		Wait mode	—	22	60	μA
		Stop mode	—	0.7	3.0	μA

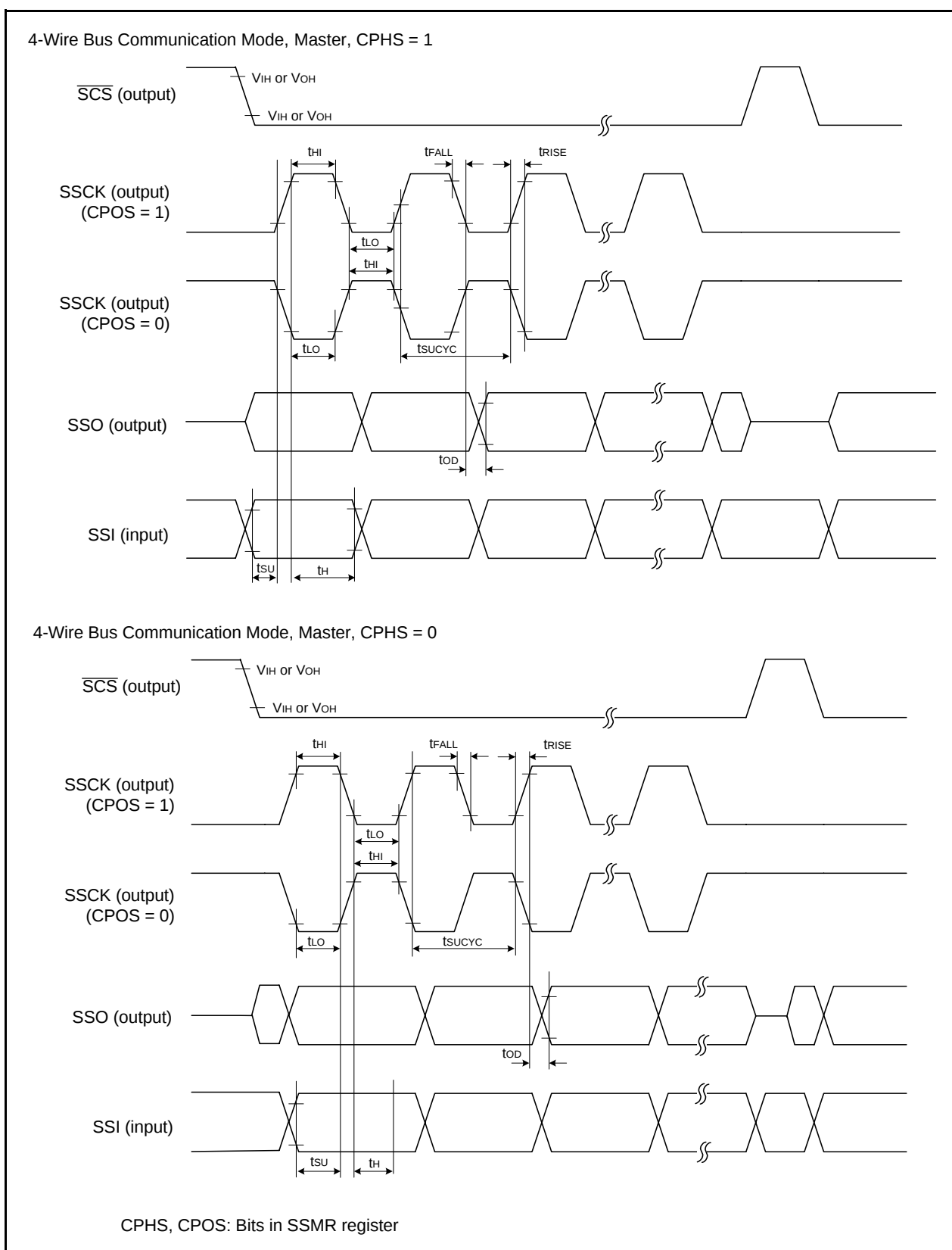


Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

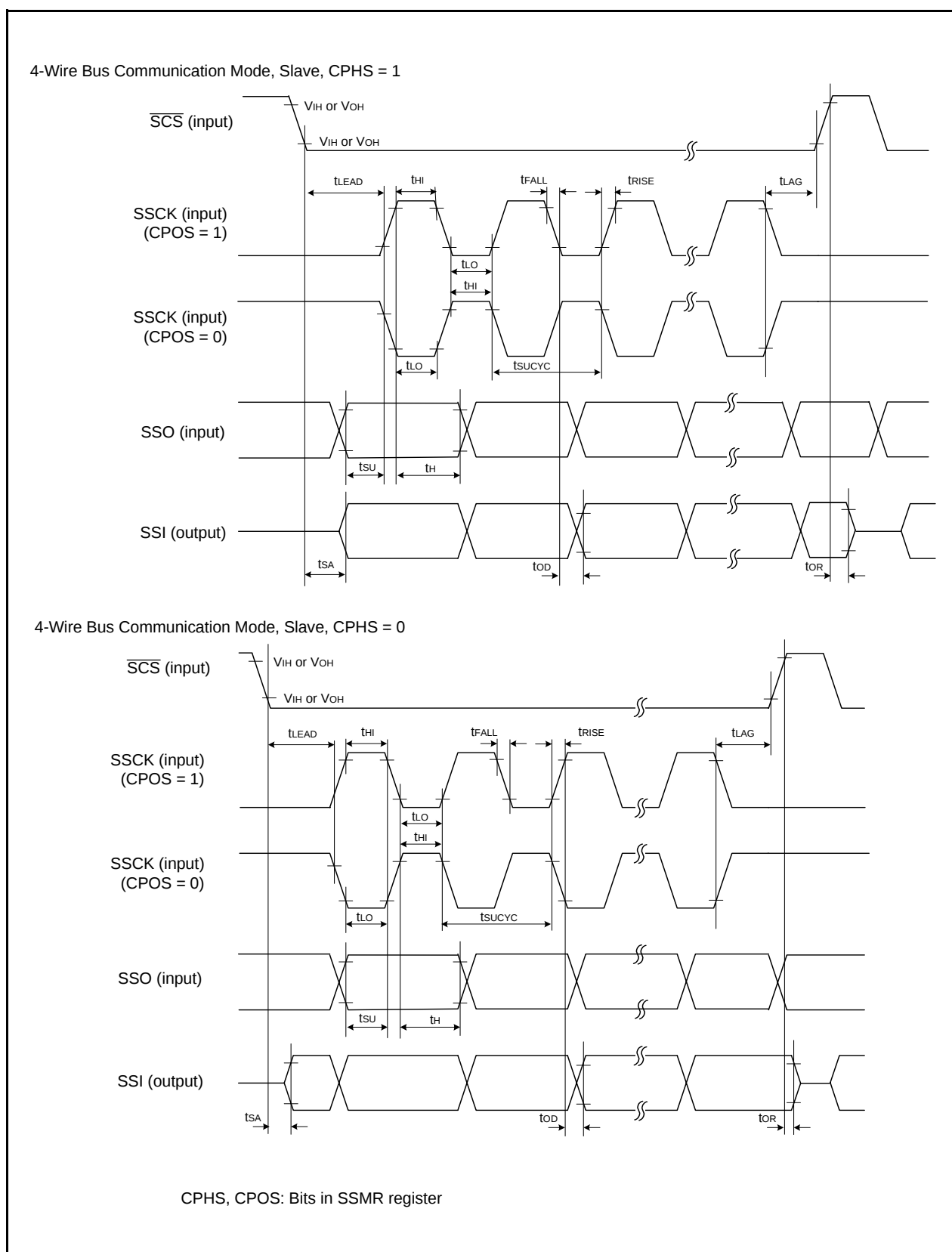
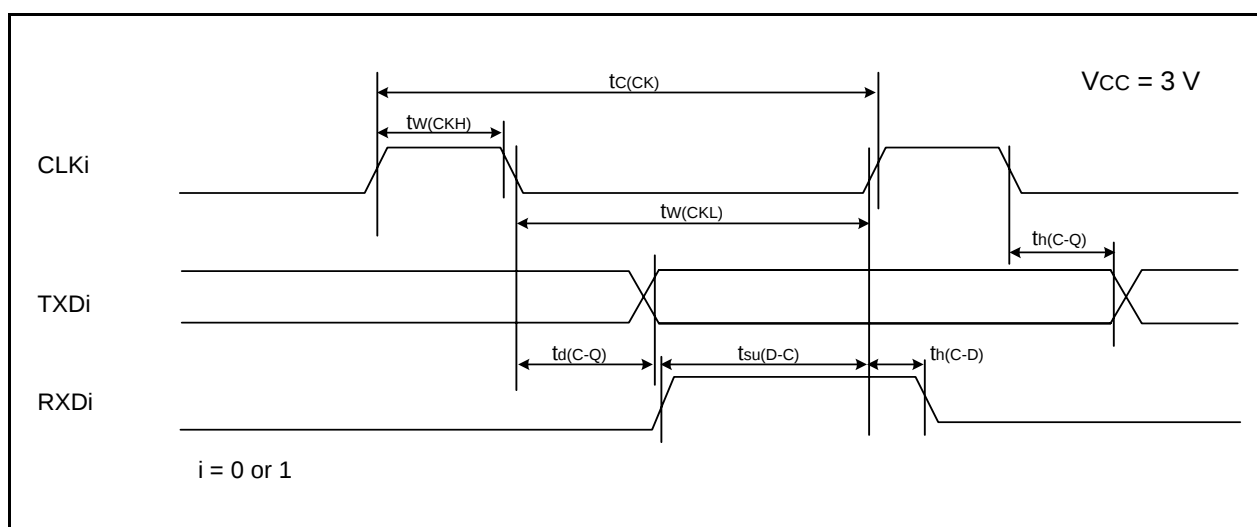


Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.57 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

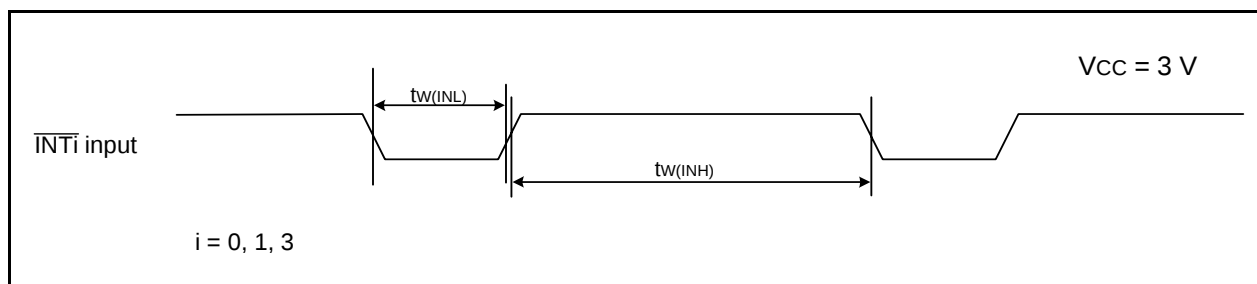
i = 0 or 1

**Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.58 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.34 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	May 25, 2007	16	Figure 3.2 part number revised
		30	Table 5.10 revised
		53	Table 5.39 NOTE4 added
		55	Table 5.42 revised
1.40a	Jun 14, 2007	5, 7	Table 1.3 and Table 1.4 revised
2.00	Mar 01, 2008	1, 49	1.1, 5.2 "J and K versions are ..." deleted
		5, 7	Table 1.3, Table 1.4 revised
		11	Table 1.6 NOTE3 added
		15, 16	Figure 3.1, Figure 3.2; "Expanded area" deleted
		17	Table 4.1 "002Ch" added
		18	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"
		24, 49	Table 5.2, Table 5.35; NOTE2 revised
2.10	Sep 26, 2008	30	Table 5.10 revised, NOTE4 added
		–	"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E
		26, 51	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		27, 52	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		53	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added
			Table 5.40 revised
		54	Table 5.41 revised
			Figure 5.22 revised

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