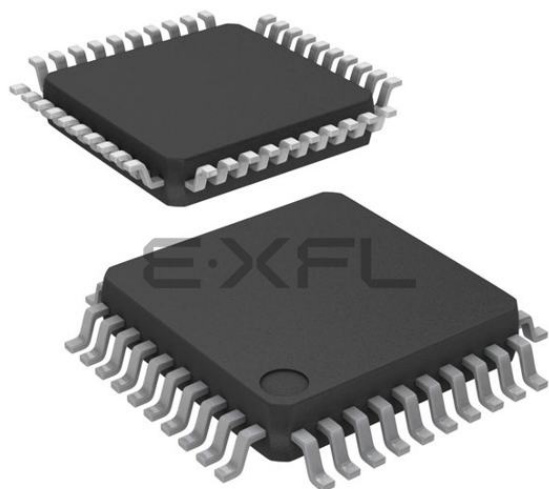




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21274syfp-x6

Table 1.2 Functions and Specifications for R8C/27 Group

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.4 Product Information of R8C/27 Group
Peripheral Functions	Ports	I/O ports: 25 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Start-on-reset selectable
	Interrupts	Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation-stopped detector	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾
Package		32-pin molded-plastic LQFP

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

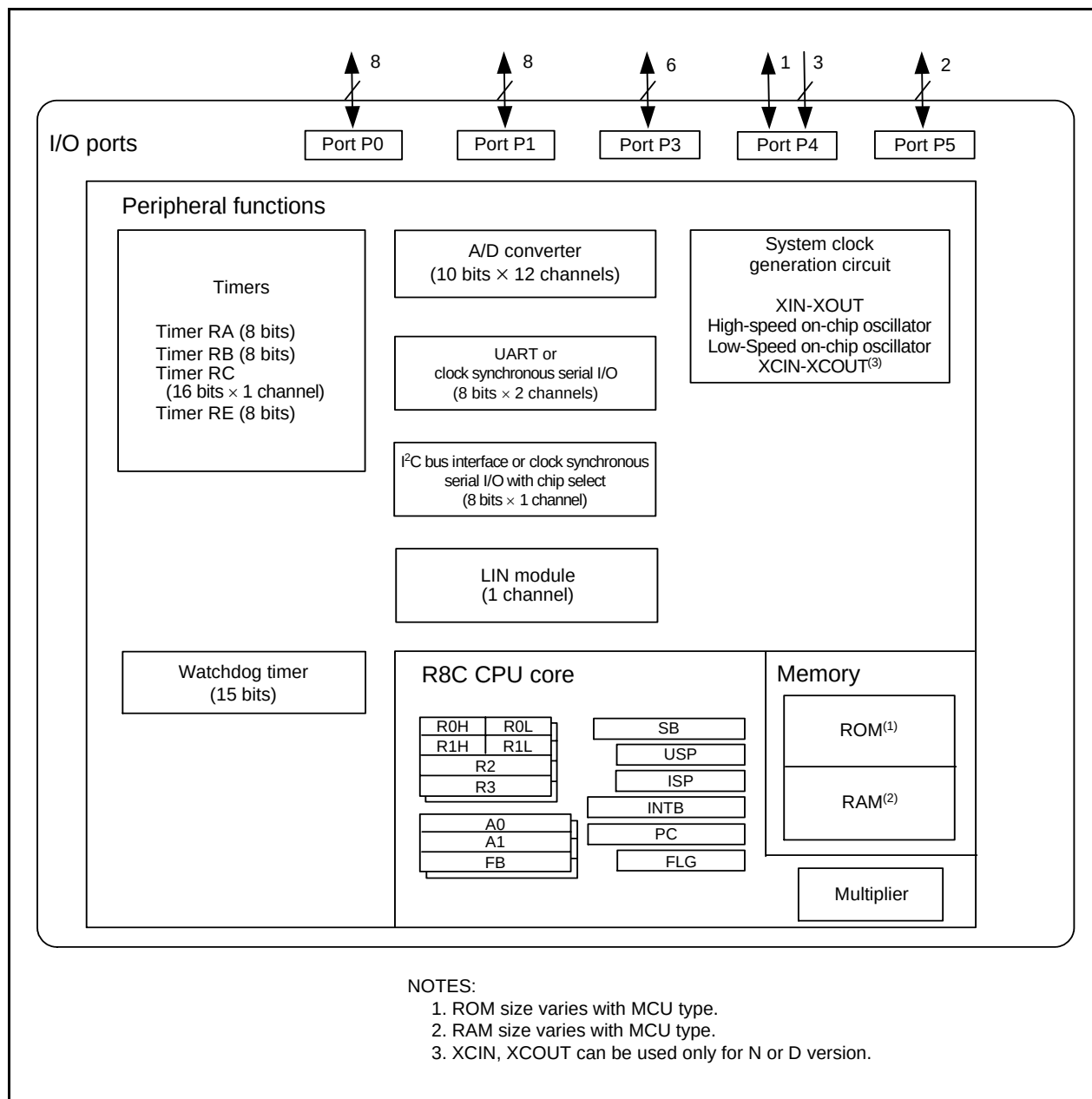


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/26 Group and Table 1.4 lists the Product Information for R8C/27 Group.

Table 1.3 Product Information for R8C/26 Group

Current of Sep. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F21262SNFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version		
R5F21264SNFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SNXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version	Factory programming product ⁽¹⁾	
R5F21264SNXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SNXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SNXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21262SDXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version		
R5F21264SDXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A			
R5F21265SDXXXFP	24 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21266SDXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264JXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	J version		
R5F21266JXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			
R5F21264KXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	K version		
R5F21266KXXXFP	32 Kbytes	1.5 Kbytes	PLQP0032GB-A			

NOTE:

1. The user ROM is programmed before shipment.

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C bus Interface	A/D Converter
1		P3_5		(TRCIOD) ⁽¹⁾		SSCK	SCL	
2		P3_7		TRA0	RXD1/ (TXD1) ^(1, 3)	SSO		
3	RESET							
4	XOUT/XCOUT ⁽²⁾	P4_7						
5	VSS/AVSS							
6	XIN/XCIN ⁽²⁾	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	INT0		(RXD1) ^(1, 3)			
10		P1_7	INT1	TRAIO				
11		P3_6	(INT1) ⁽¹⁾		(TXD1)/ (RXD1) ^(1, 3)			
12		P3_1		TRBO				
13		P5_4		TRCIOD				
14		P5_3		TRCIOC				
15		P1_6			CLK0	(SSI) ⁽¹⁾		
16		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0			
17		P1_4			TXD0			
18		P1_3	KI3	(TRBO)				AN11
19		P1_2	KI2	TRCIOB				AN10
20	VRFF	P4_2						
21		P1_1	KI1	TRCIOA/ TRCTRG				AN9
22		P1_0	KI0					AN8
23		P3_3	INT3	TRCCLK		SSI		
24		P3_4		(TRCIOC) ⁽¹⁾		SCS	SDA	
25		P0_7						AN0
26		P0_6						AN1
27		P0_5			CLK1			AN2
28		P0_4		TREO				AN3
29		P0_3						AN4
30		P0_2						AN5
31		P0_1						AN6
32		P0_0			(TXD1) ^(1, 3)			AN7

NOTES:

1. This can be assigned to the pin in parentheses by a program.
2. XCIN, XCOU can be used only for N or D version.
3. For the combination of using pins TXD1 and RXD1, refer to **Figure 15.7 Registers PINSR1 and PMR** of Hardware Manual (REJ09B0278).

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽²⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4 ⁽³⁾	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6 ⁽³⁾	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7 ⁽³⁾	FRA7	When shipping
002Dh			
002Eh			
002Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 (2)	VCA1	00001000b
0032h	Voltage Detection Register 2 (2)	VCA2	• N, D version 00h(3) 00100000b(4) • J, K version 00h(7) 01000000b(8)
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register (5)	VW1C	• N, D version 00001000b • J, K version 0000X000b(7) 0100X001b(8)
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register (6)	VW0C	0000X000b(3)
0039h			0100X001b(4)
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register(9)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- The LVD00N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset or the LVD00N bit in the OFS register is set to 0, and hardware reset.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) These regions are reserved. Do not access locations in these regions.
- The LVD10N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 1 reset, or the LVD10N bit in the OFS register is set to 0 and hardware reset.
- Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾	R8C/26 Group	100 ⁽³⁾	–	–	times
		R8C/27 Group	1,000 ⁽³⁾	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 2.7 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38	40	42	MHz
		V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	37.6	40	42.4	MHz
		V _{CC} = 2.2 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34	40	46	MHz
		V _{CC} = 5.0 V ± 10% -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	40.8	MHz
		V _{CC} = 5.0 V ± 10% -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	40.8	MHz
		V _{CC} = 5.0 V, T _{opr} = 25°C	—	36.864	—	MHz
—	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register ⁽⁴⁾	V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	—	3%	%
—	Value in FRA1 register after reset		08h ⁽³⁾	—	F7h ⁽³⁾	—
—	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	—	+0.3	—	MHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	400	—	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	15	—	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	—	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		—	—	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
t _{OR}	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Table 5.17 Electrical Characteristics (3) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS}	Wait mode	—	25	75	μA
		Stop mode	—	0.8	3.0	μA

Table 5.22 Electrical Characteristics (3) [V_{CC} = 3 V]

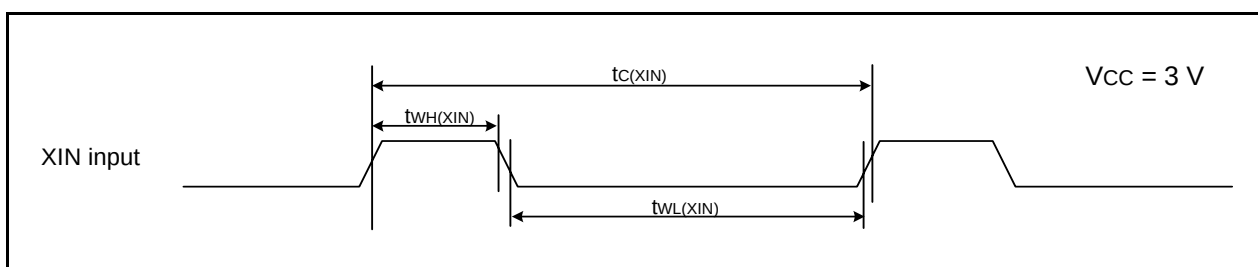
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}, \overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{TRAIO}}, \overline{\text{RXD0}}, \overline{\text{RXD1}}, \overline{\text{CLK0}}, \overline{\text{CLK1}}, \overline{\text{SSI}}, \overline{\text{SCL}}, \overline{\text{SDA}}, \overline{\text{SSO}}$			0.1	0.3	—	V
		$\overline{\text{RESET}}$			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

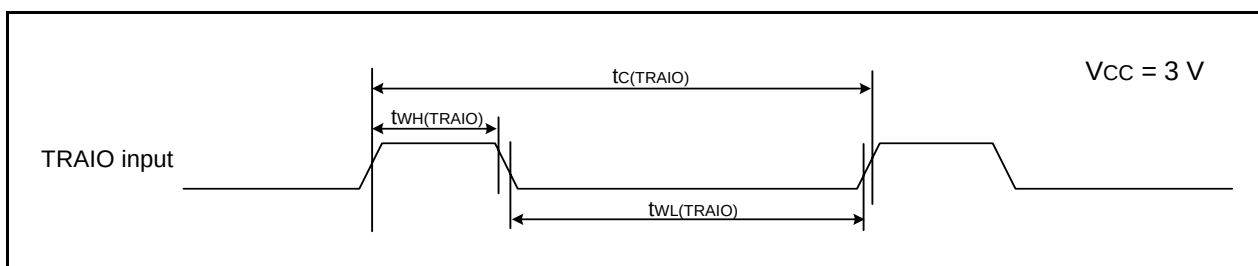
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.24 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.25 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

**Table 5.29 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	—	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	100	230	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	—	100	230	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	—	25	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	22	60	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	20	55	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	3.0	—	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	1.8	—	μA
			Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.7	3.0
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	1.1	—	μA

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} + 0.3	V
V _O	Output voltage		-0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	-40 °C ≤ T _{opr} ≤ 85 °C	300	mW
		85 °C ≤ T _{opr} ≤ 125 °C	125	mW
T _{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.35 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage			2.7	—	5.5	V
V _{SS} /AV _{SS}	Supply voltage			—	0	—	V
V _{IH}	Input "H" voltage			0.8 V _{CC}	—	V _{CC}	V
V _{IL}	Input "L" voltage			0	—	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output "H" current	Sum of all pins I _{OH} (peak)		—	—	-60	mA
I _{OH} (peak)	Peak output "H" current			—	—	-10	mA
I _{OH} (avg)	Average output "H" current			—	—	-5	mA
I _{OL} (sum)	Peak sum output "L" currents	Sum of all pins I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	Peak output "L" currents			—	—	10	mA
I _{OL} (avg)	Average output "L" current			—	—	5	mA
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
—	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version)	0	—	20	MHz
			3.0 V ≤ V _{CC} ≤ 5.5 V (K version)	0	—	16	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	—	125	—	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	—	—	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected	—	—	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.42 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature · supply voltage dependence	V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾	38	40	42	MHz
		V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾	37.6	40	42.4	MHz
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	400	–	μA

NOTES:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

Table 5.43 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

Table 5.44 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.46 Timing Requirements of I²C bus Interface⁽¹⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cy} c + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cy} c + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cy} c + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cy} c ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cy} c ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cy} c ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cy} c ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cy} c ⁽²⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cy} c + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{cy}c = 1/f₁(s)

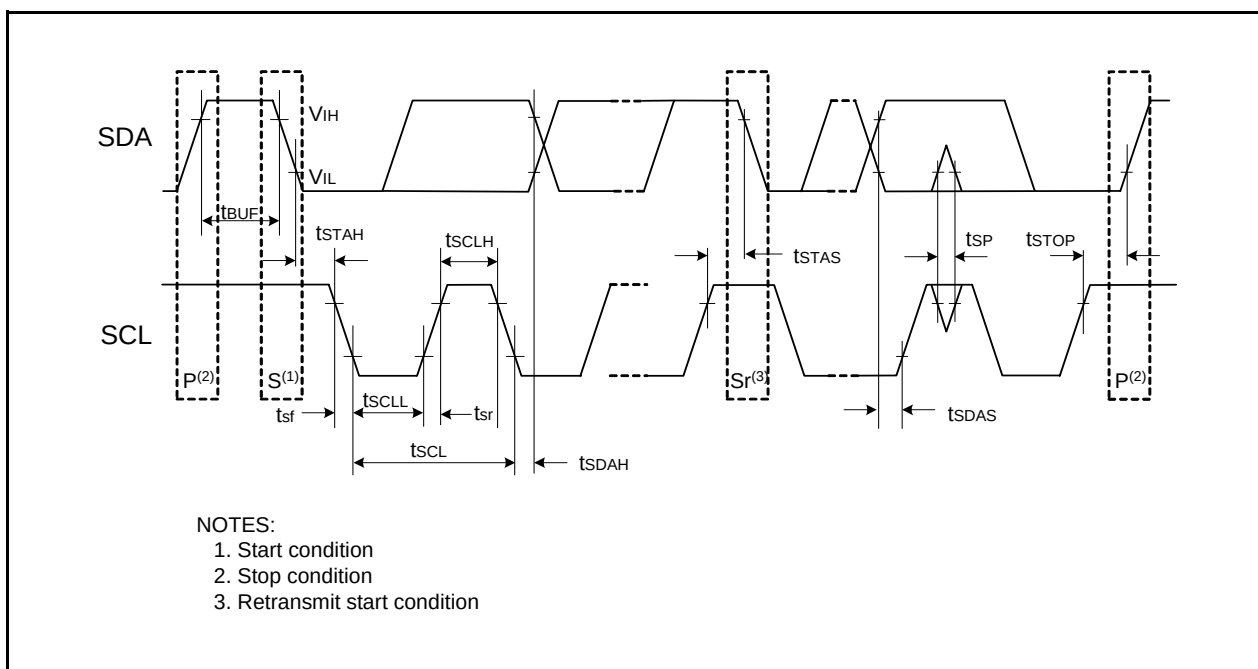
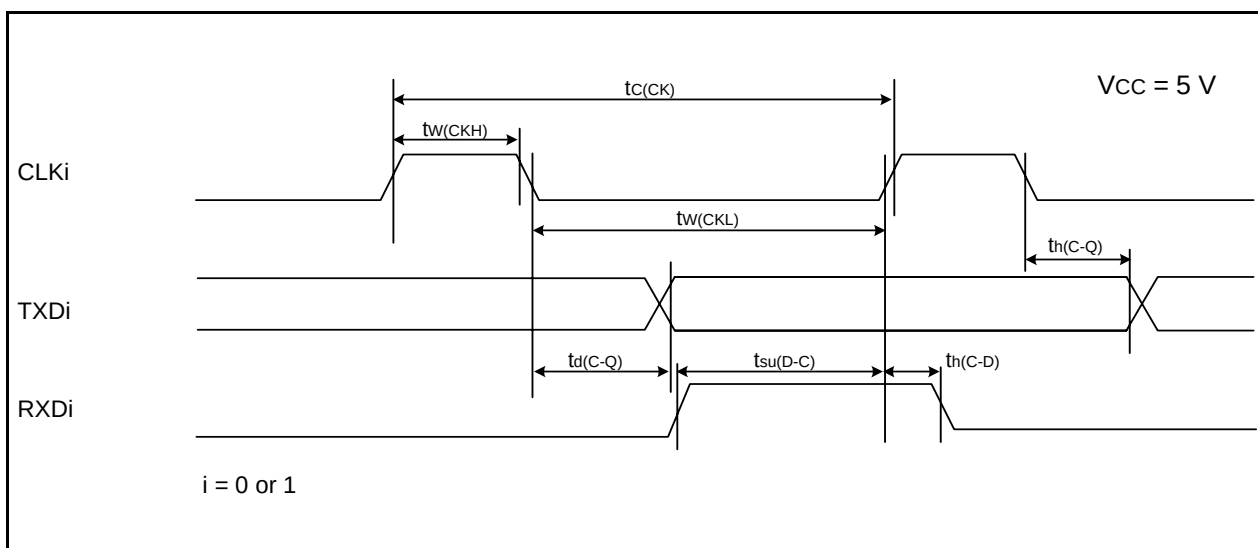
**Figure 5.26 I/O Timing of I²C bus Interface**

Table 5.51 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

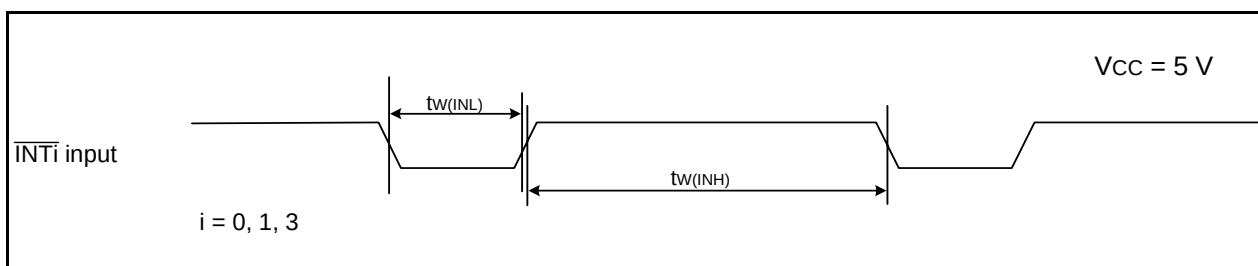
i = 0 or 1

**Figure 5.29 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.52 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.30 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

REVISION HISTORY	R8C/26 Group, R8C/27 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 08, 2006	27	Table 5.9, Figure 5.3 revised and Table 5.10 deleted
		28	Table 5.10, Table 5.11 revised
		34	Table 5.15 revised
		35	Table 5.16 revised
		36	Table 5.17 revised
		39	Table 5.22 revised
		40	Table 5.23 revised
		44	Table 5.29 revised
		47	Package Dimensions; "Diagrams showing the latest...website." added
1.10	Nov 29, 2006	All pages	"J, K version" added
		1	1 "J and K versions are under development...notice." added
		1.1	1.1 revised
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 NOTE3 added
		5	Table 1.3, Figure 1.2 revised
		6	Table 1.4, Figure 1.3 revised
		7	Figure 1.4 NOTE3 added
		8	Table 1.5 revised
		9	Table 1.6 NOTE2 added
		13	Figure 3.1 revised
		14	Figure 3.2 revised
		15	Table 4.1; "0000h to 003Fh" → "0000h to 002Fh" revised • NOTE3 added
		16	Table 4.2; "0040h to 007Fh" → "0030h to 007Fh" revised • 0032h, 0036h: "After reset" is revised • 0038h: NOTE revised • NOTES 2, 5, 6 revised and NOTE 7, 8 added
		19	Table 4.5 NOTE2 added
		28	Table 5.10 revised
		48 to 66	5.2 J, K Version added
1.20	Jan 17, 2007	18	Table 4.4 NOTE2 added
1.30	May 25, 2007	2	Table 1.1 revised
		3	Table 1.2 revised
		5	Table 1.3 revised
		6	Figure 1.2 revised
		7	Table 1.4 revised
		8	Figure 1.3 revised
		9	Figure 1.4 NOTE4 added
		15	Figure 3.1 part number revised