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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21276sdfp-v2">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21276sdfp-v2</a>

## 1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/26 Group and Table 1.2 outlines the Functions and Specifications for R8C/27 Group.

**Table 1.1 Functions and Specifications for R8C/26 Group**

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ( $f(XIN) = 20$ MHz, $VCC = 3.0$ to $5.5$ V) (other than K version) 62.5 ns ( $f(XIN) = 16$ MHz, $VCC = 3.0$ to $5.5$ V) (K version) 100 ns ( $f(XIN) = 10$ MHz, $VCC = 2.7$ to $5.5$ V) 200 ns ( $f(XIN) = 5$ MHz, $VCC = 2.2$ to $5.5$ V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to <b>Table 1.3 Product Information for R8C/26 Group</b>
Peripheral Functions	Ports	I/O ports: 25 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits $\times$ 1 channel Timer RB: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits $\times$ 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I <sup>2</sup> C bus Interface <sup>(1)</sup> Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Start-on-reset selectable
	Interrupts	Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits <ul style="list-style-type: none"> <li>XIN clock generation circuit (with on-chip feedback resistor)</li> <li>On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function</li> <li>XCIN clock generation circuit (32 kHz) (N, D version)</li> <li>Real-time clock (timer RE) (N, D version)</li> </ul>
	Oscillation-stopped detector	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to $5.5$ V ( $f(XIN) = 20$ MHz) (other than K version) $VCC = 3.0$ to $5.5$ V ( $f(XIN) = 16$ MHz) (K version) $VCC = 2.7$ to $5.5$ V ( $f(XIN) = 10$ MHz) $VCC = 2.2$ to $5.5$ V ( $f(XIN) = 5$ MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA ( $VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ( $VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 $\mu$ A ( $VCC = 3.0$ V, wait mode ( $f(XCIN) = 32$ kHz)) Typ. 0.7 $\mu$ A ( $VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to $5.5$ V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>
Package		32-pin molded-plastic LQFP

**NOTES:**

- I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
- Specify the D, K version if D, K version functions are to be used.

## 1.6 Pin Functions

Table 1.5 lists Pin Functions.

**Table 1.5 Pin Functions**

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 to 5.5 V (J, K version are 2.7 to 5.5 V) to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input (N, D version)	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUNT pins. To use an external clock, input it to the XCIN pin and leave the XCOUNT pin open.
XCIN clock output (N, D version)	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRA0	O	Timer RA output pin
	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIO, TRCIOD	I/O	Sharing output-compare output / input-capture input / PWM / PWM2 output pins
Timer RE	TREO	O	Timer RE output pin
Serial interface	CLK0, CLK1	I/O	Clock I/O pin
	RXD0, RXD1	I	Receive data input pin
	TXD0, TXD1	O	Transmit data output pin
I <sup>2</sup> C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_7, P1_0 to P1_7, P3_1, P3_3 to P3_7, P4_5, P5_3, P5_4	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_7 also function as LED drive ports (N, D version).
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input      O: Output      I/O: Input and output

### 3. Memory

#### 3.1 R8C/26 Group

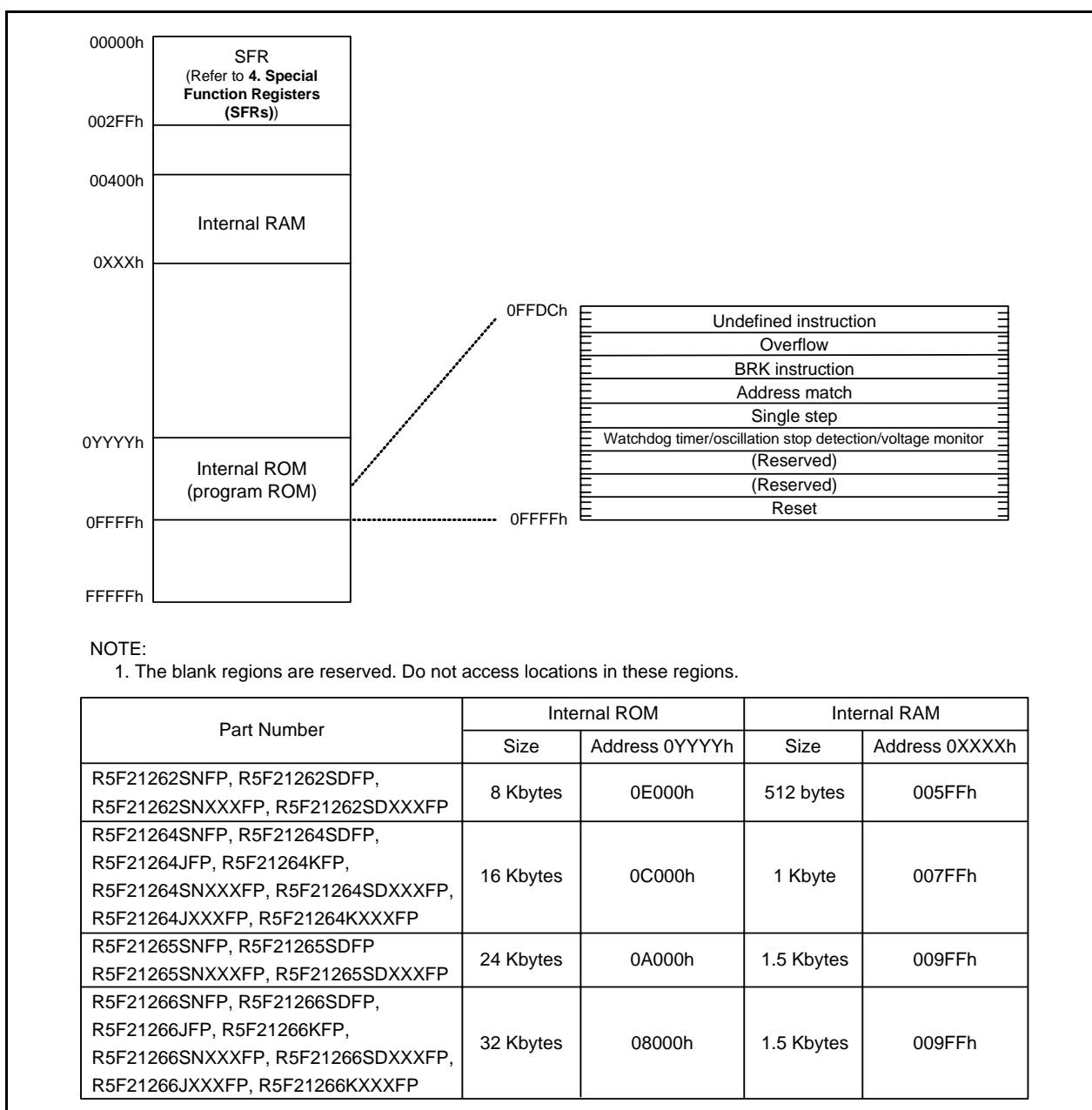
Figure 3.1 is a Memory Map of R8C/26 Group. The R8C/26 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



**Figure 3.1 Memory Map of R8C/26 Group**

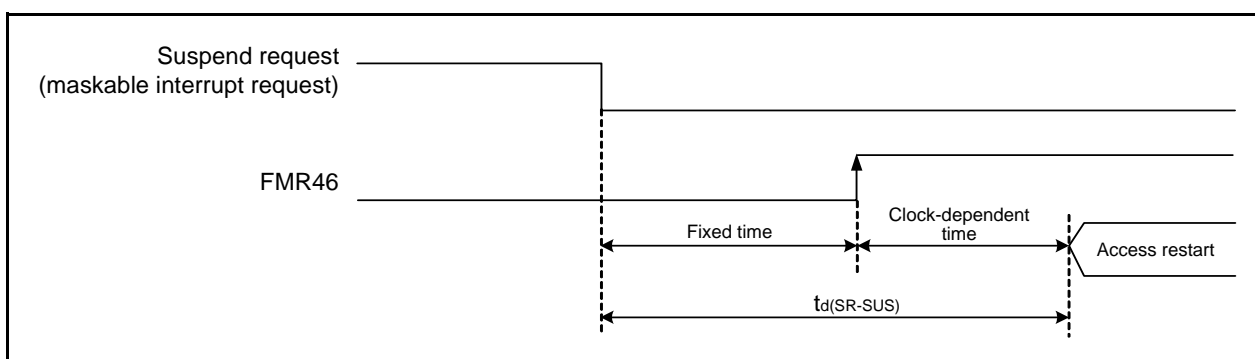


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det0</sub>	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, V <sub>CC</sub> = 5.0 V	—	0.9	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		—	—	300	μs
V <sub>ccmin</sub>	MCU operating voltage minimum value		2.2	—	—	V

## NOTES:

1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage detection level <sup>(4)</sup>		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time <sup>(2)</sup>		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs

## NOTES:

1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.  
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time <sup>(2)</sup>		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs

## NOTES:

1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

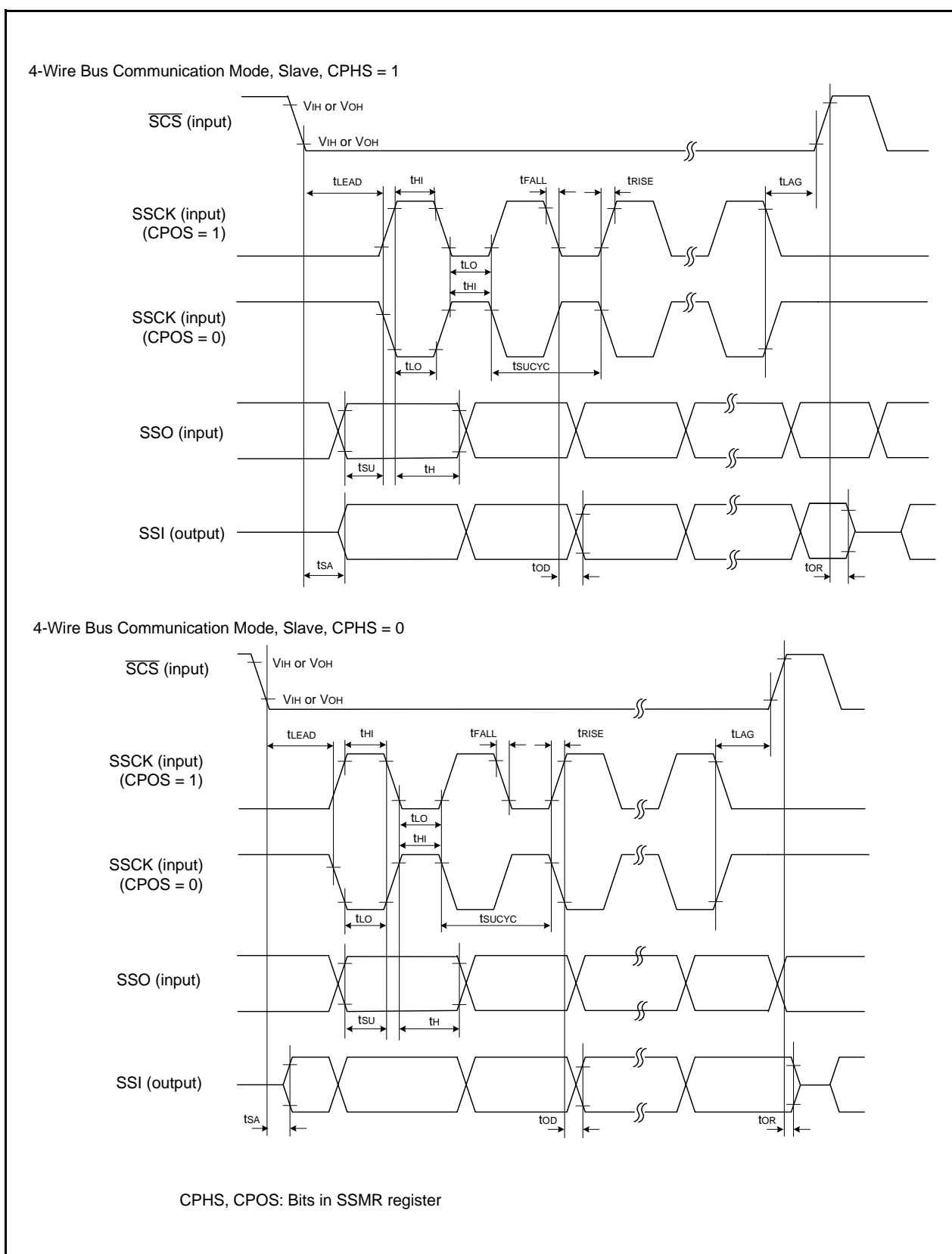
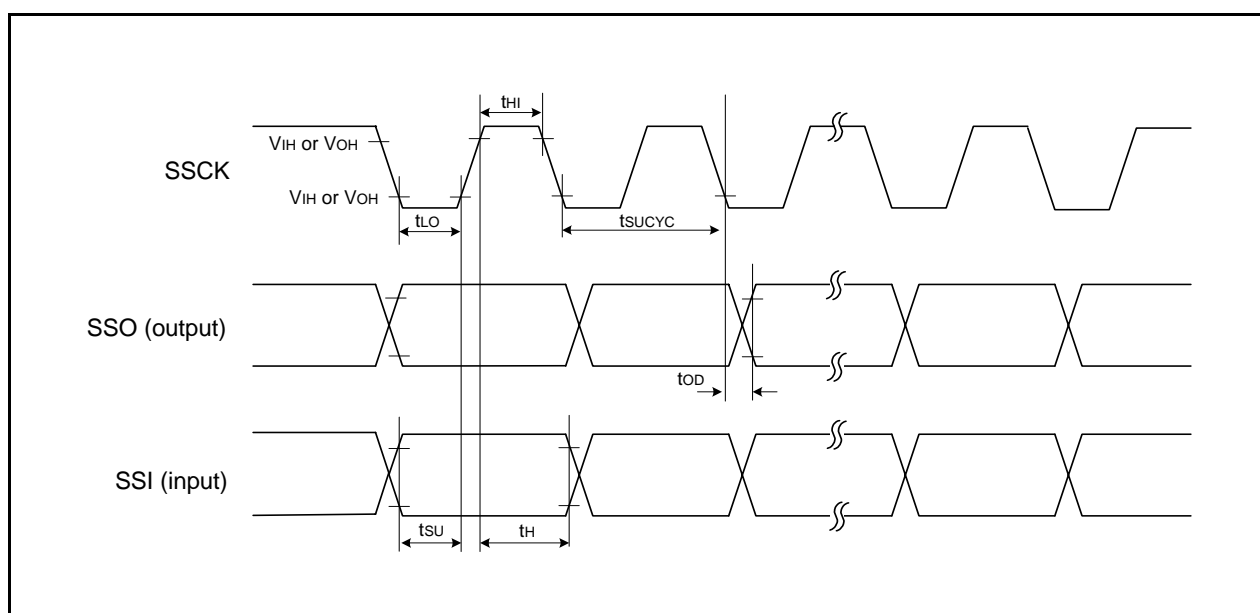


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)



**Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)**

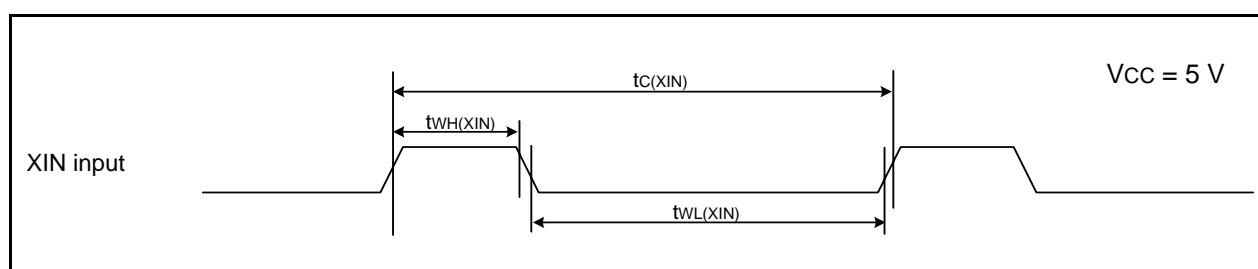
**Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]**  
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	—	10	17	mA
		High-speed on-chip oscillator mode	—	10	15	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Low-speed clock mode	—	130	300	μA
		Low-speed clock mode	—	30	—	μA

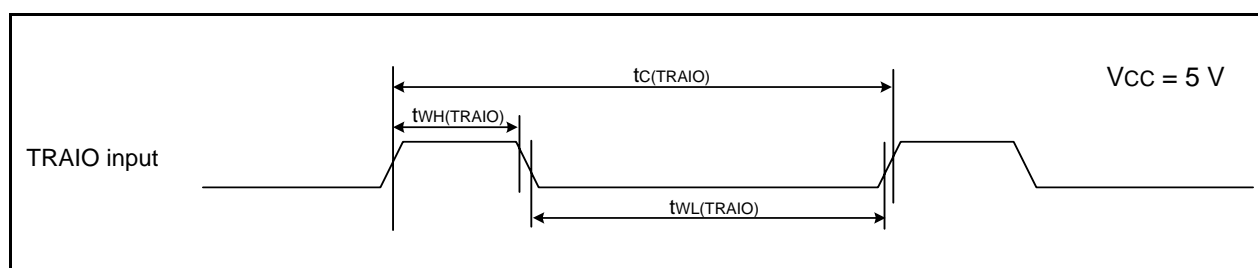


**Timing Requirements****(Unless Otherwise Specified:  $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = 25^{\circ}\text{C}$ ) [ $V_{CC} = 5\text{ V}$ ]****Table 5.18 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	$\mu\text{s}$
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	$\mu\text{s}$
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	$\mu\text{s}$

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input**

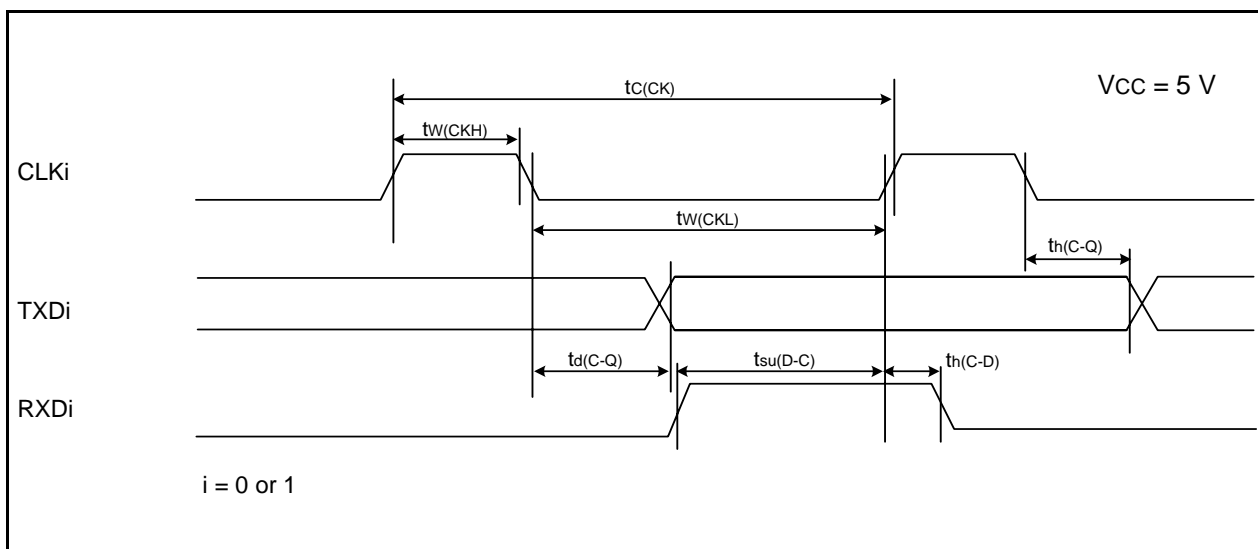
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

**Figure 5.9 TRAIO Input Timing Diagram when  $V_{CC} = 5\text{ V}$**

**Table 5.20 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

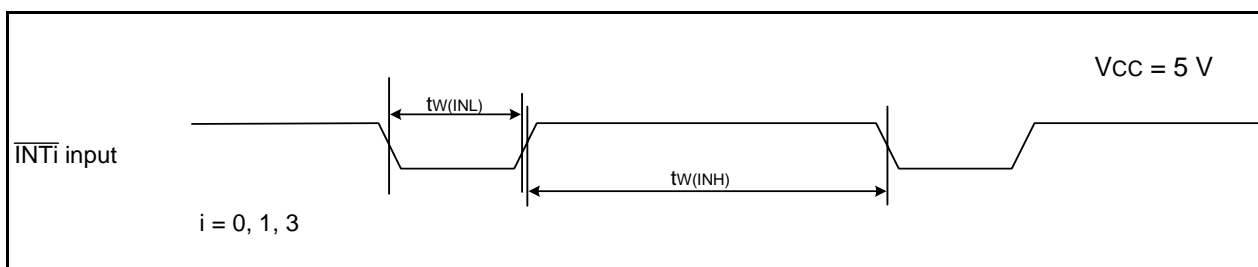
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt  $\overline{INTi}$  (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 <sup>(2)</sup>	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 5 V**

**Table 5.29 Electrical Characteristics (6) [V<sub>CC</sub> = 2.2 V]  
(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

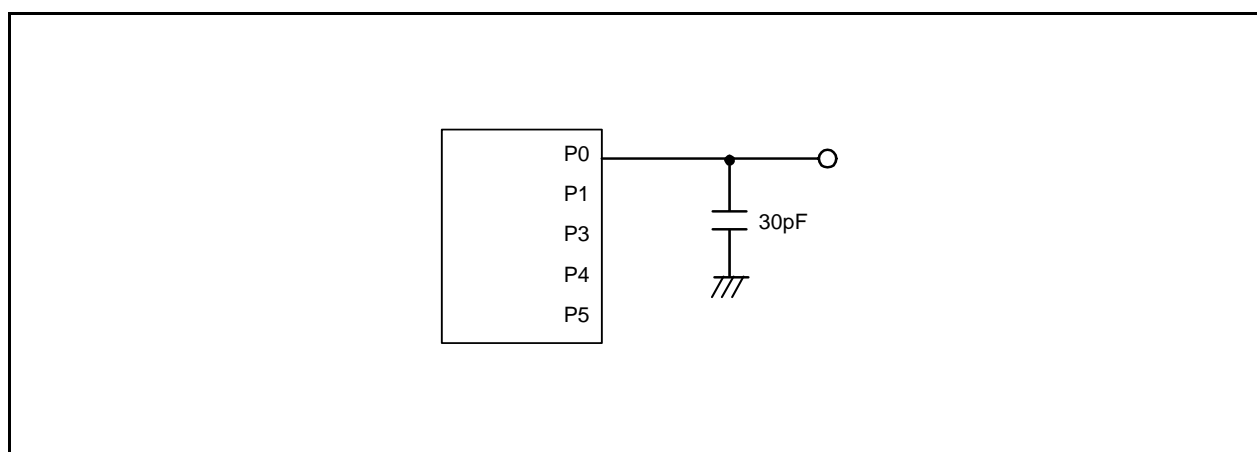
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V <sub>SS</sub>	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on f <sub>OCO</sub> = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN clock off High-speed on-chip oscillator on f <sub>OCO</sub> = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1			μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1			μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
		Stop mode	XIN clock off, T <sub>opr</sub> = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA
			XIN clock off, T <sub>opr</sub> = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA

**Table 5.36 A/D Converter Characteristics**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bits
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	$\pm 3$	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	$\pm 2$	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	$\pm 5$	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	$\pm 2$	LSB
$R_{ladder}$	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
$t_{conv}$	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	$\mu\text{s}$
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	$\mu\text{s}$
$V_{ref}$	Reference voltage			2.7	—	$AV_{CC}$	V
$V_{IA}$	Analog input voltage <sup>(2)</sup>			0	—	$AV_{CC}$	V
—	A/D operating clock frequency	Without sample and hold		0.25	—	10	MHz
		With sample and hold		1	—	10	MHz

**NOTES:**

1.  $AV_{CC} = 2.7$  to  $5.5 \text{ V}$  at  $T_{opr} = -40$  to  $85^\circ\text{C}$  (J version) /  $-40$  to  $125^\circ\text{C}$  (K version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Figure 5.20 Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

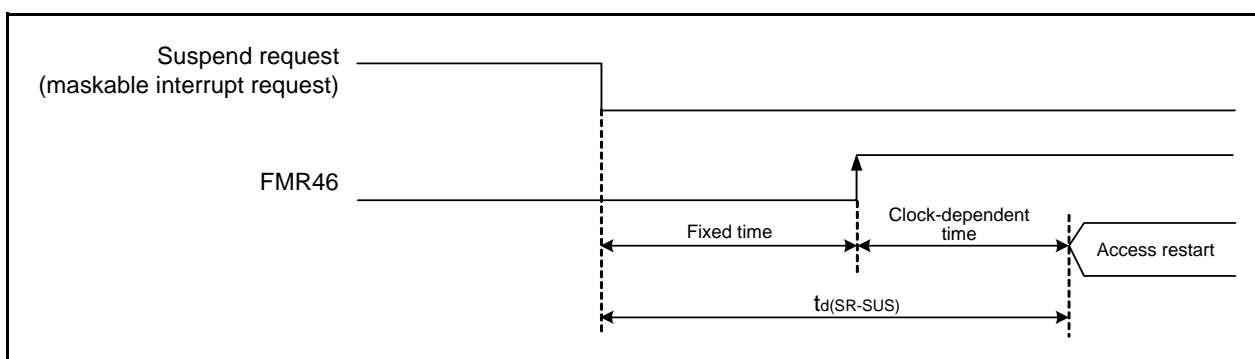


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage detection level <sup>(2, 4)</sup>		2.70	2.85	3.0	V
t <sub>d</sub> (V <sub>det1</sub> -A)	Voltage monitor 1 reset generation time <sup>(5)</sup>		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d</sub> (E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs
V <sub>ccmin</sub>	MCU operating voltage minimum value		2.70	—	—	V

## NOTES:

1. The measurement condition is V<sub>CC</sub> = 2.7 to 5.5 V and T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V<sub>det2</sub> > V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.  
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V<sub>det1</sub> when V<sub>CC</sub> falls. When using the digital filter, its sampling time is added to t<sub>d</sub>(V<sub>det1</sub>-A). When using the voltage monitor 1 reset, maintain this time until V<sub>CC</sub> = 2.0 V after the voltage passes V<sub>det1</sub> when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage detection level <sup>(2)</sup>		3.3	3.6	3.9	V
t <sub>d</sub> (V <sub>det2</sub> -A)	Voltage monitor 2 reset/interrupt request generation time <sup>(3, 5)</sup>		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d</sub> (E-A)	Waiting time until voltage detection circuit operation starts <sup>(4)</sup>		—	—	100	μs

## NOTES:

1. The measurement condition is V<sub>CC</sub> = 2.7 to 5.5 V and T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V<sub>det2</sub> > V<sub>det1</sub>.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes V<sub>det2</sub>.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to t<sub>d</sub>(V<sub>det2</sub>-A). When using the voltage monitor 2 reset, maintain this time until V<sub>CC</sub> = 2.0 V after the voltage passes V<sub>det2</sub> when the power supply falls.

**Table 5.45 Timing Requirements of Clock Synchronous Serial I/O with Chip Select<sup>(1)</sup>**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc <sup>(2)</sup>
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc <sup>(2)</sup>
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc <sup>(2)</sup>
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc <sup>(2)</sup>
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc <sup>(2)</sup>
tSA	SSI slave access time			–	–	1.5tcyc + 100	ns
tOR	SSI slave out open time			–	–	1.5tcyc + 100	ns

**NOTES:**

1.  $V_{CC} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V at  $T_{opr} = -40$  to  $85^{\circ}\text{C}$  (J version) /  $-40$  to  $125^{\circ}\text{C}$  (K version), unless otherwise specified.
2.  $1\text{tcyc} = 1/f_1(\text{s})$

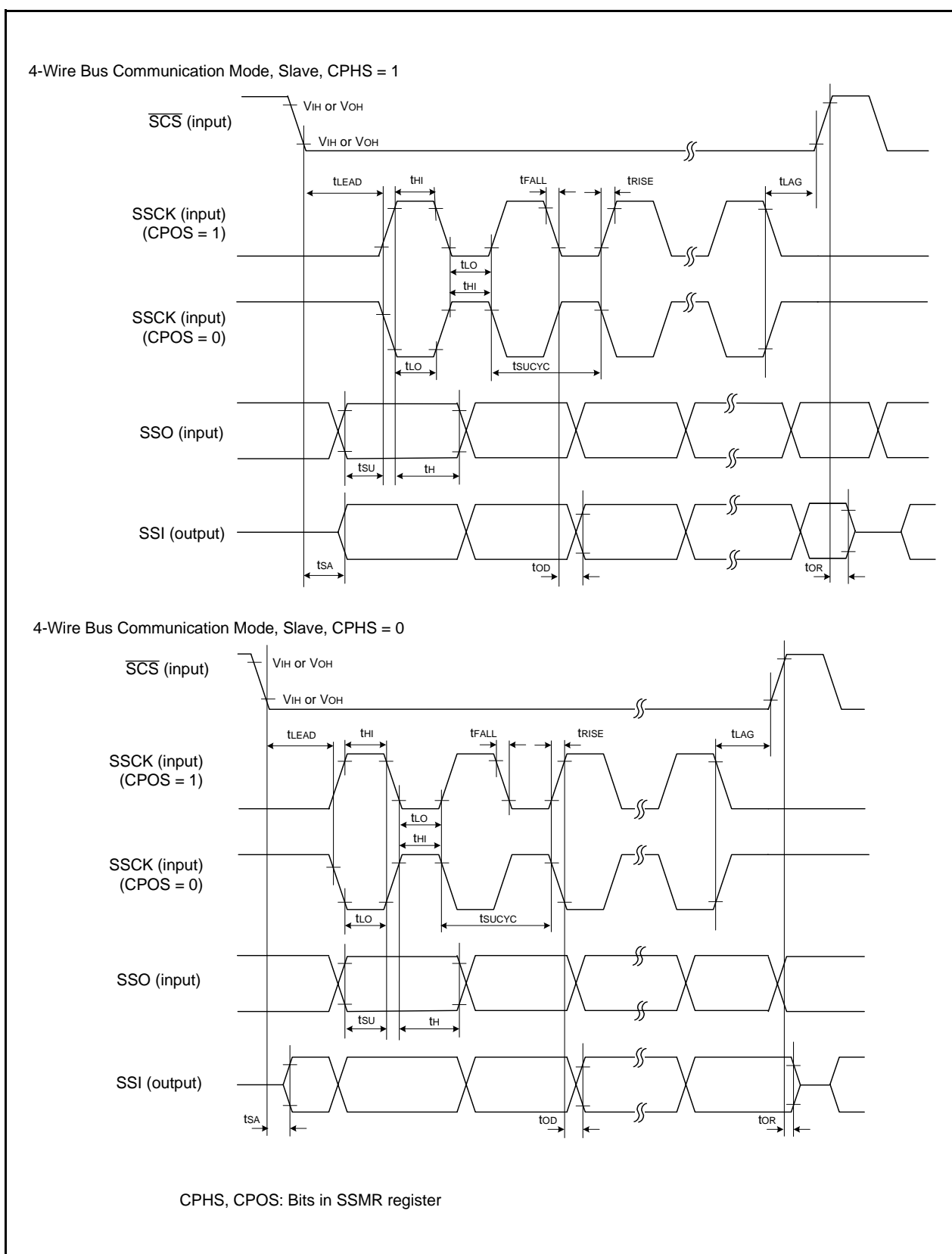
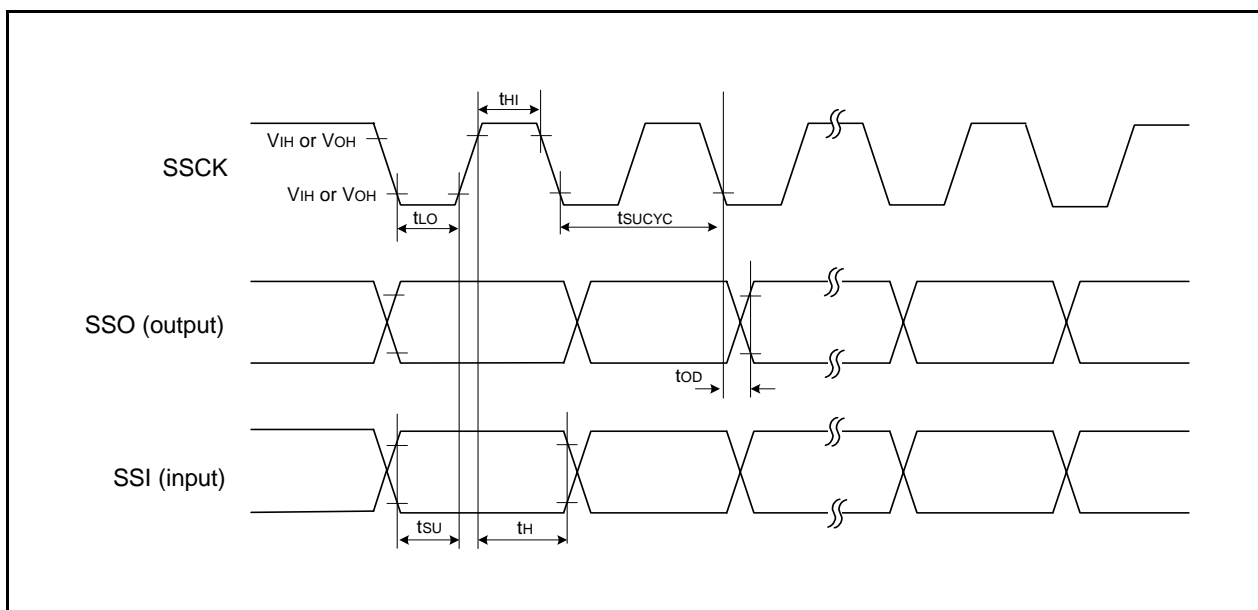


Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)



**Figure 5.25 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)**

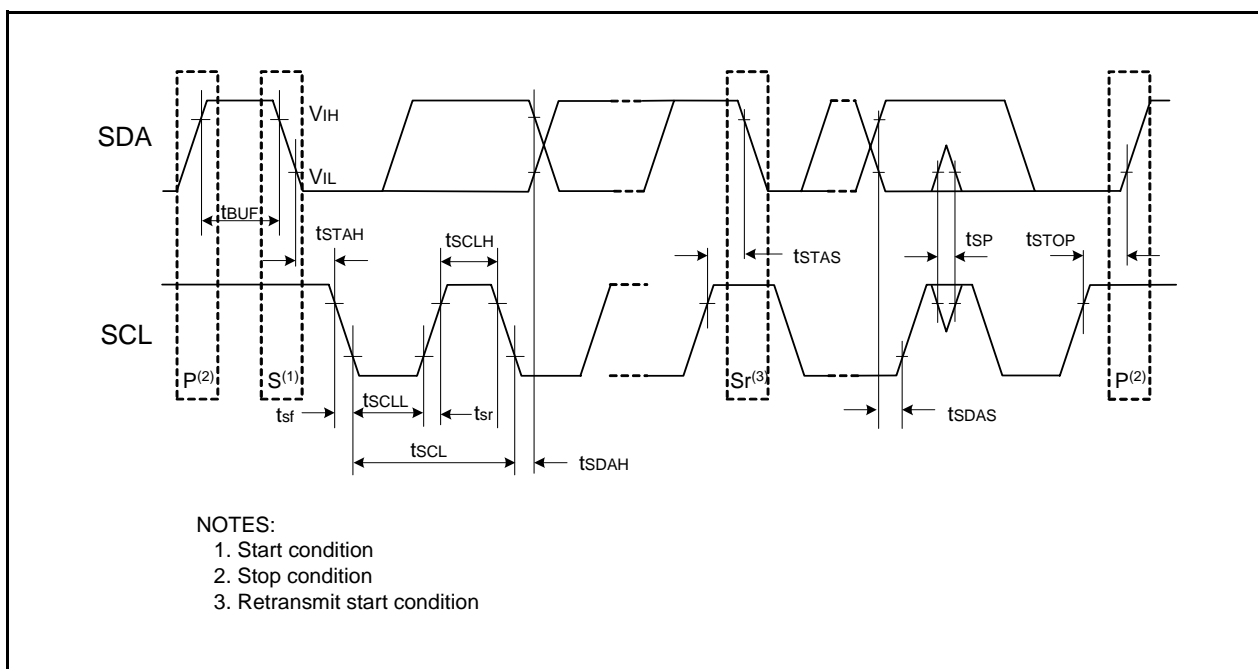


**Table 5.46 Timing Requirements of I<sup>2</sup>C bus Interface<sup>(1)</sup>**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t <sub>SCL</sub>	SCL input cycle time		12t <sub>CYC</sub> + 600 <sup>(2)</sup>	–	–	ns
t <sub>SCLH</sub>	SCL input “H” width		3t <sub>CYC</sub> + 300 <sup>(2)</sup>	–	–	ns
t <sub>SCLL</sub>	SCL input “L” width		5t <sub>CYC</sub> + 500 <sup>(2)</sup>	–	–	ns
t <sub>sf</sub>	SCL, SDA input fall time		–	–	300	ns
t <sub>SP</sub>	SCL, SDA input spike pulse rejection time		–	–	1t <sub>CYC</sub> <sup>(2)</sup>	ns
t <sub>BUF</sub>	SDA input bus-free time		5t <sub>CYC</sub> <sup>(2)</sup>	–	–	ns
t <sub>STAH</sub>	Start condition input hold time		3t <sub>CYC</sub> <sup>(2)</sup>	–	–	ns
t <sub>STAS</sub>	Retransmit start condition input setup time		3t <sub>CYC</sub> <sup>(2)</sup>	–	–	ns
t <sub>STOP</sub>	Stop condition input setup time		3t <sub>CYC</sub> <sup>(2)</sup>	–	–	ns
t <sub>SDAS</sub>	Data input setup time		1t <sub>CYC</sub> + 20 <sup>(2)</sup>	–	–	ns
t <sub>SDAH</sub>	Data input hold time		0	–	–	ns

## NOTES:

1. V<sub>CC</sub> = 2.7 to 5.5 V, V<sub>SS</sub> = 0 V at T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t<sub>CYC</sub> = 1/f<sub>1</sub>(s)

**Figure 5.26 I/O Timing of I<sup>2</sup>C bus Interface**

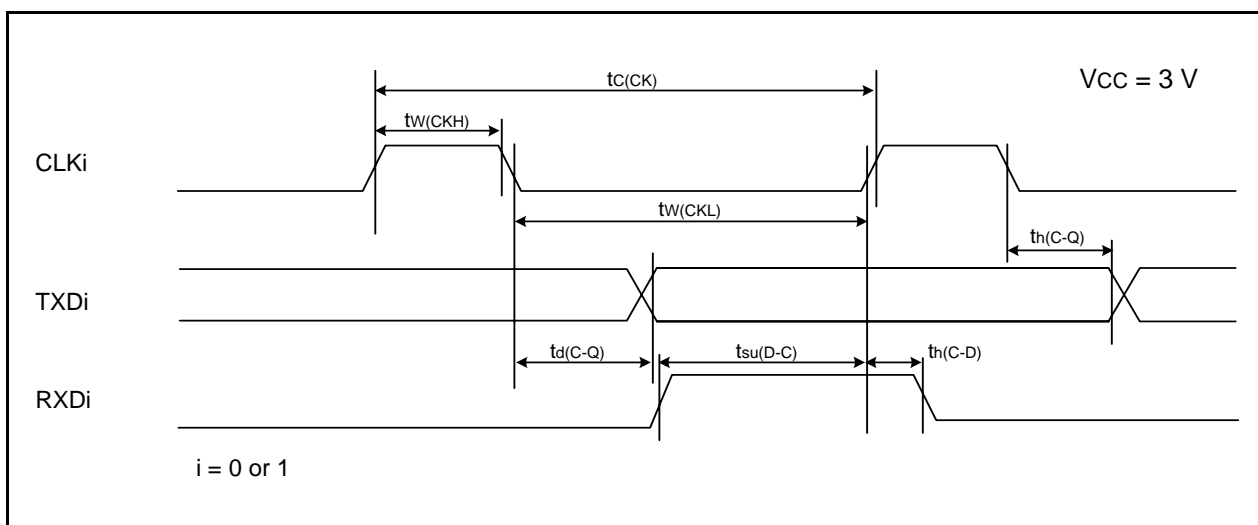
**Table 5.54 Electrical Characteristics (4) [V<sub>CC</sub> = 3 V]**  
**(T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V <sub>SS</sub>	High-speed clock mode	—	6	—	mA
		High-speed on-chip oscillator mode	—	2	—	mA
		High-speed on-chip oscillator mode	—	5	9	mA
		Low-speed on-chip oscillator mode	—	2	—	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Wait mode	—	25	70	μA
		Wait mode	—	23	55	μA
		Stop mode	—	0.7	3.0	μA
		Stop mode	—	1.1	—	μA
		Stop mode	—	3.8	—	μA

**Table 5.57 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

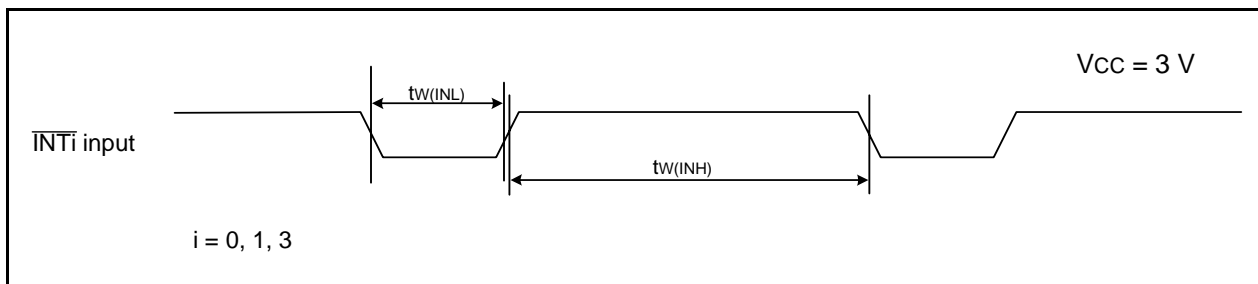
i = 0 or 1

**Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.58 External Interrupt  $\overline{INTi}$  (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 <sup>(2)</sup>	—	ns

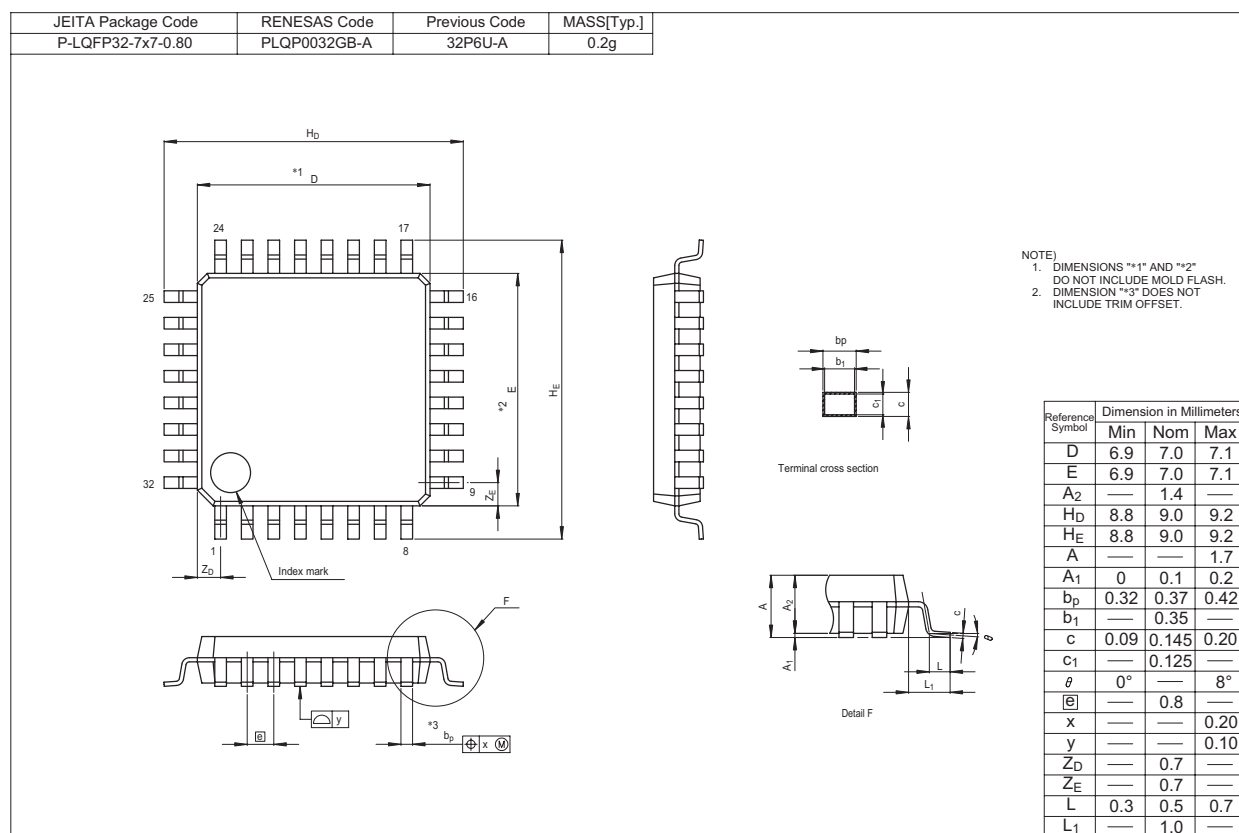
## NOTES:

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.34 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 3 V**

## Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



# REVISION HISTORY

# R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	May 25, 2007	16	Figure 3.2 part number revised
		30	Table 5.10 revised
		53	Table 5.39 NOTE4 added
		55	Table 5.42 revised
1.40a	Jun 14, 2007	5, 7	Table 1.3 and Table 1.4 revised
2.00	Mar 01, 2008	1, 49	1.1, 5.2 "J and K versions are ..." deleted
		5, 7	Table 1.3, Table 1.4 revised
		11	Table 1.6 NOTE3 added
		15, 16	Figure 3.1, Figure 3.2; "Expanded area" deleted
		17	Table 4.1 "002Ch" added
		18	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"
		24, 49	Table 5.2, Table 5.35; NOTE2 revised
2.10	Sep 26, 2008	30	Table 5.10 revised, NOTE4 added
		–	"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E
		26, 51	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		27, 52	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		53	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added
			Table 5.40 revised
		54	Table 5.41 revised
			Figure 5.22 revised

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