1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/26 Group and Table 1.2 outlines the Functions and Specifications for R8C/27 Group.

Table 1.1 Functions and Specifications for R8C/26 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/26 Group**
Peripheral Functions	Ports	I/O ports: 25 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Start-on-reset selectable
	Interrupts	Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation-stopped detector	XIN clock oscillation stop detection function

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register[2]	TREHR	00h
011Bh	Timer RE Day of Week Data Register[2]	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage	Except P1_0 to P1_7, XOUT	IOH = 5 mA		Vcc - 2.0		Vcc	V
			IOH = -200 μA		Vcc - 0.5		Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	IOH = -20 mA	Vcc - 2.0		Vcc	V
			Drive capacity LOW	IOH = -5 mA	Vcc - 2.0		Vcc	V
		XOUT	Drive capacity HIGH	IOH = -1 mA	Vcc - 2.0		Vcc	V
			Drive capacity LOW	IOH = -500 μA	Vcc - 2.0		Vcc	V
VOL	Output “L” voltage	Except P1_0 to P1_7, XOUT	IOL = 5 mA				2.0	V
			IOL = 200 μA				0.45	V
		P1_0 to P1_7	Drive capacity HIGH	IOL = 20 mA			2.0	V
			Drive capacity LOW	IOL = 5 mA			2.0	V
		XOUT	Drive capacity HIGH	IOL = 1 mA			2.0	V
			Drive capacity LOW	IOL = 500 μA			2.0	V
VT+-VT-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5		V
		$\overline{RESET}$			0.1	1.0		V
IIH	Input “H” current		VI = 5 V, Vcc = 5 V				5.0	μA
IIL	Input “L” current		VI = 0 V, Vcc = 5 V				-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN				1.0		MΩ
RfXCIN	Feedback resistance	XCIN				18		MΩ
VRAM	RAM hold voltage		During stop mode		1.8			V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -20 to 85 °C (N version) / -40 to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.22 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage	Except P1_0 to P1_7, XOUT	IOH = -1 mA		Vcc - 0.5		Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	IOH = -5 mA	Vcc - 0.5		Vcc	V
			Drive capacity LOW	IOH = -1 mA	Vcc - 0.5		Vcc	V
		XOUT	Drive capacity HIGH	IOH = -0.1 mA	Vcc - 0.5		Vcc	V
			Drive capacity LOW	IOH = -50 μA	Vcc - 0.5		Vcc	V
VOL	Output “L” voltage	Except P1_0 to P1_7, XOUT	IOL = 1 mA				0.5	V
		P1_0 to P1_7	Drive capacity HIGH	IOL = 5 mA			0.5	V
			Drive capacity LOW	IOL = 1 mA			0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1 mA			0.5	V
			Drive capacity LOW	IOL = 50 μA			0.5	V
VT+-VT-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3		V
		$\overline{RESET}$			0.1	0.4		V
IIH	Input “H” current		VI = 3 V, Vcc = 3 V				4.0	μA
IIL	Input “L” current		VI = 0 V, Vcc = 3 V				-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V		66	160	500	kΩ
RfXIN	Feedback resistance	XIN				3.0		MΩ
RfXCIN	Feedback resistance	XCIN				18		MΩ
VRAM	RAM hold voltage		During stop mode		1.8			V

NOTE:
1. Vcc = 2.7 to 3.3 V at Topr = -20 to 85 °C (N version) / -40 to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P1_0 to P1_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5		Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OH} = -2 mA	Vcc - 0.5		Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5		Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5		Vcc	V
			Drive capacity LOW	I_{OH} = -50 μA	Vcc - 0.5		Vcc	V
V_{OL}	Output “L” voltage	Except P1_0 to P1_7, XOUT	I_{OL} = 1 mA				0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OL} = 2 mA			0.5	V
			Drive capacity LOW	I_{OL} = 1 mA			0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA			0.5	V
			Drive capacity LOW	I_{OL} = 50 μA			0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.05	0.3		V
		$\overline{RESET}$			0.05	0.15		V
I_{IH}	Input “H” current		VI = 2.2 V				4.0	μA
I_{IL}	Input “L” current		VI = 0 V				-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN				5		MΩ
R_{fXCIN}	Feedback resistance	XCIN				35		MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8			V

NOTE:
1. Vcc = 2.2 V at T_{opr} = -20 to 85 °C (N version) / -40 to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 2.2 V]

Table 5.30 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200		ns
$t_{WH(XIN)}$	XIN input “H” width	90		ns
$t_{WL(XIN)}$	XIN input “L” width	90		ns
$t_{c(XCIN)}$	XCIN input cycle time	14		s
$t_{WH(XCIN)}$	XCIN input “H” width	7		s
$t_{WL(XCIN)}$	XCIN input “L” width	7		s

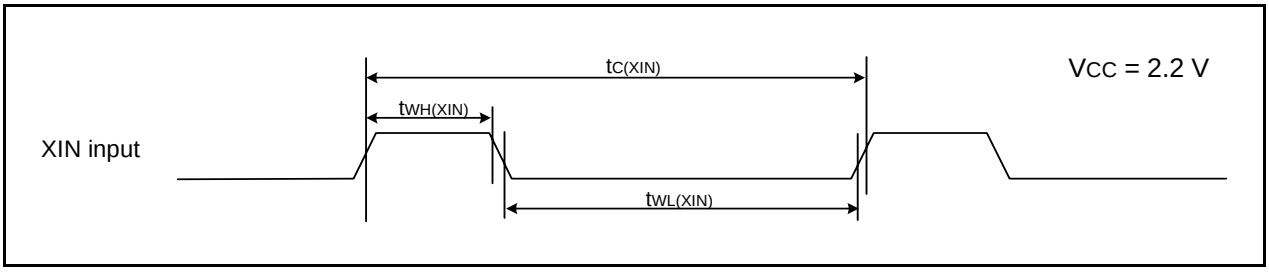

Figure 5.16 XIN Input and XCIN Input Timing Diagram when V_{CC} = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500		ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200		ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200		ns

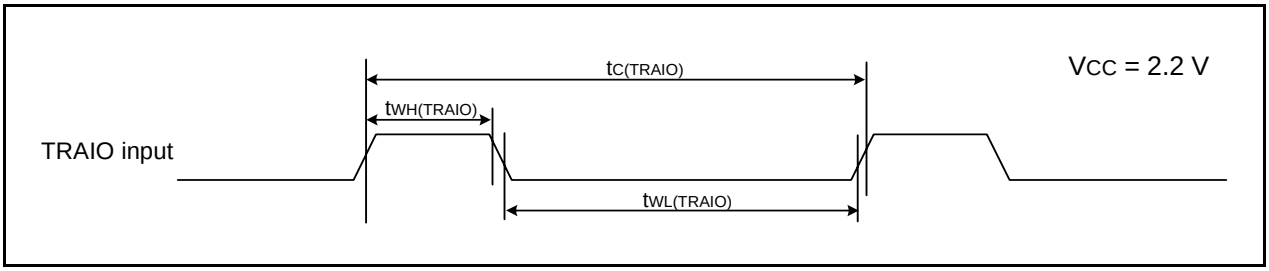

Figure 5.17 TRAIO Input Timing Diagram when V_{CC} = 2.2 V