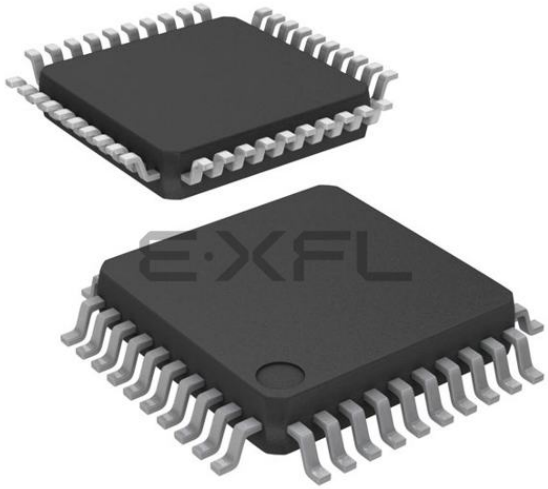
Renesas Electronics America Inc - R5F21276SYFP#V2 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21276syfp-v2

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/26 Group and Table 1.2 outlines the Functions and Specifications for R8C/27 Group.

Table 1.1 Functions and Specifications for R8C/26 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/26 Group**
Peripheral Functions	Ports	I/O ports: 25 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I2C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Start-on-reset selectable
	Interrupts	Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation-stopped detector	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version)
		-40 to 85°C (D, J version)(2), -40 to 125°C (K version)(2)
Package		32-pin molded-plastic LQFP

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
1		P3_5		(TRCIOD)(1)		SSCK	SCL	
2		P3_7		TRAO	RXD1/ (TXD1)(1, 3)	SSO		
3	$\overline{\text{RESET}}$							
4	XOUT/XCOUT(2)	P4_7						
5	VSS/AVSS							
6	XIN/XCIN(2)	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	$\overline{\text{INT0}}$		(RXD1)(1, 3)			
10		P1_7	$\overline{\text{INT1}}$	TRAIO				
11		P3_6	($\overline{\text{INT1}}$)(1)		(TXD1)/ (RXD1)(1, 3)			
12		P3_1		TRBO				
13		P5_4		TRCIOD				
14		P5_3		TRCIOC				
15		P1_6			CLK0	(SSI)(1)		
16		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0			
17		P1_4			TXD0			
18		P1_3	$\overline{\text{KI3}}$	(TRBO)				AN11
19		P1_2	$\overline{\text{KI2}}$	TRCIOB				AN10
20	VRFF	P4_2						
21		P1_1	$\overline{\text{KI1}}$	TRCIOA/ TRCTRG				AN9
22		P1_0	$\overline{\text{KI0}}$					AN8
23		P3_3	$\overline{\text{INT3}}$	TRCCLK		SSI		
24		P3_4		(TRCIOC)(1)		$\overline{\text{SCS}}$	SDA	
25		P0_7						AN0
26		P0_6						AN1
27		P0_5			CLK1			AN2
28		P0_4		TREO				AN3
29		P0_3						AN4
30		P0_2						AN5
31		P0_1						AN6
32		P0_0			(TXD1)(1, 3)			AN7

NOTES:
1. This can be assigned to the pin in parentheses by a program.
2. XCIN, XCOUT can be used only for N or D version.
3. For the combination of using pins TXD1 and RXD1, refer to **Figure 15.7 Registers PINSR1 and PMR** of Hardware Manual (REJ09B0278).

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

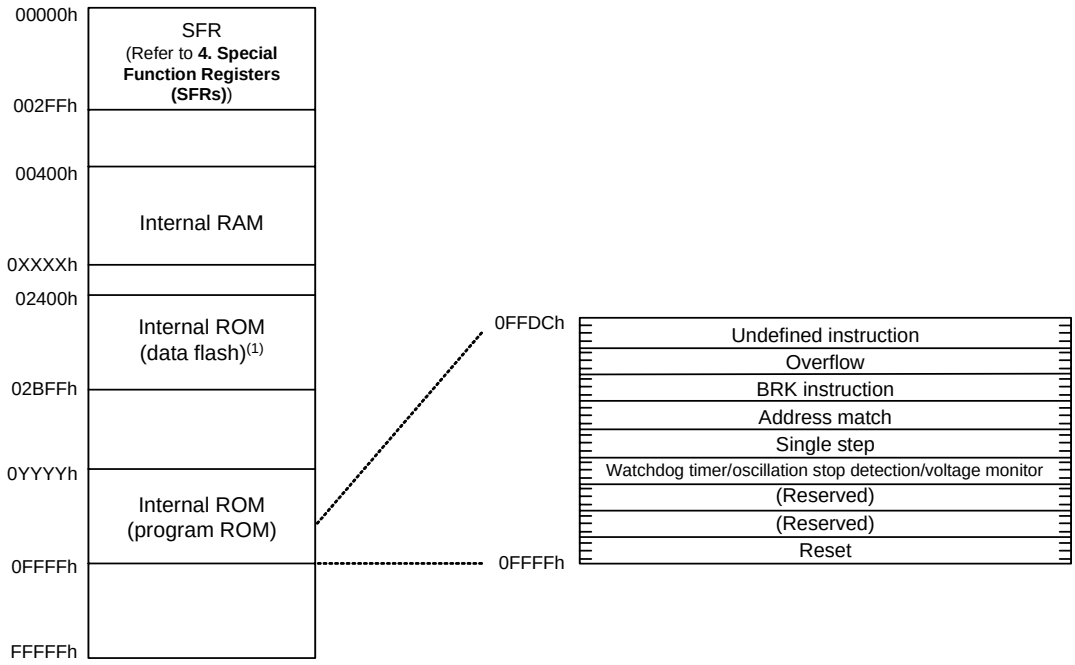
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3.2 R8C/27 Group

Figure 3.2 is a Memory Map of R8C/27 Group. The R8C/27 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21272SNFP, R5F21272SDFP, R5F21272SNXXXFP, R5F21272SDXXXFP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21274SNFP, R5F21274SDFP, R5F21274JFP, R5F21274KFP, R5F21274SNXXXFP, R5F21274SDXXXFP, R5F21274JXXXFP, R5F21274KXXXFP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21275SNFP, R5F21275SDFP, R5F21275SNXXXFP, R5F21275SDXXXFP	24 Kbytes	0A000h	1.5 Kbytes	009FFh
R5F21276SNFP, R5F21276SDFP, R5F21276JFP, R5F21276KFP, R5F21276SNXXXFP, R5F21276SDXXXFP, R5F21276JXXXFP, R5F21276KXXXFP	32 Kbytes	08000h	1.5 Kbytes	009FFh

Figure 3.2 Memory Map of R8C/27 Group

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

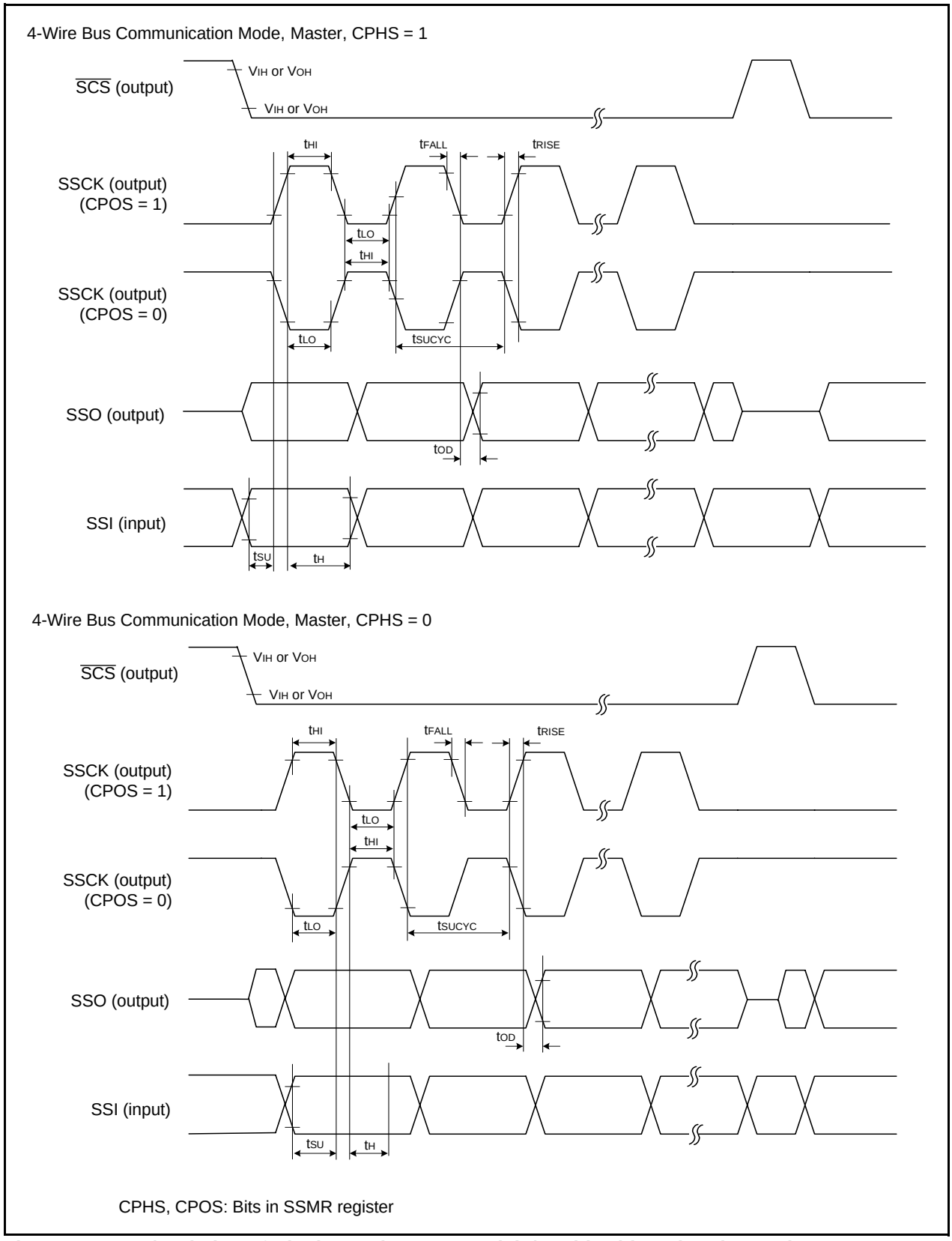


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P1_0 to P1_7, XOUT	I_{OH} = –5 mA		V_{CC} - 2.0	–	V_{CC}	V
			I_{OH} = -200 μA		V_{CC} - 0.5	–	V_{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OH} = -20 mA	V_{CC} - 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -5 mA	V_{CC} - 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} - 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 μA	V_{CC} - 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P1_0 to P1_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

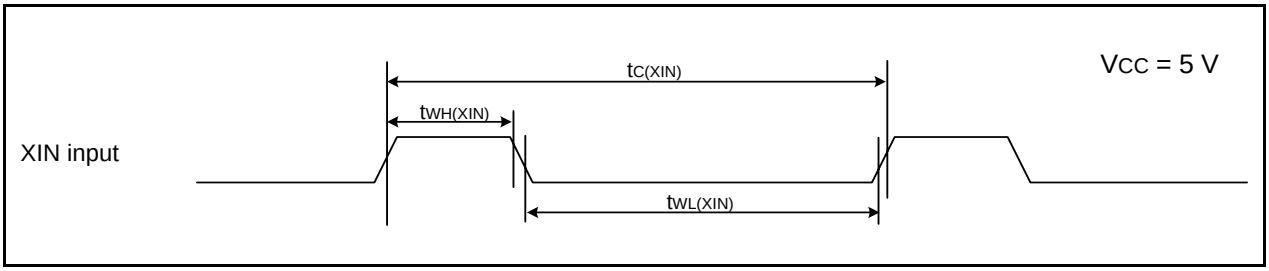


Figure 5.8 XIN Input and XCIN Input Timing Diagram when V_{CC} = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

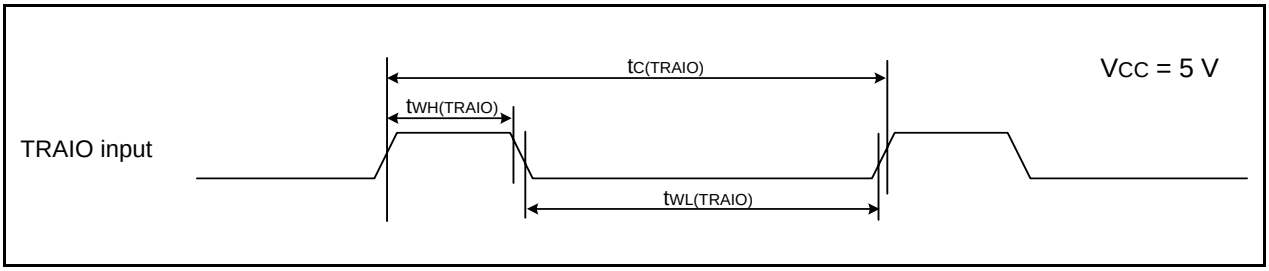


Figure 5.9 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

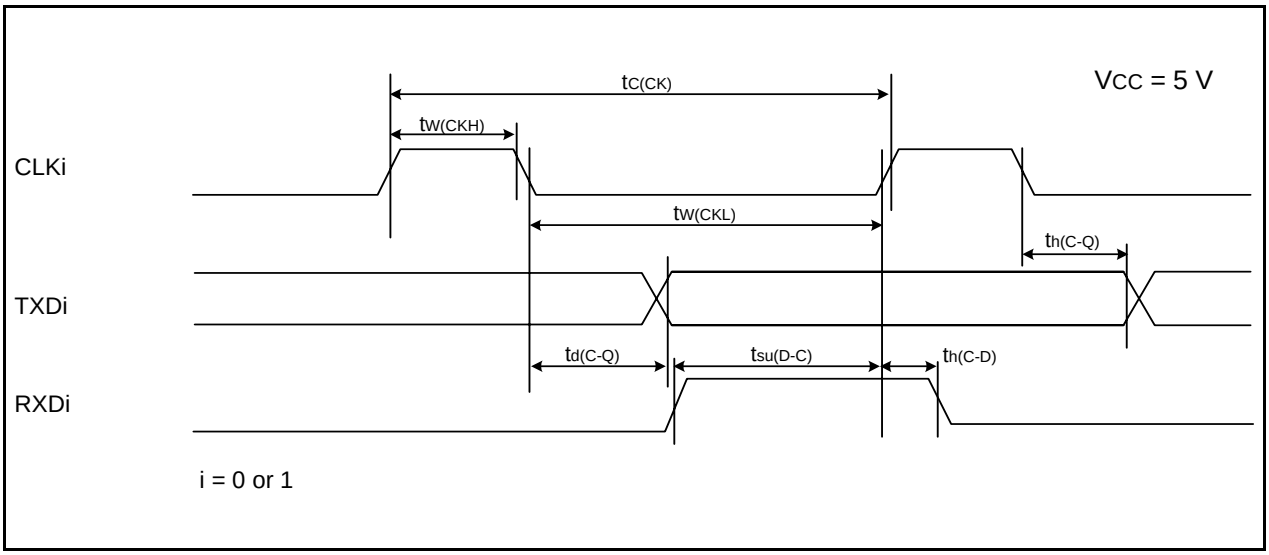


Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V

Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

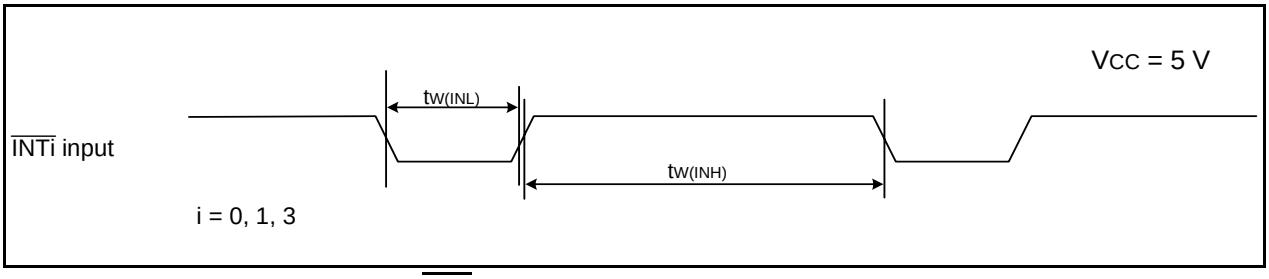


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V_{SS}	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	100	230	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	1.8	–	µA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

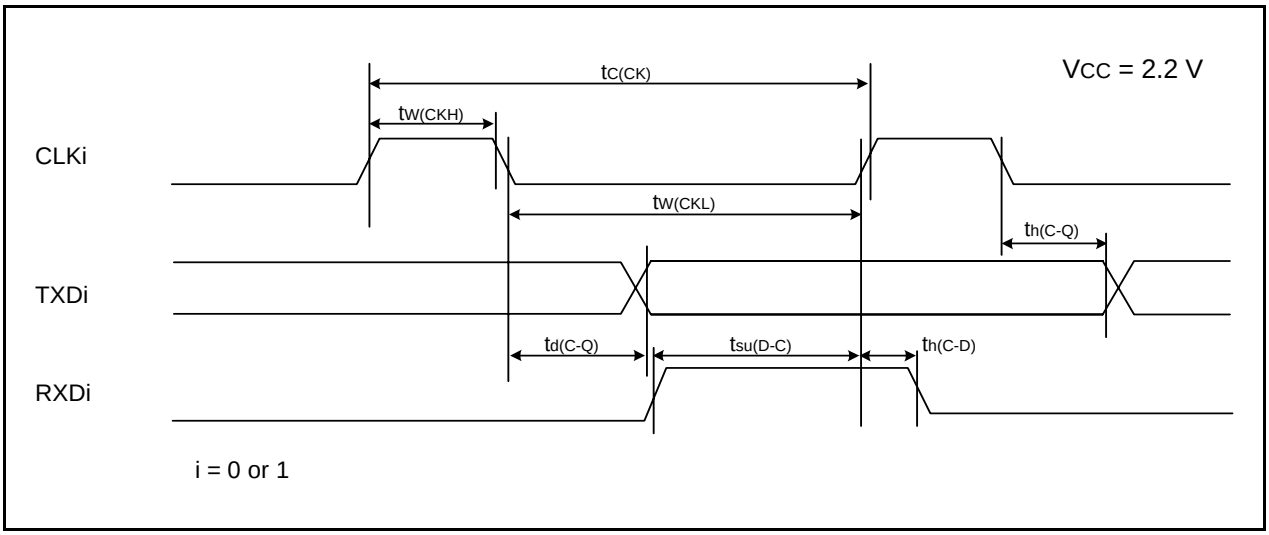


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

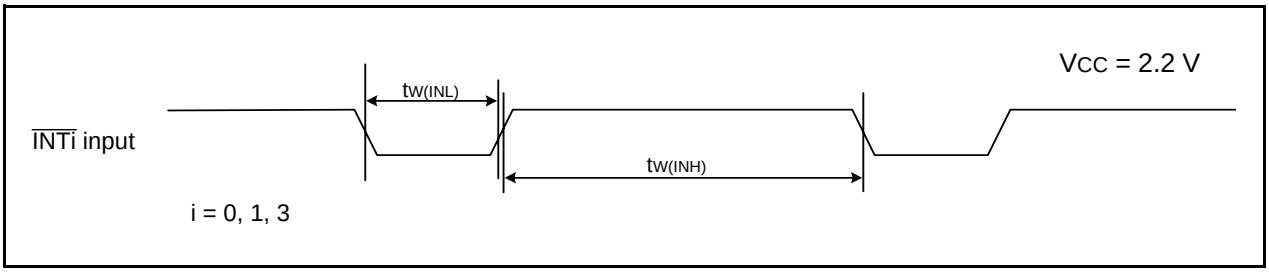


Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage		-0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	-40 °C ≤ T_{opr} ≤ 85 °C	300	mW
		85 °C ≤ T_{opr} ≤ 125 °C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.35 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V (other than K version)	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V (K version)	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V (other than K version)	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V (K version)	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.47 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -5 mA		V_{CC} - 2.0	–	V_{CC}	V
			I_{OH} = -200 μA		V_{CC} - 0.3	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} - 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 μA	V_{CC} - 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5V		–	–	-5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.48 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	4.0	–	µA

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.49 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

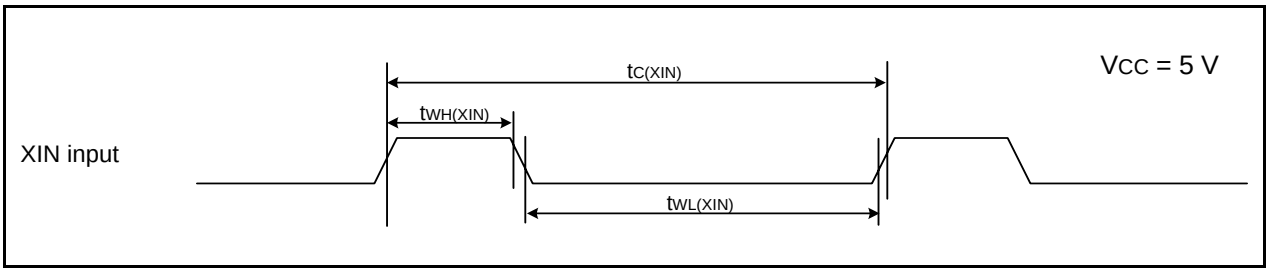


Figure 5.27 XIN Input Timing Diagram when V_{CC} = 5 V

Table 5.50 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

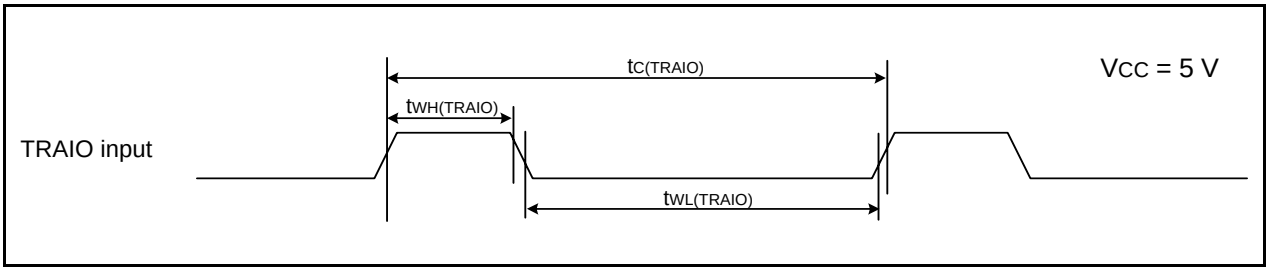


Figure 5.28 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.51 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

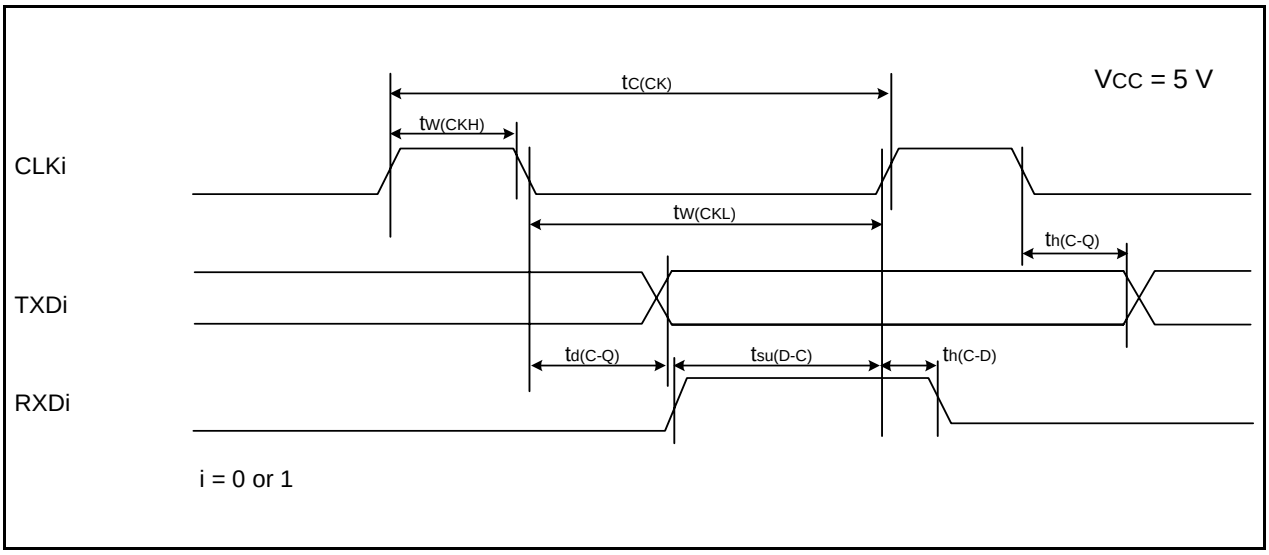


Figure 5.29 Serial Interface Timing Diagram when VCC = 5 V

Table 5.52 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

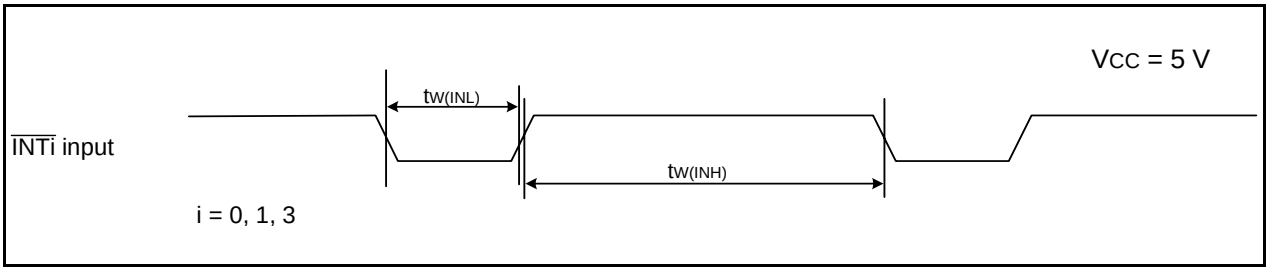


Figure 5.30 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 5.55 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

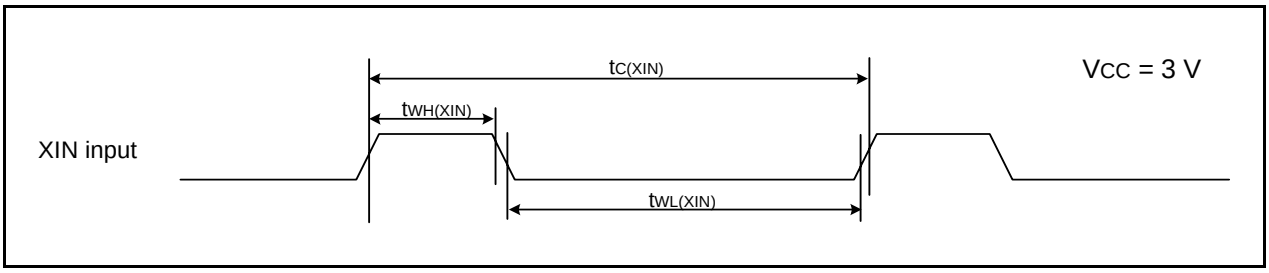


Figure 5.31 XIN Input Timing Diagram when V_{CC} = 3 V

Table 5.56 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

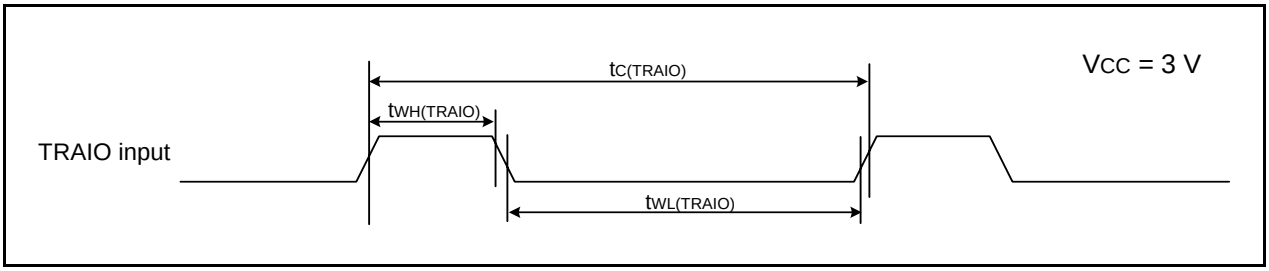


Figure 5.32 TRAIO Input Timing Diagram when V_{CC} = 3 V

REVISION HISTORY	R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 08, 2006	27	Table 5.9, Figure 5.3 revised and Table 5.10 deleted
		28	Table 5.10, Table 5.11 revised
		34	Table 5.15 revised
		35	Table 5.16 revised
		36	Table 5.17 revised
		39	Table 5.22 revised
		40	Table 5.23 revised
		44	Table 5.29 revised
		47	Package Dimensions; “Diagrams showing the latest...website.” added
1.10	Nov 29, 2006	All pages	“J, K version” added
		1	1 “J and K versions are under development...notice.” added 1.1 revised
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 NOTE3 added
		5	Table 1.3, Figure 1.2 revised
		6	Table 1.4, Figure 1.3 revised
		7	Figure 1.4 NOTE3 added
		8	Table 1.5 revised
		9	Table 1.6 NOTE2 added
		13	Figure 3.1 revised
		14	Figure 3.2 revised
		15	Table 4.1; “0000h to 003Fh” → “0000h to 002Fh” revised • NOTE3 added
		16	Table 4.2; “0040h to 007Fh” → “0030h to 007Fh” revised • 0032h, 0036h: “After reset” is revised • 0038h: NOTE revised • NOTES 2, 5, 6 revised and NOTE 7, 8 added
		19	Table 4.5 NOTE2 added
		28	Table 5.10 revised
		48 to 66	5.2 J, K Version added
1.20	Jan 17, 2007	18	Table 4.4 NOTE2 added
1.30	May 25, 2007	2	Table 1.1 revised
		3	Table 1.2 revised
		5	Table 1.3 revised
		6	Figure 1.2 revised
		7	Table 1.4 revised
		8	Figure 1.3 revised
		9	Figure 1.4 NOTE4 added
		15	Figure 3.1 part number revised

REVISION HISTORY	R8C/26 Group, R8C/27 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	May 25, 2007	16	Figure 3.2 part number revised
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		5, 7	Table 1.3, Table 1.4 revised
		11	Table 1.6 NOTE3 added
		15, 16	Figure 3.1, Figure 3.2; “Expanded area” deleted
		17	Table 4.1 “002Ch” added
		18	Table 4.2 “0036h”; J, K version “0100X000b” → “0100X001b”
		24, 49	Table 5.2, Table 5.35; NOTE2 revised
		30	Table 5.10 revised, NOTE4 added
2.10	Sep 26, 2008	–	“RENESAS TECHNICAL UP DATE” reflected: TN-16C-A172A/E
		26, 51	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		27, 52	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		53	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added Table 5.40 revised
		54	Table 5.41 revised Figure 5.22 revised