Infineon Technologies - C167CRL33MHAKXQLA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	33MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167crl33mhakxqla1

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2 General Device Information

2.1 Introduction

The C167CR derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 16.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

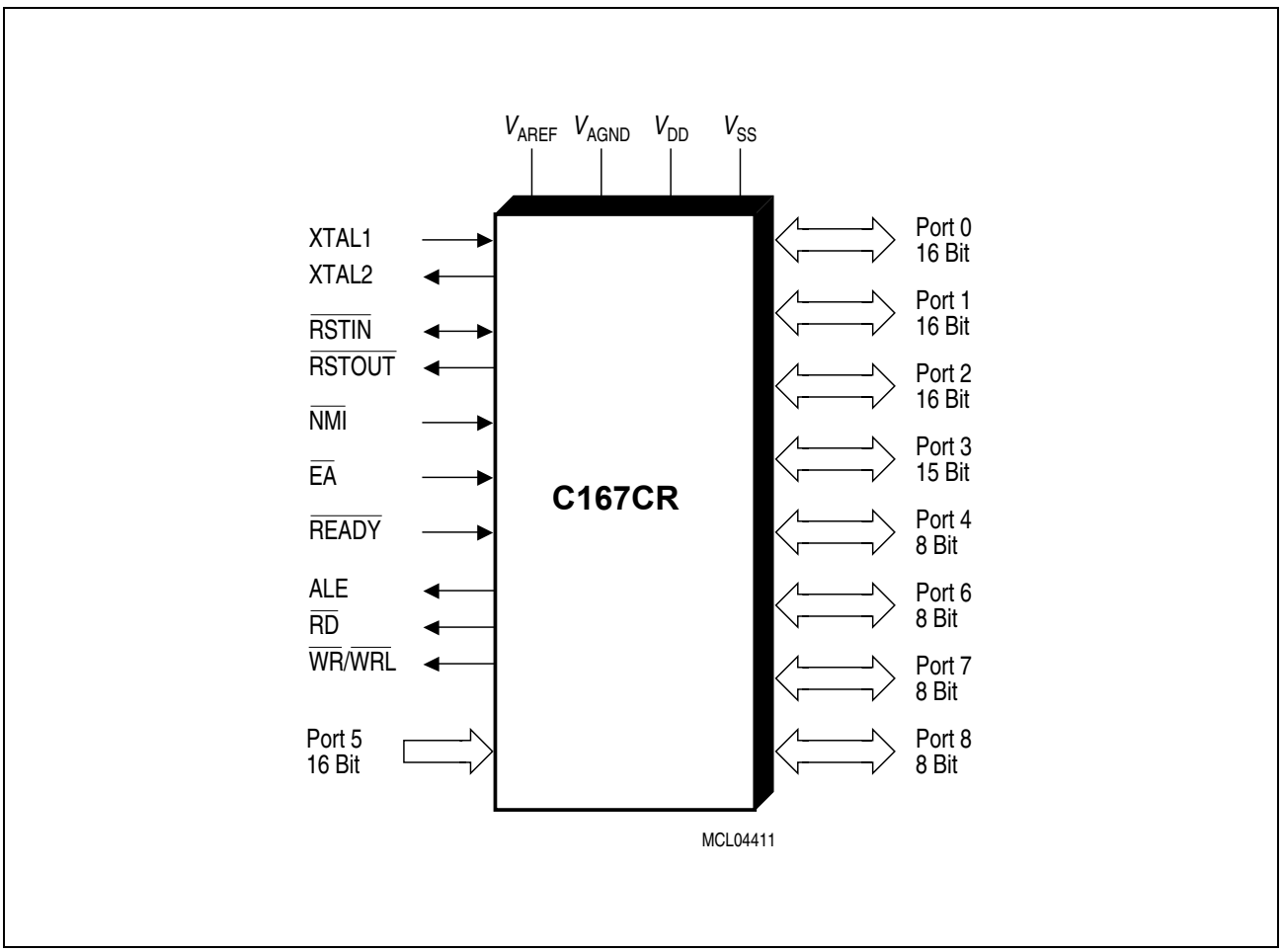


Figure 1 Logic Symbol

Table 2 Pin Definitions and Functions P-MQFP-144-8

Symbol	Pin No.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	7	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	$\overline{BREQ}$ Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	9	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	11	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	12	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0
P0L.0-7	100-107		
P0H.0-7	108, 111-117		
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
P1L.0-7	118-125		
P1H.0-7	128-135		
P1H.4	132	I	CC24IO CAPCOM2: CC24 Capture Input
P1H.5	133	I	CC25IO CAPCOM2: CC25 Capture Input
P1H.6	134	I	CC26IO CAPCOM2: CC26 Capture Input
P1H.7	135	I	CC27IO CAPCOM2: CC27 Capture Input
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	B10	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	A10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	D9	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	C9	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	B9	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	A9	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	D8	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	C8	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	A13	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	B12	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	D10	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	C11	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	A12	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	B11	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	C10	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	A11	O	$\overline{BREQ}$ Bus Request Output
$\overline{NMI}$	C14	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{NMI}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{NMI}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{NMI}$ should be pulled high externally.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{EA}$	M9	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
$\overline{WR}$/ $\overline{WRL}$	N9	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	P9	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	P10	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	P6	O	A16 Least Significant Segment Address Line
P4.1	M6	O	A17 Segment Address Line
P4.2	L6	O	A18 Segment Address Line
P4.3	N7	O	A19 Segment Address Line
P4.4	P7	O	A20 Segment Address Line
P4.5	M7	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	L7	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	N8	O	A23 Most Significant Segment Address Line

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
OWE (V_{PP})	N6	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	M1	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	K3	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	L2	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	M2	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	N1	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	P2	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	M3	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	N2	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	N3	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	P3	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	N4	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	M4	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	L4	O	$\overline{BHE}$	External Memory High Byte Enable Signal,
		O	$\overline{WRH}$	External Memory High Byte Write Strobe
P3.13	P4	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	N5	O	CLKOUT	System Clock Output (= CPU Clock)

Note: When the on-chip CAN Module is to be used the segment address output on Port 4 must be limited to 4 bits (i.e. A19 … A16) in order to enable the alternate function of the CAN interface pins. CS lines can be used to increase the total amount of addressable external memory.

The C167CR also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	$00'0000_H$	00_H	III
• Software Reset		RESET	$00'0000_H$	00_H	III
• W-dog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
• Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
• Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved	–	–	$[2C_H - 3C_H]$	$[0B_H - 0F_H]$	–
Software Traps • TRAP Instruction	–	–	Any $[00'0000_H - 00'01FC_H]$ in steps of 4_H	Any $[00_H - 7F_H]$	Current CPU Priority

3.7 General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.8 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

3.15 Special Function Registers Overview

The following table lists all SFRs which are implemented in the C167CR in alphabetical order.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Note: Registers within device specific interface modules (CAN) are only present in the corresponding device, of course.

Table 8 C167CR Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	–	CAN1 Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	–	CAN1 Control / Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	–	CAN1 Global Mask Short	$UFUU_H$

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CR and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C167CR will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C167CR.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	0.2 V_{DD} - 0.1	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	0.3 V_{DD}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	2.0	V	–
Input high voltage (TTL, all except RSTIN and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage RSTIN (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	–	mV	Series resistance = 0 Ω
Output low voltage (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, CLKOUT, RSTOUT, RSTIN[2)])	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL} = 1.6 mA

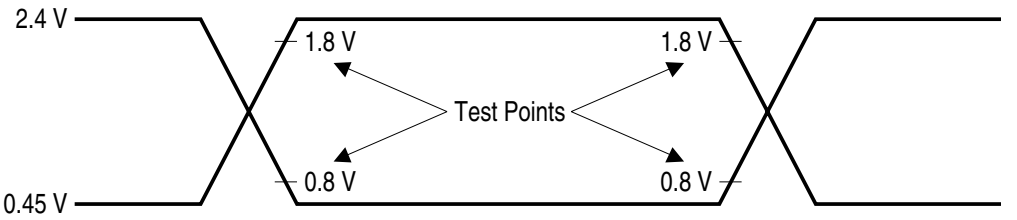
Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \text{ (DC = duty cycle)} \quad (2)$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

4.4.3 Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.45 V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

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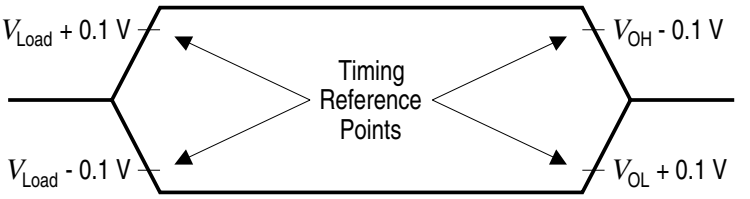
Figure 13 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

MCA00763

Figure 14 Float Waveforms

4.4.4 External Bus Timing

Table 17 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	30[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter.
For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for f_{CPU} > 25 MHz).
For longer periods the relative deviation decreases (see PLL deviation formula).

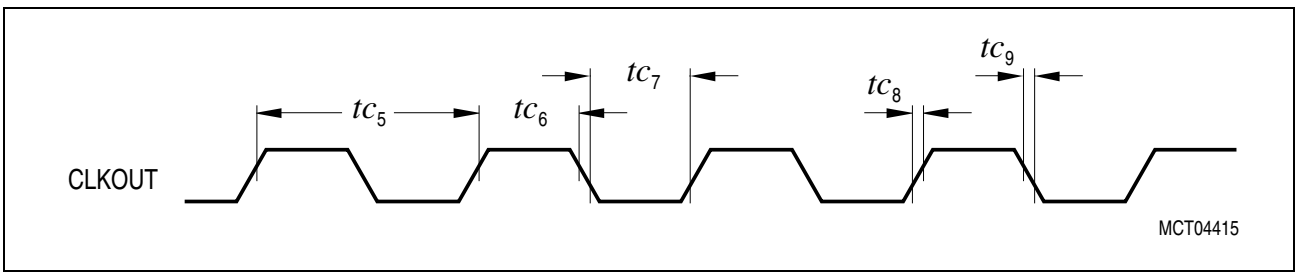


Figure 15 CLKOUT Signal Timing

Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

Table 18 Variable Memory Cycles

Bus Cycle Type	Bus Cycle Duration	Unit	25/33 MHz, 0 Waitstates
Demultiplexed bus cycle with normal ALE	4 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	80 ns/60.6 ns
Demultiplexed bus cycle with extended ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with normal ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with extended ALE	8 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	160 ns/121.2 ns

Table 19 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Output delay from CLKOUT falling edge Valid for: address, BHE, early CS, write data out, ALE	tc_{10}	CC	-2	11	ns
Output delay from CLKOUT rising edge Valid for: latched CS, ALE low	tc_{11}	CC	-2	6	ns
Output delay from CLKOUT rising edge Valid for: WR low (no RW delay), RD low (no RW delay)	tc_{12}	CC	-2	8	ns
Output delay from CLKOUT falling edge Valid for: RD/WR low (with RW delay), RD high (with RW delay)	tc_{13}	CC	-2	6	ns
Input setup time to CLKOUT falling edge Valid for: read data in	tc_{14}	SR	14	–	ns
Input hold time after CLKOUT falling edge Valid for: read data in[1)]	tc_{15}	SR	0	–	ns
Output hold time after CLKOUT falling edge Valid for: address, BHE, early CS[2)]	tc_{17}	CC	-2	6	ns
Output hold time after CLKOUT edge[3)] Valid for: write data out	tc_{18}	CC	-2	–	ns
Output delay from CLKOUT falling edge Valid for: WR high	tc_{19}	CC	-2	4	ns
Turn off delay after CLKOUT edge[3)] Valid for: write data out	tc_{20}	CC	–	7	ns
Turn on delay after CLKOUT falling edge[3)] Valid for: write data out	tc_{21}	CC	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore the read data may be removed immediately after the rising edge of RD. Address changes before the end of RD have also no impact on (demultiplexed) read cycles.

2) Due to comparable propagation delays (at comparable capacitive loads) the address does not change before WR goes high. The minimum output delay (tc_{17min}) is therefore the actual value of tc_{19}.

3) Not subject to production test - verified by design/characterization.

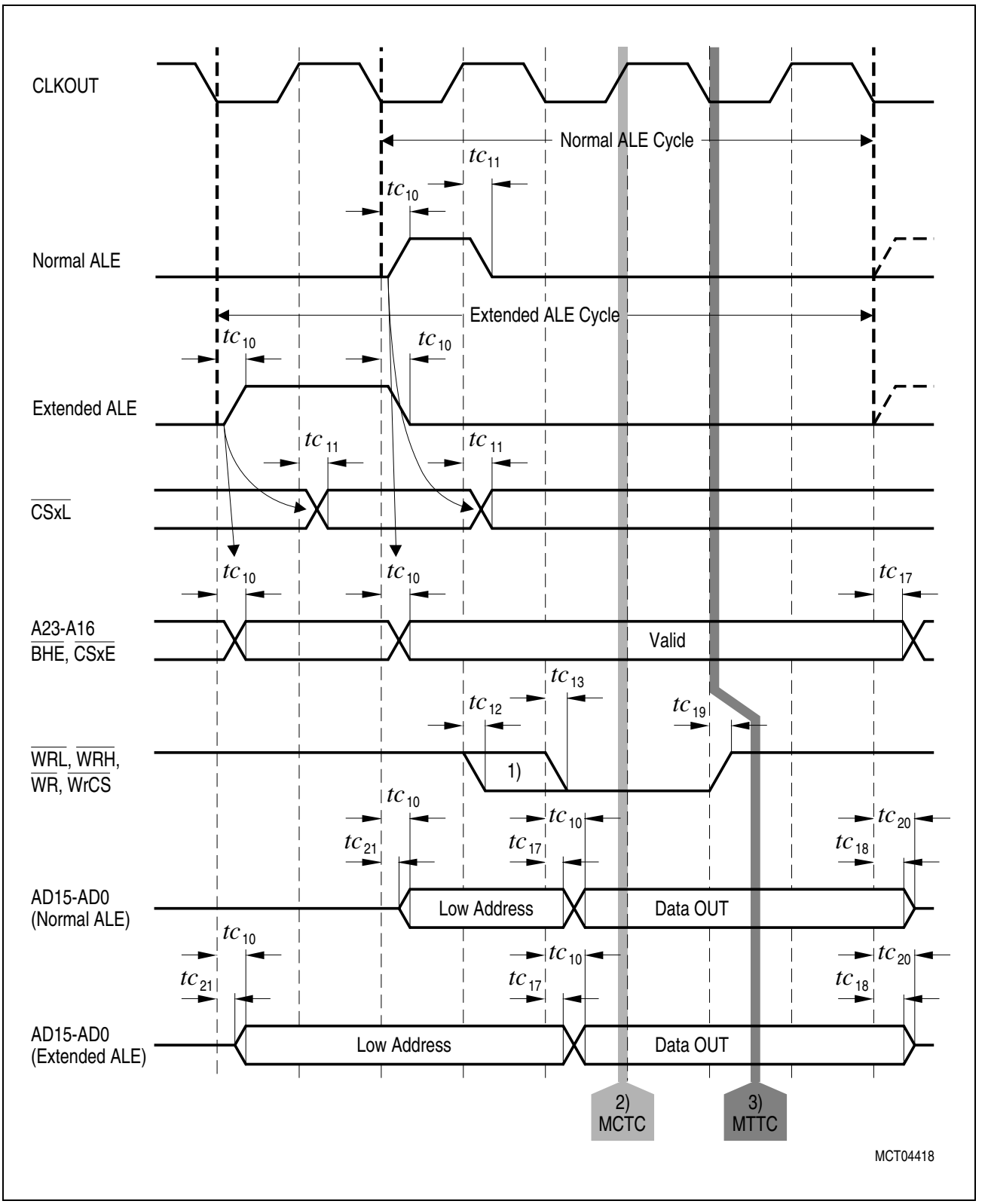


Figure 18 Multiplexed Bus, Write Access

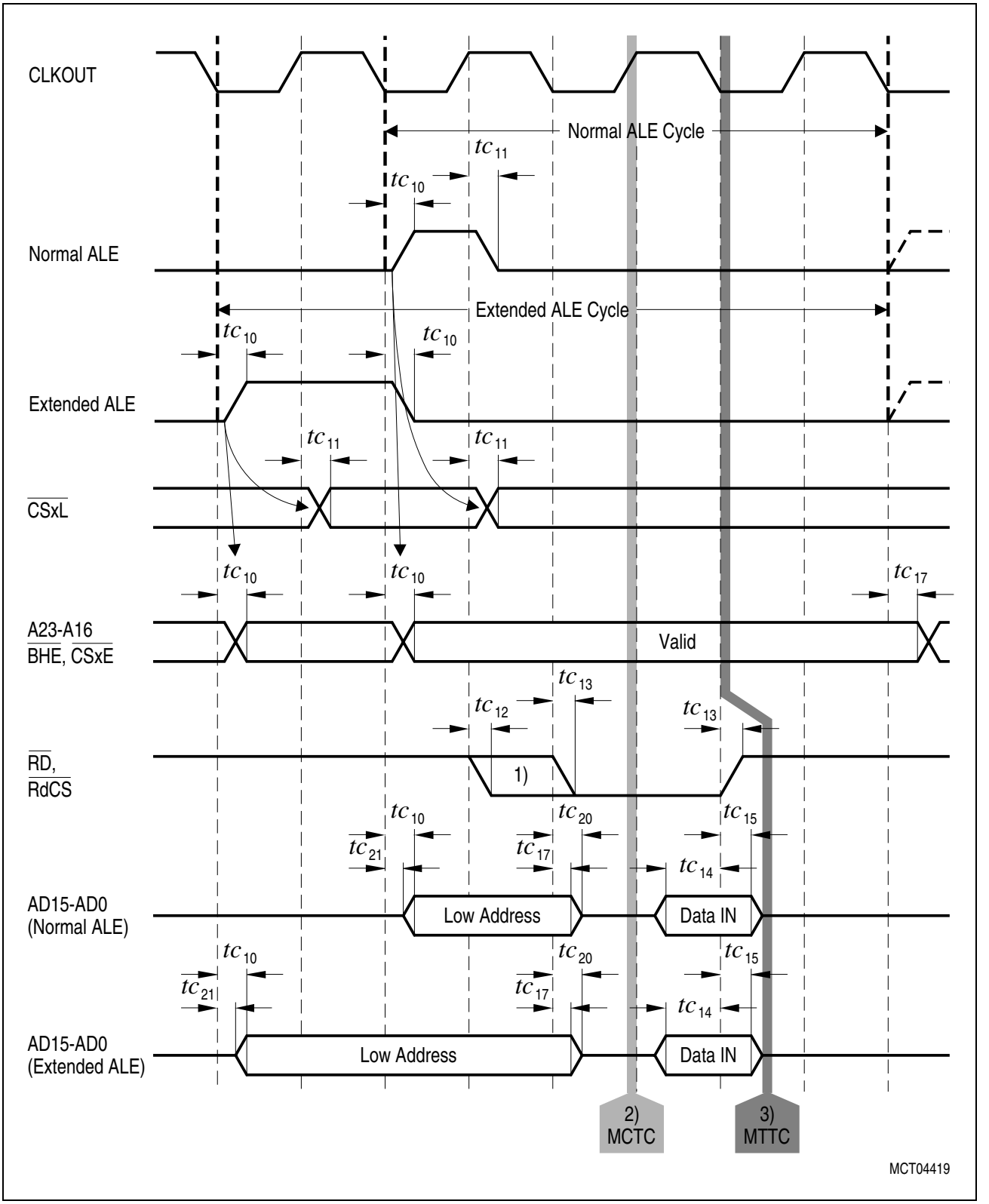


Figure 19 Multiplexed Bus, Read Access

External XRAM Access

If XPER-Share mode is enabled the on-chip XRAM of the C167CR can be accessed (during hold states) by an external master like an asynchronous SRAM.

Table 22 XRAM Access Timing (Operating Conditions apply)[1)]

Parameter		Symbol		Limits		Unit
				Min.	Max.	
Address setup time before $\overline{RD}$/$\overline{WR}$ falling edge		t_{40}	SR	4	–	ns
Address hold time after $\overline{RD}$/$\overline{WR}$ rising edge		t_{41}	SR	0	–	ns
Data turn on delay after $\overline{RD}$ falling edge	Read	t_{42}	CC	1	–	ns
Data output valid delay after address latched	Read	t_{43}	CC	–	40	ns
Data turn off delay after $\overline{RD}$ rising edge	Read	t_{44}	CC	1	14	ns
Write data setup time before $\overline{WR}$ rising edge	Write	t_{45}	SR	10	–	ns
Write data hold time after $\overline{WR}$ rising edge	Write	t_{46}	SR	2	–	ns
$\overline{WR}$ pulse width	Write	t_{47}	SR	20	–	ns
$\overline{WR}$ signal recovery time	Write	t_{48}	SR	t_{40}	–	ns

1) The minimum access cycle time is 60 ns.

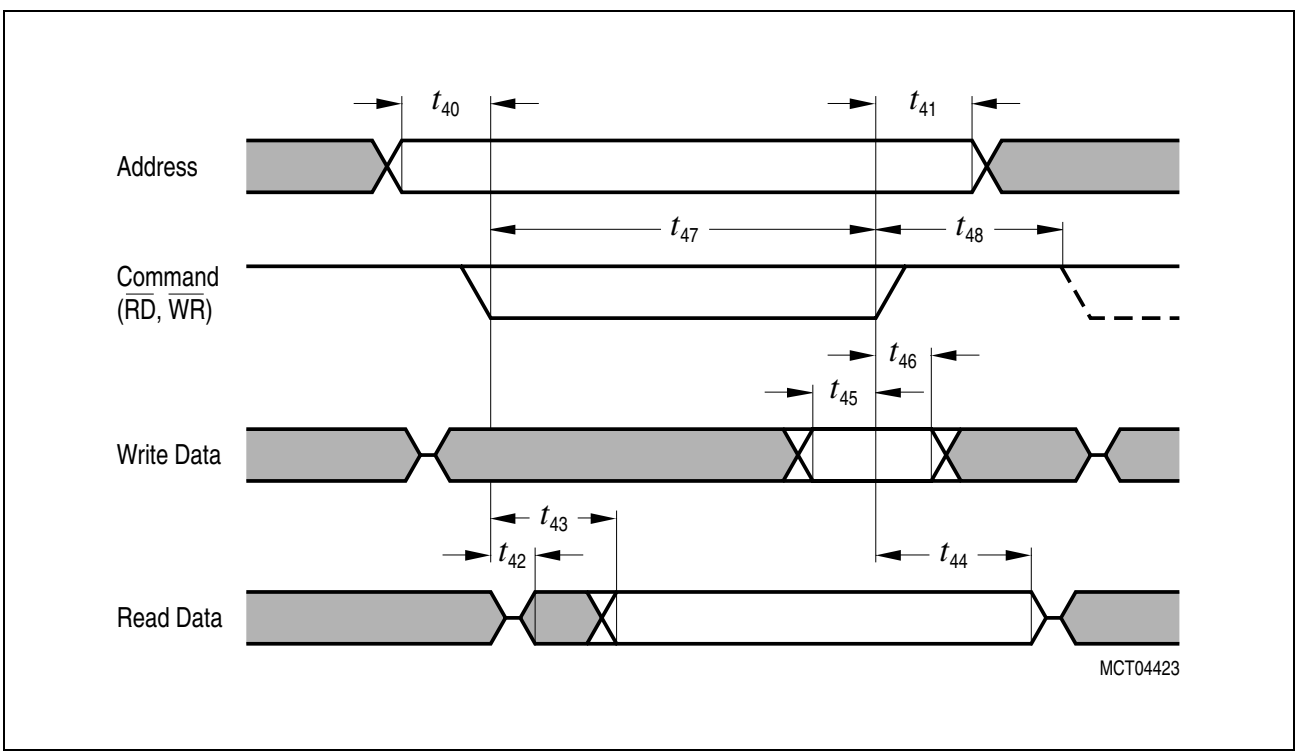


Figure 23 External Access to the XRAM