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Details

Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	33MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	113
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167crl33mhakxuma2

General Device Information
Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P2		I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:
P2.0	F3	I/O	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	F2	I/O	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	F4	I/O	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	G4	I/O	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	G3	I/O	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	G2	I/O	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	G1	I/O	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	H1	I/O	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	H4	I/O	CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, I EX0IN Fast External Interrupt 0 Input
P2.9	J1	I/O	CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, I EX1IN Fast External Interrupt 1 Input
P2.10	J2	I/O	CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., I EX2IN Fast External Interrupt 2 Input
P2.11	J4	I/O	CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., I EX3IN Fast External Interrupt 3 Input
P2.12	J3	I/O	CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., I EX4IN Fast External Interrupt 4 Input
P2.13	K1	I/O	CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., I EX5IN Fast External Interrupt 5 Input
P2.14	K2	I/O	CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., I EX6IN Fast External Interrupt 6 Input
P2.15	L1	I/O	CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., I EX7IN Fast External Interrupt 7 Input, I T7IN CAPCOM2: Timer T7 Count Input
V_{AREF}	B2	—	Reference voltage for the A/D converter.
V_{AGND}	C2	—	Reference ground for the A/D converter.

3.1 Memory Organization

The memory space of the C167CR is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 Mbytes. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have additionally been made directly bit-addressable.

The C167CR incorporates 128/32 Kbytes (depending on the derivative) of on-chip mask-programmable ROM for code or constant data. The lower 32 Kbytes of the on-chip ROM can be mapped either to segment 0 or segment 1.

2 Kbytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

2 Kbytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bit-addressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external RAM and/or ROM can be connected to the microcontroller.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{\text{CS}}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C167CR offers the possibility to switch the $\overline{\text{CS}}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{\text{CS}}$ signals are directly generated from the address. The unlatched $\overline{\text{CS}}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular 'Ready' function.

A $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit $\overline{\text{HLDEN}}$ in register PSW. After setting $\overline{\text{HLDEN}}$ once, pins P6.7 ... P6.5 ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{\text{HLDA}}$ pin is an output. By setting bit DP6.7 to '1' the Slave Mode is selected where pin $\overline{\text{HLDA}}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 Mbytes of external memory space, this address space can be restricted to 1 Mbyte, 256 Kbyte, or to 64 Kbyte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 Mbytes is used.

Functional Description
Table 4 C167CR Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040 _H	10 _H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044 _H	11 _H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048 _H	12 _H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004C _H	13 _H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050 _H	14 _H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054 _H	15 _H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058 _H	16 _H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005C _H	17 _H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060 _H	18 _H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064 _H	19 _H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068 _H	1A _H
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006C _H	1B _H
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070 _H	1C _H
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074 _H	1D _H
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078 _H	1E _H
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007C _H	1F _H
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0 _H	30 _H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4 _H	31 _H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8 _H	32 _H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CC _H	33 _H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0 _H	34 _H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4 _H	35 _H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8 _H	36 _H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DC _H	37 _H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0 _H	38 _H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4 _H	39 _H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8 _H	3A _H
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00EC _H	3B _H
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00E0 _H	3C _H
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110 _H	44 _H

3.7 General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.8 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

Functional Description

3.15 Special Function Registers Overview

The following table lists all SFRs which are implemented in the C167CR in alphabetical order.

Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter “E” in column “Physical Address”. Registers within on-chip X-peripherals are marked with the letter “X” in column “Physical Address”.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Note: Registers within device specific interface modules (CAN) are only present in the corresponding device, of course.

Table 8 C167CR Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	FF98 _H	CC _H	A/D Converter End of Conversion Interrupt Control Register	0000 _H
ADCON b	FFA0 _H	D0 _H	A/D Converter Control Register	0000 _H
ADDAT	FEA0 _H	50 _H	A/D Converter Result Register	0000 _H
ADDAT2	F0A0 _H E	50 _H	A/D Converter 2 Result Register	0000 _H
ADDRSEL1	FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2	FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3	FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4	FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC b	FF9A _H	CD _H	A/D Converter Overrun Error Interrupt Control Register	0000 _H
BUSCON0 b	FF0C _H	86 _H	Bus Configuration Register 0	0XX0 _H
BUSCON1 b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2 b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3 b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4 b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
C1BTR	EF04 _H X	–	CAN1 Bit Timing Register	UUUU _H
C1CSR	EF00 _H X	–	CAN1 Control / Status Register	XX01 _H
C1GMS	EF06 _H X	–	CAN1 Global Mask Short	UFUU _H

Functional Description
Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
CC19IC	b	F166 _H	E B3 _H	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000 _H
CC1IC	b	FF7A _H	BD _H	CAPCOM Reg. 1 Interrupt Ctrl. Reg.	0000 _H
CC2		FE84 _H	42 _H	CAPCOM Register 2	0000 _H
CC20		FE68 _H	34 _H	CAPCOM Register 20	0000 _H
CC20IC	b	F168 _H	E B4 _H	CAPCOM Reg. 20 Interrupt Ctrl. Reg.	0000 _H
CC21		FE6A _H	35 _H	CAPCOM Register 21	0000 _H
CC21IC	b	F16A _H	E B5 _H	CAPCOM Reg. 21 Interrupt Ctrl. Reg.	0000 _H
CC22		FE6C _H	36 _H	CAPCOM Register 22	0000 _H
CC22IC	b	F16C _H	E B6 _H	CAPCOM Reg. 22 Interrupt Ctrl. Reg.	0000 _H
CC23		FE6E _H	37 _H	CAPCOM Register 23	0000 _H
CC23IC	b	F16E _H	E B7 _H	CAPCOM Reg. 23 Interrupt Ctrl. Reg.	0000 _H
CC24		FE70 _H	38 _H	CAPCOM Register 24	0000 _H
CC24IC	b	F170 _H	E B8 _H	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000 _H
CC25		FE72 _H	39 _H	CAPCOM Register 25	0000 _H
CC25IC	b	F172 _H	E B9 _H	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000 _H
CC26		FE74 _H	3A _H	CAPCOM Register 26	0000 _H
CC26IC	b	F174 _H	E BA _H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000 _H
CC27		FE76 _H	3B _H	CAPCOM Register 27	0000 _H
CC27IC	b	F176 _H	E BB _H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000 _H
CC28		FE78 _H	3C _H	CAPCOM Register 28	0000 _H
CC28IC	b	F178 _H	E BC _H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000 _H
CC29		FE7A _H	3D _H	CAPCOM Register 29	0000 _H
CC29IC	b	F184 _H	E C2 _H	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000 _H
CC2IC	b	FF7C _H	BE _H	CAPCOM Reg. 2 Interrupt Ctrl. Reg.	0000 _H
CC3		FE86 _H	43 _H	CAPCOM Register 3	0000 _H
CC30		FE7C _H	3E _H	CAPCOM Register 30	0000 _H
CC30IC	b	F18C _H	E C6 _H	CAPCOM Reg. 30 Interrupt Ctrl. Reg.	0000 _H
CC31		FE7E _H	3F _H	CAPCOM Register 31	0000 _H
CC31IC	b	F194 _H	E CA _H	CAPCOM Reg. 31 Interrupt Ctrl. Reg.	0000 _H
CC3IC	b	FF7E _H	BF _H	CAPCOM Reg. 3 Interrupt Ctrl. Reg.	0000 _H

Functional Description
Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
S0EIC	b	FF70 _H	B8 _H	Serial Chan. 0 Error Interrupt Ctrl. Reg.	0000 _H
S0RBUF		FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	XX _H
S0RIC	b	FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC	b	F19C _H	E CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF		FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Reg. (write only)	00 _H
S0TIC	b	FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H
SP		FE12 _H	09 _H	CPU System Stack Pointer Register	FC00 _H
SSCBR		F0B4 _H	E 5A _H	SSC Baudrate Register	0000 _H
SSCCON	b	FFB2 _H	D9 _H	SSC Control Register	0000 _H
SSCEIC	b	FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB		F0B2 _H	E 59 _H	SSC Receive Buffer	XXXX _H
SSCRIC	b	FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB		F0B0 _H	E 58 _H	SSC Transmit Buffer	0000 _H
SSCTIC	b	FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV		FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN		FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b	FF12 _H	89 _H	CPU System Configuration Register	¹⁾ 0xx0 _H
T0		FE50 _H	28 _H	CAPCOM Timer 0 Register	0000 _H
T01CON	b	FF50 _H	A8 _H	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000 _H
T0IC	b	FF9C _H	CE _H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000 _H
T0REL		FE54 _H	2A _H	CAPCOM Timer 0 Reload Register	0000 _H
T1		FE52 _H	29 _H	CAPCOM Timer 1 Register	0000 _H
T1IC	b	FF9E _H	CF _H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000 _H
T1REL		FE56 _H	2B _H	CAPCOM Timer 1 Reload Register	0000 _H
T2		FE40 _H	20 _H	GPT1 Timer 2 Register	0000 _H
T2CON	b	FF40 _H	A0 _H	GPT1 Timer 2 Control Register	0000 _H

4 Electrical Parameters

4.1 General Parameters

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	$V_{DD} + 0.5$	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	100	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Electrical Parameters

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, $f_{CPUmax} = 33 \text{ MHz}$
		2.5 ¹⁾	5.5	V	Power Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin ²⁾³⁾
Absolute sum of overload currents	$\Sigma I_{OV} $	–	50	mA	³⁾
External Load Capacitance	C_L	–	50	pF	Pin drivers in fast edge mode (PDCR.BIPEC = '0')
		–	30	pF	Pin drivers in reduced edge mode (PDCR.BIPEC = '1') ³⁾
		–	100	pF	Pin drivers in fast edge mode, $f_{CPUmax} = 25 \text{ MHz}$ ⁴⁾
Ambient temperature	T_A	0	70	°C	SAB-C167CR ...
		-40	85	°C	SAF-C167CR ...
		-40	125	°C	SAK-C167CR ...

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5 \text{ V}$ or $V_{OV} < V_{SS} - 0.5 \text{ V}$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL1, \overline{RD} , \overline{WR} , etc.

3) Not subject to production test - verified by design/characterization.

4) The increased capacitive load is valid for the 25 MHz-derivatives up to a CPU clock frequency of 25 MHz. Under these circumstances the timing parameters as specified in the "C167CR Data Sheet 1999-06" are valid.

Electrical Parameters

- 9) This specification is valid during Reset and during Adapt-mode.
 10) Not subject to production test - verified by design/characterization.

Table 12 Power Consumption C167CR (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DD}	—	$15 + 2.5 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current	I_{ID}	—	$10 + 1.0 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ¹⁾
Power-down mode supply current	I_{PD}	—	50	μA	$V_{DD} = V_{DDmax}$ ²⁾

- 1) The supply current is a function of the operating frequency. This dependency is illustrated in [Figure 9](#). These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD} , all outputs (including pins configured as outputs) disconnected.

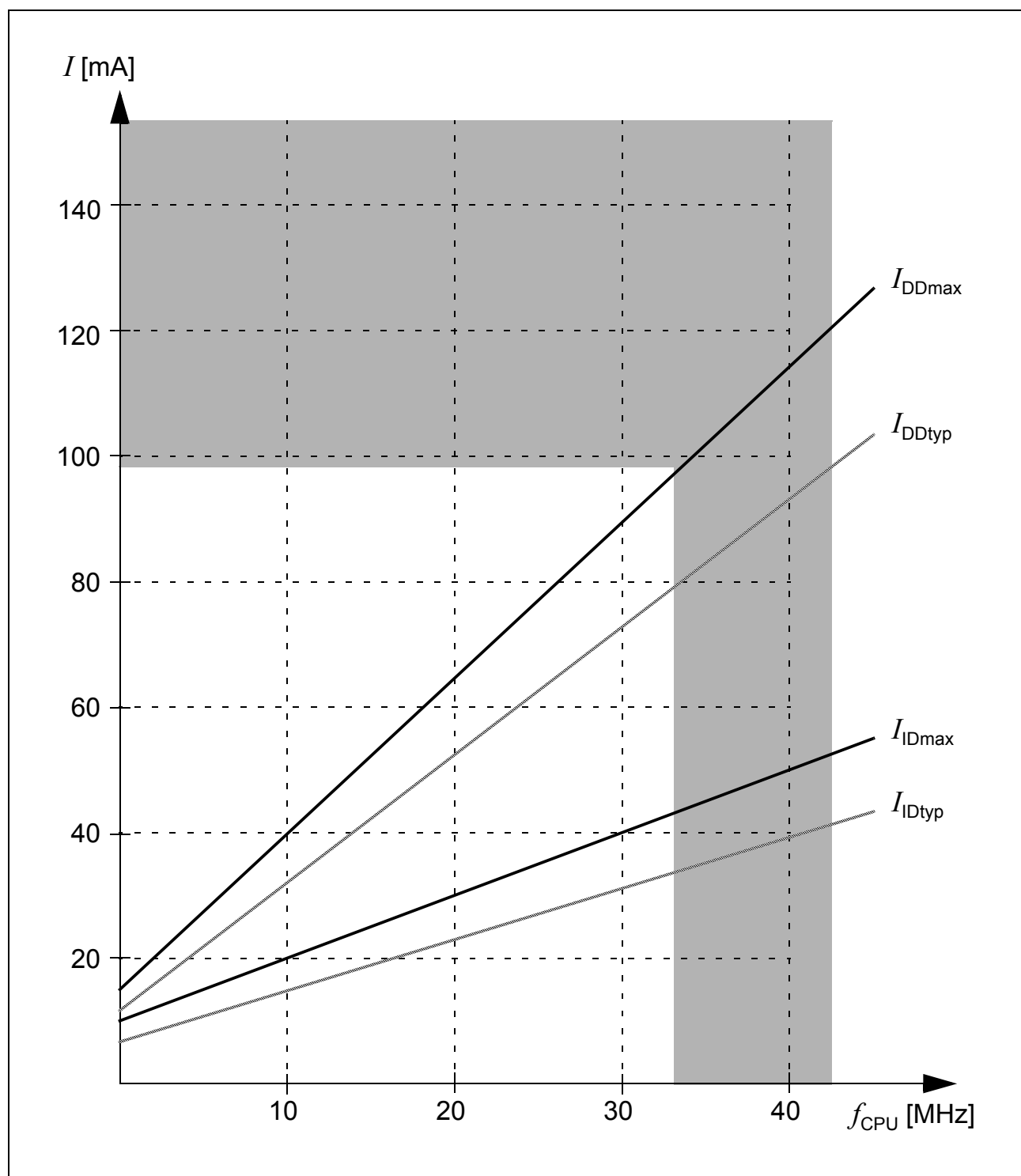


Figure 9 Supply/Idle Current as a Function of Operating Frequency

Electrical Parameters
4.3 Analog/Digital Converter Parameters
Table 13 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Analog reference supply	V_{AREF} SR	4.0	$V_{DD} + 0.1$	V	1)
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.1$	$V_{SS} + 0.2$	V	—
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}	0.5	6.25	MHz	3)
Conversion time	t_C CC	—	$40 t_{BC} + t_S + 2 t_{CPU}$	—	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL} CC	—	$3328 t_{BC}$	—	5)
Total unadjusted error	TUE CC	—	± 2	LSB	1)
Internal resistance of reference voltage source	R_{AREF} SR	—	$t_{BC} / 60 - 0.25$	k Ω	t_{BC} in [ns] ⁶⁾⁷⁾
Internal resistance of analog source	R_{ASRC} SR	—	$t_S / 450 - 0.25$	k Ω	t_S in [ns] ⁷⁾⁸⁾
ADC input capacitance	C_{AIN} CC	—	33	pF	7)

- 1) TUE is tested at $V_{AREF} = 5.0$ V, $V_{AGND} = 0$ V, $V_{DD} = 4.9$ V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DD} + 0.2$ V) the maximum TUE is increased to ± 3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ± 4 LSB.
- 2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from [Table 14](#).
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.
- 5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.
- 6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.
- 7) Not subject to production test - verified by design/characterization.

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- 8) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result.

Values for the sample time t_S depend on programming and can be taken from [Table 14](#).

Sample time and conversion time of the C167CR's A/D Converter are programmable. [Table 14](#) should be used to calculate the above timings.

The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 14 A/D Converter Computation Table

ADCON.15 14 (ADCTC)	A/D Converter Basic clock f_{BC}	ADCON.13 12 (ADSTC)	Sample time t_S
00	$f_{CPU} / 4$	00	$t_{BC} \times 8$
01	$f_{CPU} / 2$	01	$t_{BC} \times 16$
10	$f_{CPU} / 16$	10	$t_{BC} \times 32$
11	$f_{CPU} / 8$	11	$t_{BC} \times 64$

Converter Timing Example:

Assumptions: $f_{CPU} = 25 \text{ MHz}$ (i.e. $t_{CPU} = 40 \text{ ns}$), ADCTC = '00', ADSTC = '00'

Basic clock $f_{BC} = f_{CPU} / 4 = 6.25 \text{ MHz}$, i.e. $t_{BC} = 160 \text{ ns}$

Sample time $t_S = t_{BC} \times 8 = 1280 \text{ ns}$

Conversion time $t_C = t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) \text{ ns} = 7.8 \mu\text{s}$

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upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins P0.15-13 (P0H.7-5).

Table 15 associates the combinations of these three bits with the respective clock generation mode.

Table 15 C167CR Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{\text{CPU}} = f_{\text{OSC}} \times F$	External Clock Input Range ¹⁾	Notes
1 1 1	$f_{\text{OSC}} \times 4$	2.5 to 8.25 MHz	Default configuration
1 1 0	$f_{\text{OSC}} \times 3$	3.33 to 11 MHz	–
1 0 1	$f_{\text{OSC}} \times 2$	5 to 16.5 MHz	–
1 0 0	$f_{\text{OSC}} \times 5$	2 to 6.6 MHz	–
0 1 1	$f_{\text{OSC}} \times 1$	1 to 33 MHz	Direct drive ²⁾
0 1 0	$f_{\text{OSC}} \times 1.5$	6.66 to 22 MHz	–
0 0 1	$f_{\text{OSC}} / 2$	2 to 66 MHz	CPU clock via prescaler
0 0 0	$f_{\text{OSC}} \times 2.5$	4 to 13.2 MHz	–

1) The external clock input range refers to a CPU clock range of 10 ... 33 MHz (PLL operation).

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{\text{CPU}} = f_{\text{OSC}} \times F$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

General Notes for the Following Timing Figures

These standard notes apply to all subsequent timing figures. Additional individual notes are placed at the respective figure.

1. *The falling edge of signals \overline{RD} and $\overline{WR/WRH/WRL/WrCS}$ is controlled by the Read/Write delay feature (bit $BUSCON.RWDCx$).*
2. *A bus cycle is extended here, if MCTC waitstates are selected or if the \overline{READY} input is sampled inactive.*
3. *A bus cycle is extended here, if an MTTC waitstate is selected.*

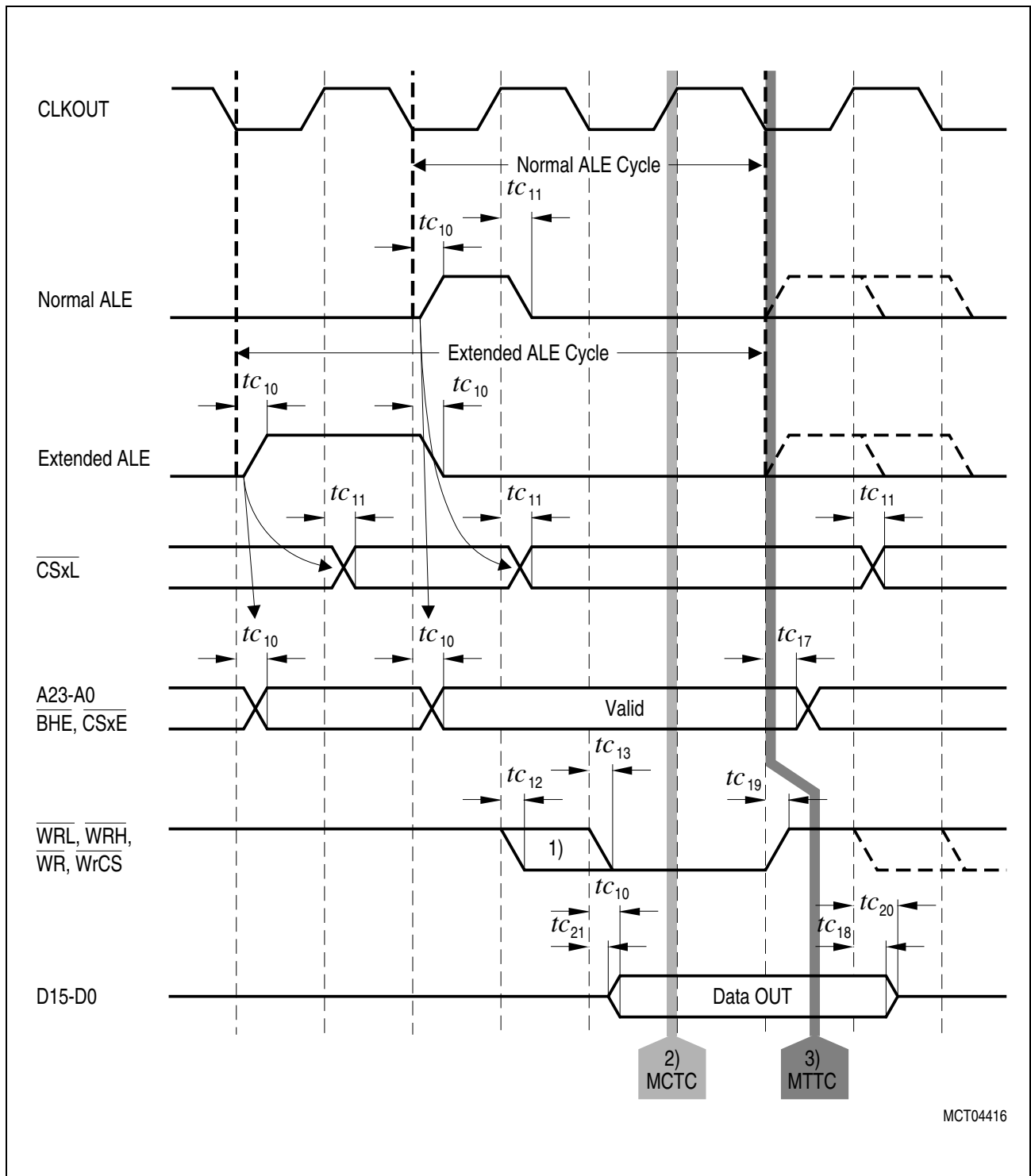


Figure 16 Demultiplexed Bus, Write Access

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External Bus Arbitration
Table 21 Bus Arbitration Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT falling edge	t_{c28}	SR	18	–	ns
CLKOUT to $\overline{\text{BREQ}}$ delay	t_{c29}	CC	-4	6	ns
CLKOUT to $\overline{\text{HLDA}}$ delay	t_{c30}	CC	-4	6	ns
$\overline{\text{CSx}}$ release ¹⁾	t_{c31}	CC	0	10	ns
$\overline{\text{CSx}}$ drive	t_{c32}	CC	-2	6	ns
Other signals release ¹⁾	t_{c33}	CC	0	10	ns
Other signals drive ¹⁾	t_{c34}	CC	0	6	ns

1) Not subject to production test - verified by design/characterization.

5 Package Outlines

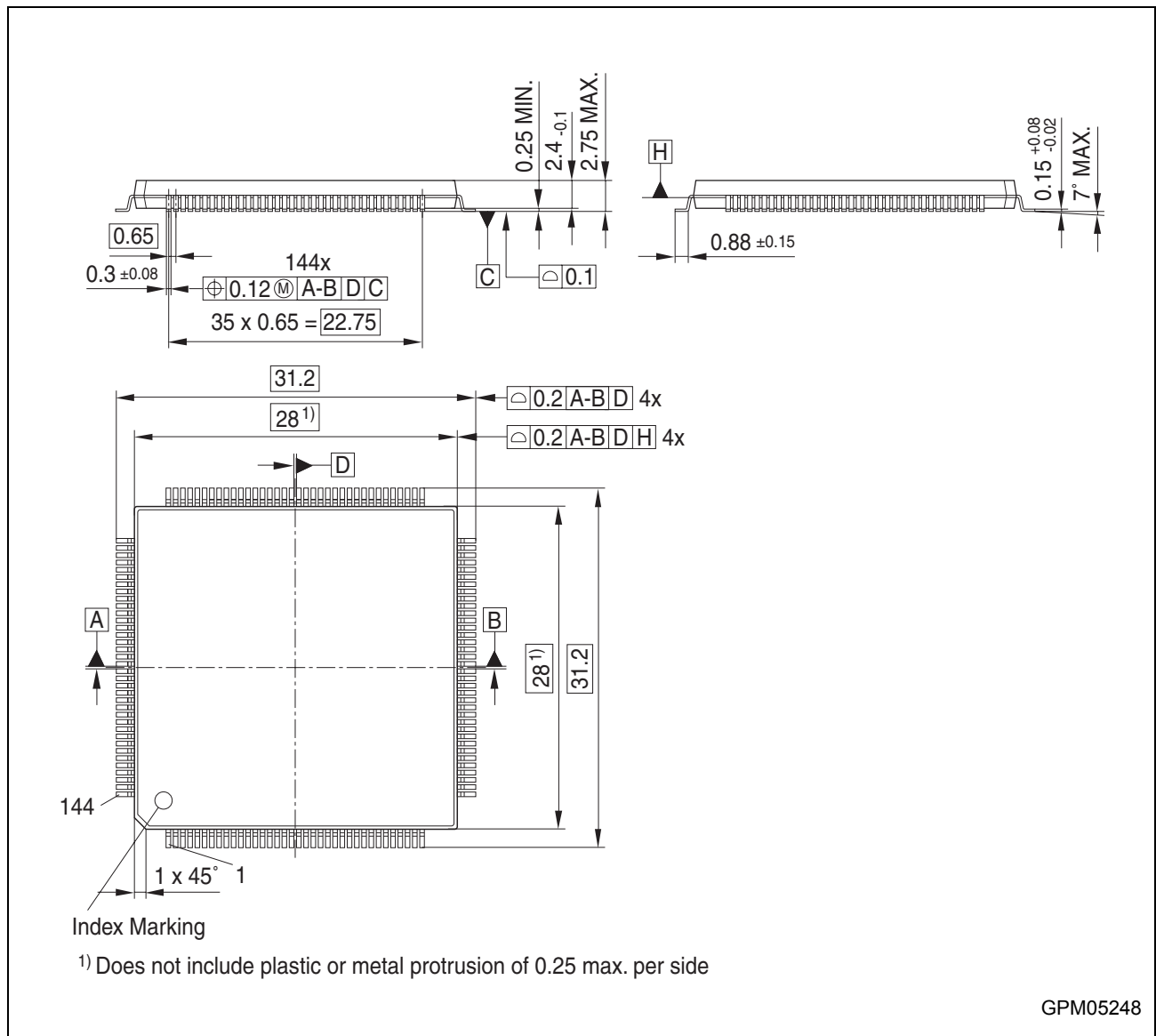


Figure 24 P-MQFP-144-8 (Plastic Metric Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

Dimensions in mm