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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167crlmhabxqla1

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- Up to 111 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package
- 176-Pin BGA Package[1)]

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CR please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **C167CR** throughout this document.

1) The external connections of the C167CR in P-BGA-176-2 are referred to as pins throughout this document, although they are mechanically realized as solder balls.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	47	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	48	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	49	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	50	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	51	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	52	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	53	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	54	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	57	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	58	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	59	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	60	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	61	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	62	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	63	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	64	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
OWE (V_{PP})	84	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	D13 C13	O I	XTAL2: Output of the oscillator amplifier circuit. XTAL1: Input to the oscillator amplifier and input to the internal clock generator. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTOUT}}$	D12	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{RSTIN}}$	E11	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	F3	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	F2	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	F4	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	G4	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	G3	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	G2	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	G1	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	H1	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	H4	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	J1	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	J2	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	J4	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	J3	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	K1	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	K2	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	L1	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input
V_{AREF}	B2	–	Reference voltage for the A/D converter.	
V_{AGND}	C2	–	Reference ground for the A/D converter.	

3.8 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
CC4		$FE88_H$		44_H	CAPCOM Register 4	0000_H
CC4IC	**b**	$FF80_H$		$C0_H$	CAPCOM Reg. 4 Interrupt Ctrl. Reg.	0000_H
CC5		$FE8A_H$		45_H	CAPCOM Register 5	0000_H
CC5IC	**b**	$FF82_H$		$C1_H$	CAPCOM Register 5 Interrupt Ctrl. Reg.	0000_H
CC6		$FE8C_H$		46_H	CAPCOM Register 6	0000_H
CC6IC	**b**	$FF84_H$		$C2_H$	CAPCOM Reg. 6 Interrupt Ctrl. Reg.	0000_H
CC7		$FE8E_H$		47_H	CAPCOM Register 7	0000_H
CC7IC	**b**	$FF86_H$		$C3_H$	CAPCOM Reg. 7 Interrupt Ctrl. Reg.	0000_H
CC8		$FE90_H$		48_H	CAPCOM Register 8	0000_H
CC8IC	**b**	$FF88_H$		$C4_H$	CAPCOM Reg. 8 Interrupt Ctrl. Reg.	0000_H
CC9		$FE92_H$		49_H	CAPCOM Register 9	0000_H
CC9IC	**b**	$FF8A_H$		$C5_H$	CAPCOM Reg. 9 Interrupt Ctrl. Reg.	0000_H
CCM0	**b**	$FF52_H$		$A9_H$	CAPCOM Mode Control Register 0	0000_H
CCM1	**b**	$FF54_H$		AA_H	CAPCOM Mode Control Register 1	0000_H
CCM2	**b**	$FF56_H$		AB_H	CAPCOM Mode Control Register 2	0000_H
CCM3	**b**	$FF58_H$		AC_H	CAPCOM Mode Control Register 3	0000_H
CCM4	**b**	$FF22_H$		91_H	CAPCOM Mode Control Register 4	0000_H
CCM5	**b**	$FF24_H$		92_H	CAPCOM Mode Control Register 5	0000_H
CCM6	**b**	$FF26_H$		93_H	CAPCOM Mode Control Register 6	0000_H
CCM7	**b**	$FF28_H$		94_H	CAPCOM Mode Control Register 7	0000_H
CP		$FE10_H$		08_H	CPU Context Pointer Register	$FC00_H$
CRIC	**b**	$FF6A_H$		$B5_H$	GPT2 CAPREL Interrupt Ctrl. Register	0000_H
CSP		$FE08_H$		04_H	CPU Code Segment Pointer Register (read only)	0000_H
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP2	**b**	$FFC2_H$		$E1_H$	Port 2 Direction Control Register	0000_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DP7	**b**	$FFD2_H$		$E9_H$	Port 7 Direction Control Register	00_H
DP8	**b**	$FFD6_H$		EB_H	Port 8 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7	**b**	$F1D2_H$	**E**	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8	**b**	$F1D6_H$	**E**	EB_H	Port 8 Open Drain Control Register	00_H
ONES		$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
P7	**b**	$FFD0_H$		$E8_H$	Port 7 Register (8 bits)	00_H
P8	**b**	$FFD4_H$		EA_H	Port 8 Register (8 bits)	00_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
T2IC	**b**	$FF60_H$		$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3		$FE42_H$		21_H	GPT1 Timer 3 Register	0000_H
T3CON	**b**	$FF42_H$		$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC	**b**	$FF62_H$		$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4		$FE44_H$		22_H	GPT1 Timer 4 Register	0000_H
T4CON	**b**	$FF44_H$		$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC	**b**	$FF64_H$		$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5		$FE46_H$		23_H	GPT2 Timer 5 Register	0000_H
T5CON	**b**	$FF46_H$		$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC	**b**	$FF66_H$		$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6		$FE48_H$		24_H	GPT2 Timer 6 Register	0000_H
T6CON	**b**	$FF48_H$		$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC	**b**	$FF68_H$		$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
T7		$F050_H$	**E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON	**b**	$FF20_H$		90_H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000_H
T7IC	**b**	$F17A_H$	**E**	BE_H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000_H
T7REL		$F054_H$	**E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H
T8		$F052_H$	**E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC	**b**	$F17C_H$	**E**	BF_H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000_H
T8REL		$F056_H$	**E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR	**b**	$FFAC_H$		$D6_H$	Trap Flag Register	0000_H
WDT		$FEAE_H$		57_H	Watchdog Timer Register (read only)	0000_H
WDTCON		$FFAE_H$		$D7_H$	Watchdog Timer Control Register	[2] $00XX_H$
XP0IC	**b**	$F186_H$	**E**	$C3_H$	CAN1 Module Interrupt Control Register	0000_H
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Unassigned Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Unassigned Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	PLL/OWD Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

4 Electrical Parameters

4.1 General Parameters

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CR and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C167CR will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C167CR.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	0.2 V_{DD} - 0.1	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	0.3 V_{DD}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	2.0	V	–
Input high voltage (TTL, all except RSTIN and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage RSTIN (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	–	mV	Series resistance = 0 Ω
Output low voltage (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, CLKOUT, RSTOUT, RSTIN[2)])	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL} = 1.6 mA

4.3 Analog/Digital Converter Parameters

Table 13 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2 t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} + 0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not subject to production test - verified by design/characterization.

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the C167CR is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see **Figure 10**).

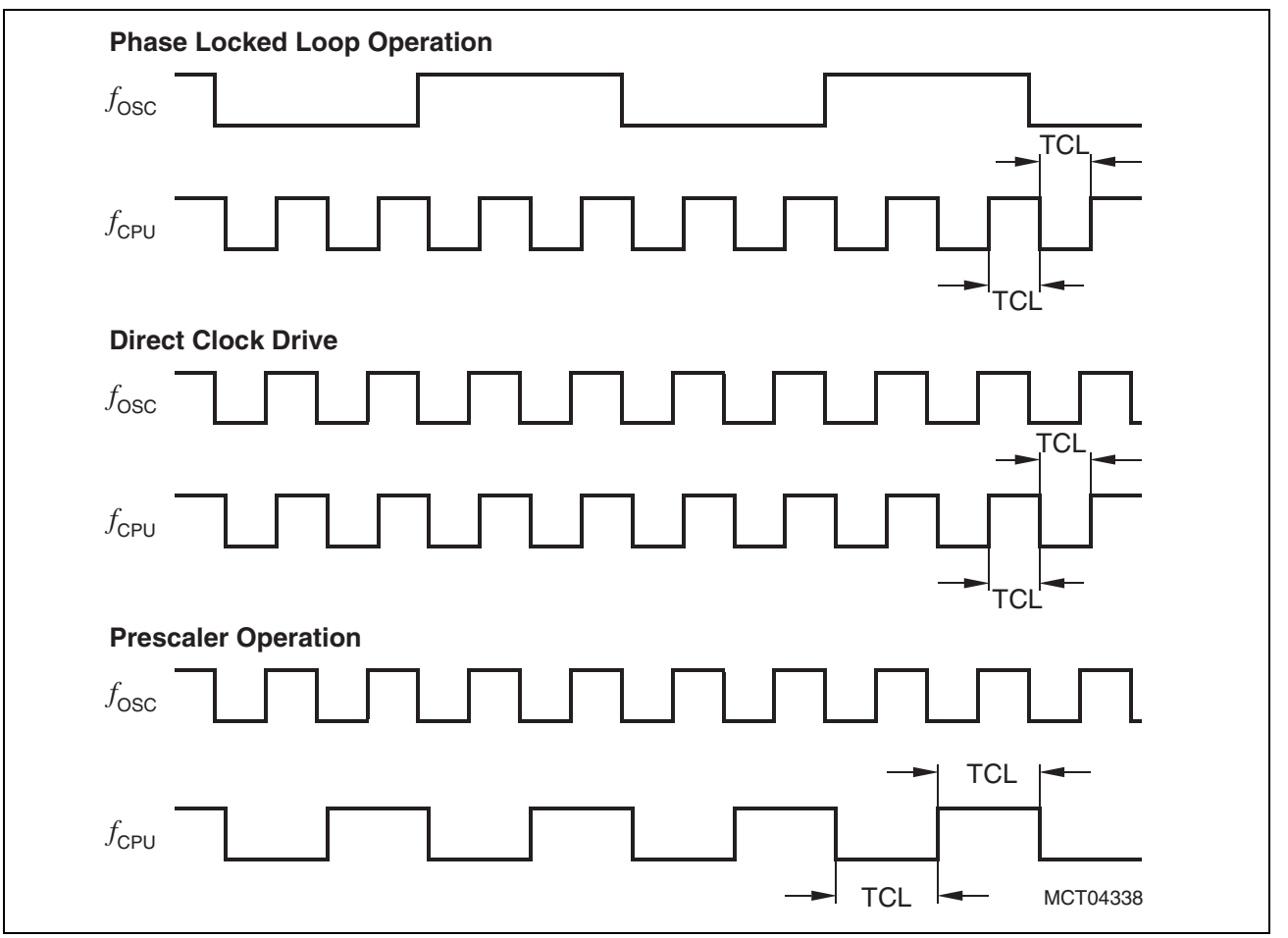

Figure 10 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C167CR.

Note: The example for PLL operation shown in the fig. above refers to a PLL factor of 4.

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5.
Upon a long hardware reset register RP0H is loaded with the logic levels present on the

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \text{ (DC = duty cycle)} \quad (2)$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

Table 19 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Output delay from CLKOUT falling edge Valid for: address, BHE, early CS, write data out, ALE	tc_{10}	CC	-2	11	ns
Output delay from CLKOUT rising edge Valid for: latched CS, ALE low	tc_{11}	CC	-2	6	ns
Output delay from CLKOUT rising edge Valid for: WR low (no RW delay), RD low (no RW delay)	tc_{12}	CC	-2	8	ns
Output delay from CLKOUT falling edge Valid for: RD/WR low (with RW delay), RD high (with RW delay)	tc_{13}	CC	-2	6	ns
Input setup time to CLKOUT falling edge Valid for: read data in	tc_{14}	SR	14	–	ns
Input hold time after CLKOUT falling edge Valid for: read data in[1)]	tc_{15}	SR	0	–	ns
Output hold time after CLKOUT falling edge Valid for: address, BHE, early CS[2)]	tc_{17}	CC	-2	6	ns
Output hold time after CLKOUT edge[3)] Valid for: write data out	tc_{18}	CC	-2	–	ns
Output delay from CLKOUT falling edge Valid for: WR high	tc_{19}	CC	-2	4	ns
Turn off delay after CLKOUT edge[3)] Valid for: write data out	tc_{20}	CC	–	7	ns
Turn on delay after CLKOUT falling edge[3)] Valid for: write data out	tc_{21}	CC	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore the read data may be removed immediately after the rising edge of RD. Address changes before the end of RD have also no impact on (demultiplexed) read cycles.

2) Due to comparable propagation delays (at comparable capacitive loads) the address does not change before WR goes high. The minimum output delay (tc_{17min}) is therefore the actual value of tc_{19}.

3) Not subject to production test - verified by design/characterization.

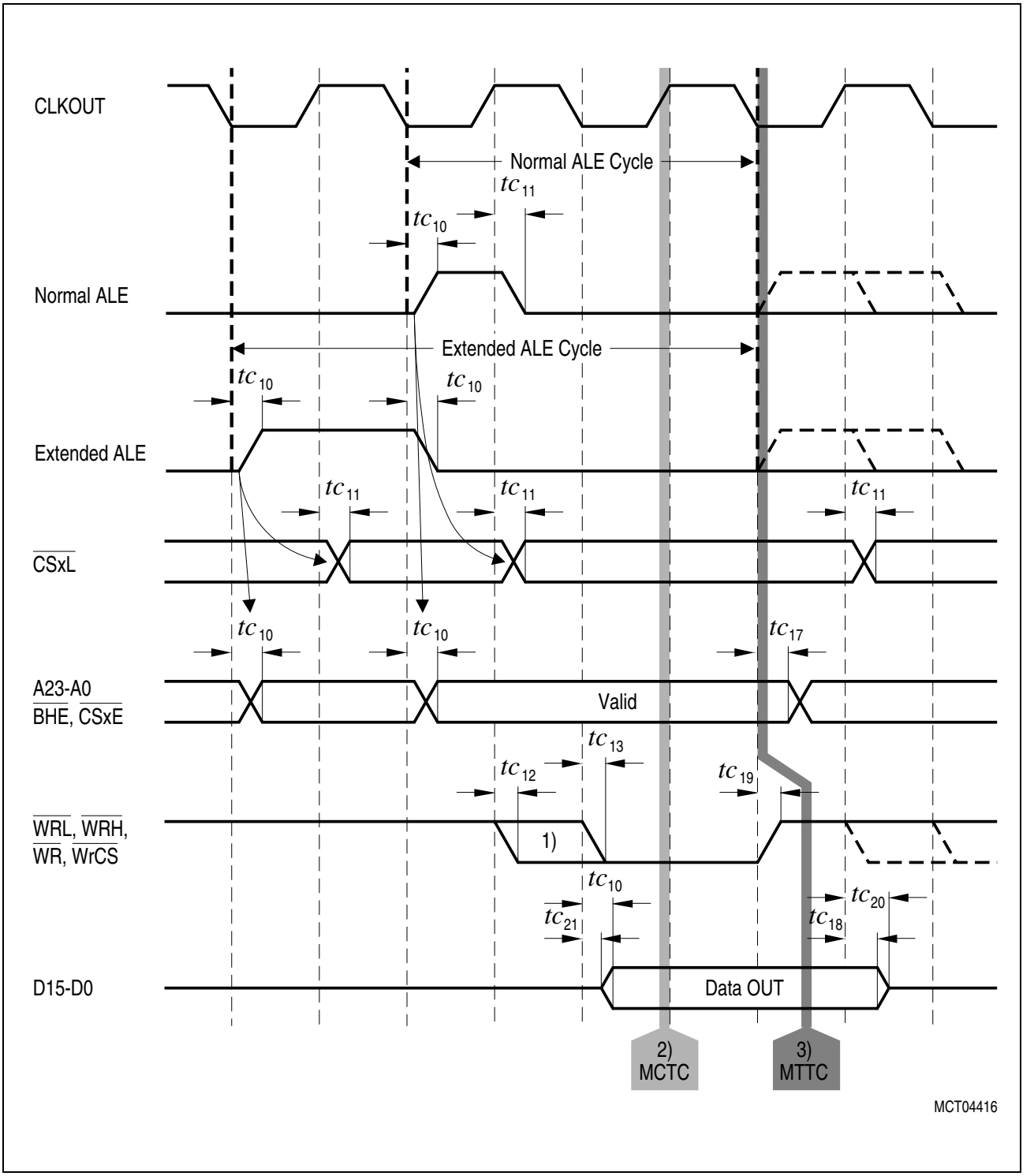

Figure 16 Demultiplexed Bus, Write Access

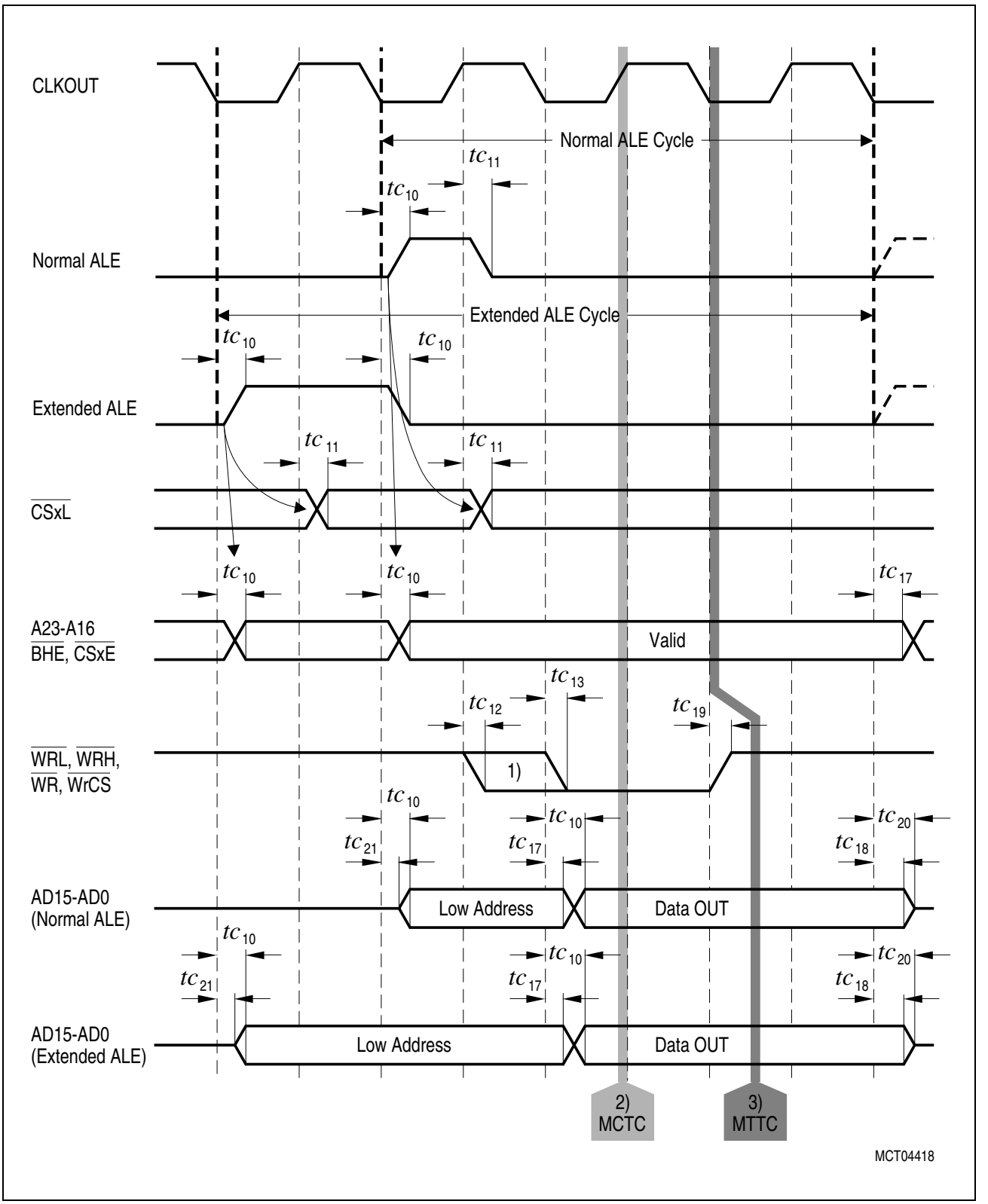

Figure 18 Multiplexed Bus, Write Access

Bus Cycle Control via $\overline{\text{READY}}$ Input

The duration of an external bus cycle can be controlled by the external circuitry via the $\overline{\text{READY}}$ input signal.

Synchronous $\overline{\text{READY}}$ permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous $\overline{\text{READY}}$ puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage.

Table 20 $\overline{\text{READY}}$ Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Input setup time to CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{25}	CC	12	–	ns
Input hold time after CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{26}	CC	0	–	ns
Asynchronous $\overline{\text{READY}}$ input low time[6)]	tc_{27}	CC	$tc_5 + tc_{25}$	–	ns

Notes (Valid also for **Figure 20**)

4. *Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).*
5. *$\overline{\text{READY}}$ sampled HIGH at this sampling point generates a $\overline{\text{READY}}$ controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.*
6. *These timings are given for test purposes only, in order to assure recognition at a specific clock edge. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT, it must fulfill tc_{27} in order to be safely synchronized. Proper deactivation of $\overline{\text{READY}}$ is guaranteed if $\overline{\text{READY}}$ is deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).*
7. *Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus **with** MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus **without** MTTC waitstate this delay is zero.*
8. *If the next following bus cycle is $\overline{\text{READY}}$ controlled, an active $\overline{\text{READY}}$ signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the MTTC waitstate of the current cycle, and on the MCTC waitstates and the ALE mode of the next following cycle. If the current cycle uses a multiplexed bus the intrinsic MUX waitstate adds another CLKOUT cycle to the $\overline{\text{READY}}$ deactivation time.*