Infineon Technologies - C167CRLMHAKXQLA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167crlmhakxqla1

C167CR
C167SR

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Revision History:	**2005-02**	V3.3
Previous Version:	V3.2, 2001-07 V3.1, 2000-04 V3.0, 2000-02 1999-10 (Introduction of clock-related timing) 1999-06 1999-03 (Summarizes and replaces all older docs) 1998-03 (C167SR/CR, 25 MHz Addendum) 07.97 / 12.96 (C167CR-4RM) 12.96 (C167CR-16RM) 06.95 (C167CR, C167SR) 06.94 / 05.93 (C167)	

Page	Subjects (major changes since last revision)
all	The layout of several graphics and text structures has been adapted to company documentation rules, obvious typographical errors have been corrected.
all	The contents of this document have been re-arranged into numbered sections and a table of contents has been added.
6	BGA-type added to product list
8	Pin designation corrected (pin 78)
9	Input threshold control added to Port 6
17 ... 25	Pin diagram and pin description for BGA package added
45	Port 6 added to input-threshold controlled ports
85	Mechanical package drawing corrected (P-MQFP-144-8)
86	Mechanical package drawing added (P-BGA-176-2)

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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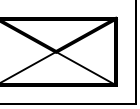

- Up to 111 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package
- 176-Pin BGA Package[1)]

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CR please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **C167CR** throughout this document.

1) The external connections of the C167CR in P-BGA-176-2 are referred to as pins throughout this document, although they are mechanically realized as solder balls.

2.2 Pin Configuration and Definition for P-MQFP-144-8

The pins of the C167CR are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package.

*Note: The P-BGA-176-2 is described in **Table 3** and **Figure 3**.*

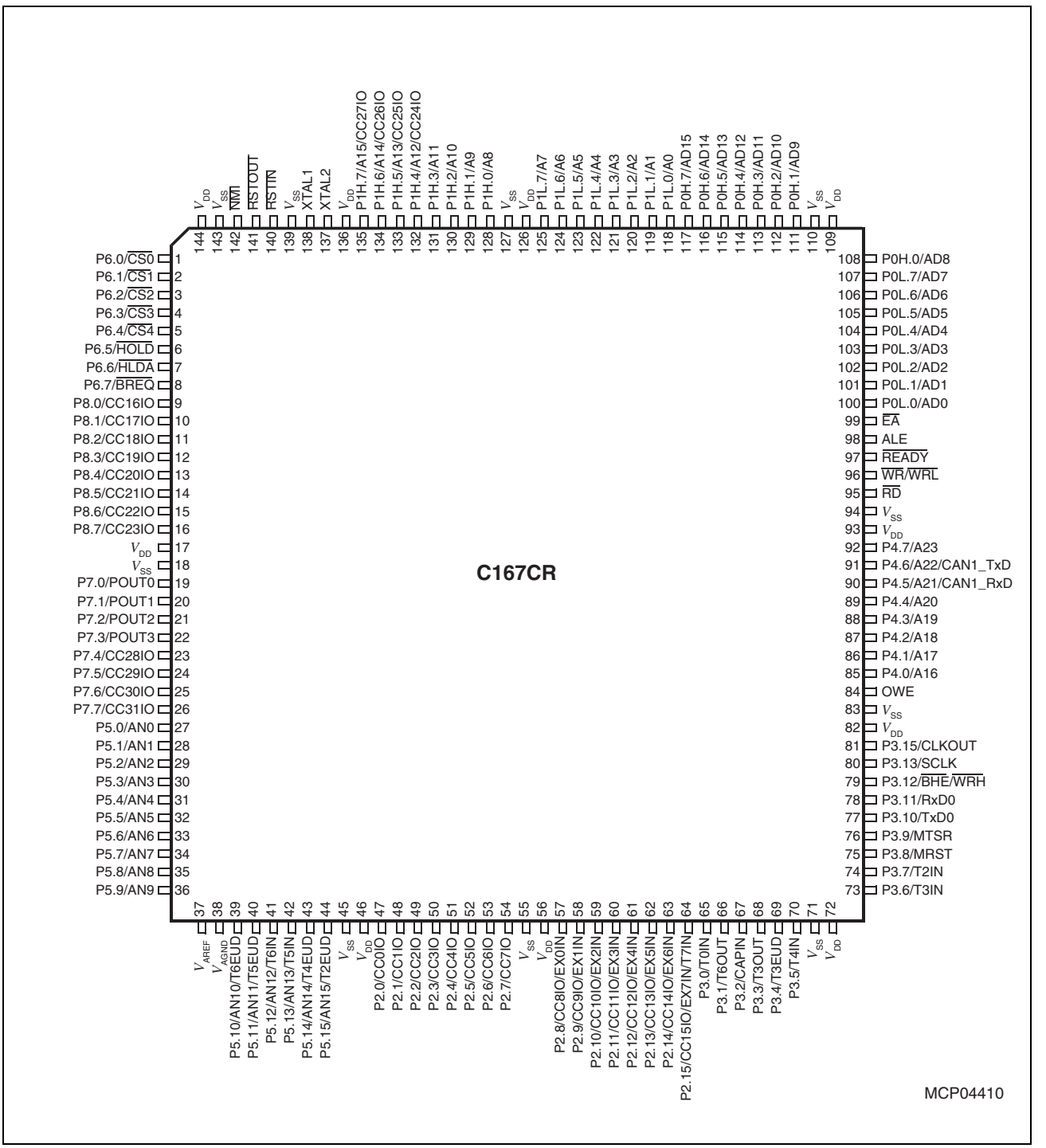

Figure 2 Pin Configuration P-MQFP-144-8 (top view)

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	47	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	48	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	49	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	50	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	51	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	52	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	53	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	54	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	57	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	58	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	59	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	60	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	61	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	62	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	63	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	64	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	85	O	A16 Least Significant Segment Address Line
P4.1	86	O	A17 Segment Address Line
P4.2	87	O	A18 Segment Address Line
P4.3	88	O	A19 Segment Address Line
P4.4	89	O	A20 Segment Address Line
P4.5	90	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	91	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	92	O	A23 Most Significant Segment Address Line
RD	95	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	96	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Table 3 Pin Definitions and Functions P-BGA-176-2

Symbol	Pin Num.	Input Outp.	Function
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	A5	I	AN0
P5.1	D5	I	AN1
P5.2	A4	I	AN2
P5.3	C5	I	AN3
P5.4	B4	I	AN4
P5.5	A3	I	AN5
P5.6	C4	I	AN6
P5.7	D4	I	AN7
P5.8	B3	I	AN8
P5.9	C3	I	AN9
P5.10	D3	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	C1	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	D1	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	D2	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	E3	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	E2	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	D7	O	POUT0 PWM Channel 0 Output
P7.1	C7	O	POUT1 PWM Channel 1 Output
P7.2	B7	O	POUT2 PWM Channel 2 Output
P7.3	A7	O	POUT3 PWM Channel 3 Output
P7.4	D6	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	C6	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	B6	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	A6	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.

Note: When the on-chip CAN Module is to be used the segment address output on Port 4 must be limited to 4 bits (i.e. A19 … A16) in order to enable the alternate function of the CAN interface pins. CS lines can be used to increase the total amount of addressable external memory.

3.4 Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C167CR is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CR supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CR has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible C167CR interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 C167CR Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H

3.5 Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin (except for CC24 … CC27) to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

3.9 Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 kbit/s/1.03 Mbit/s and half-duplex synchronous communication at up to 3.1/4.1 Mbit/s (@ 25/33 MHz CPU clock).
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25/8.25 Mbit/s (@ 25/33 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception, and error handling three separate interrupt vectors are provided.
The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

3.12 Parallel Ports

The C167CR provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 6, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 Kbytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output (CLKOUT).
Port 5 is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) of the C167CR's port drivers can be selected via the Port Driver Control Register (PDCR). Two bits select fast edges ('0') or reduced edges ('1') for bus interface pins and non-bus pins separately.
PDCR.0 = BIPEC controls PORT0, PORT1, Port 4, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE, CLKOUT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$.
PDCR.4 = NBPEC controls Port 3, Port 8, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$ (bidir. reset mode).

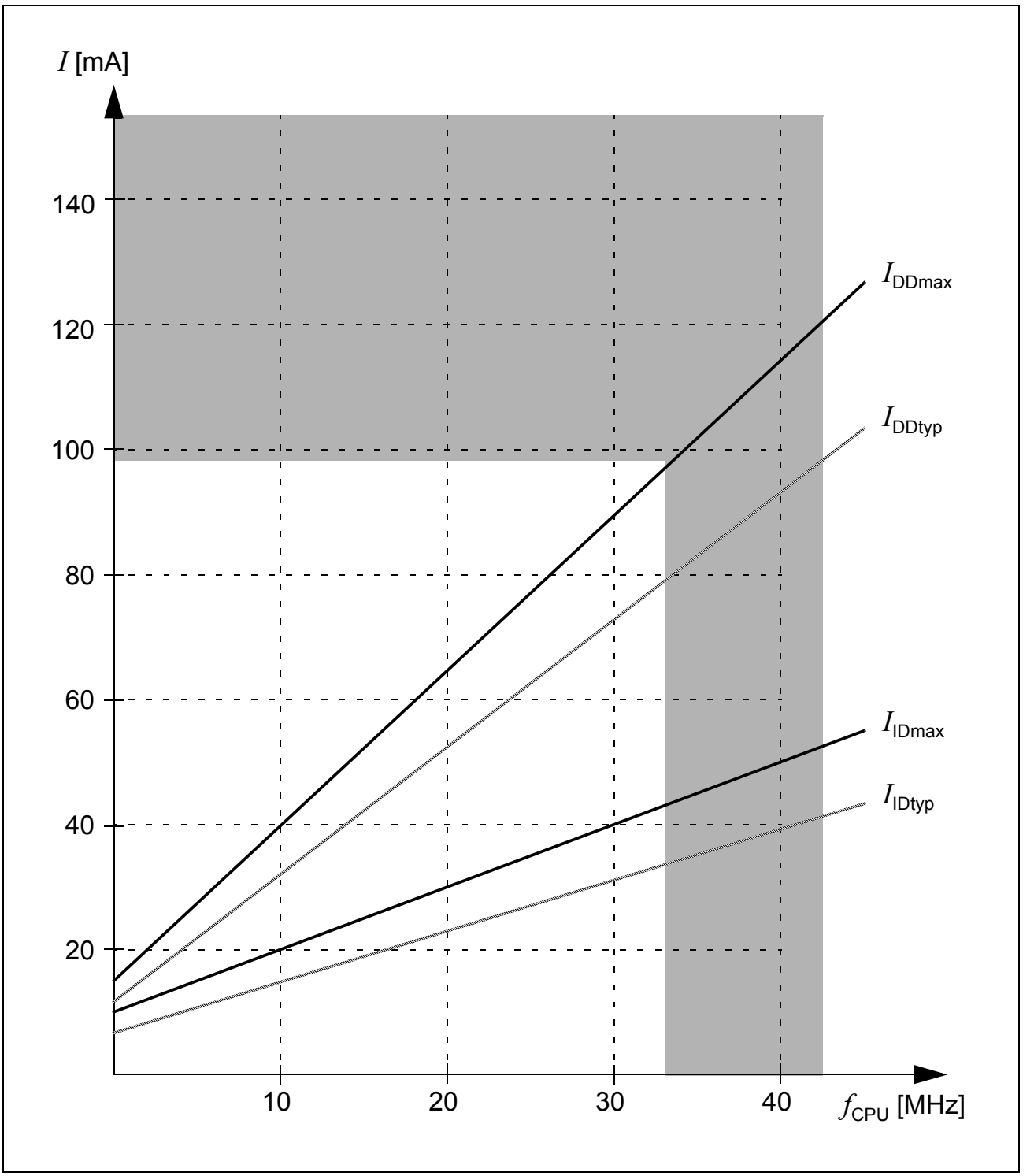

Figure 9 Supply/Idle Current as a Function of Operating Frequency

4.3 Analog/Digital Converter Parameters

Table 13 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2 t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} + 0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not subject to production test - verified by design/characterization.

4.4.4 External Bus Timing

Table 17 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	30[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter.
For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for f_{CPU} > 25 MHz).
For longer periods the relative deviation decreases (see PLL deviation formula).

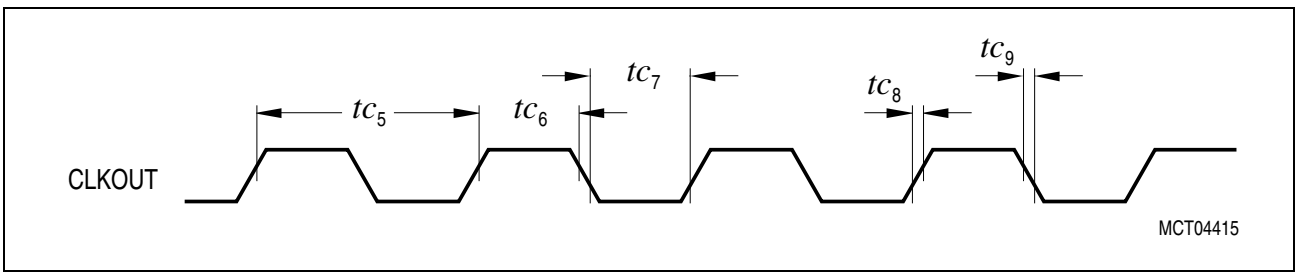

Figure 15 CLKOUT Signal Timing

Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

Table 18 Variable Memory Cycles

Bus Cycle Type	Bus Cycle Duration	Unit	25/33 MHz, 0 Waitstates
Demultiplexed bus cycle with normal ALE	4 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	80 ns/60.6 ns
Demultiplexed bus cycle with extended ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with normal ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with extended ALE	8 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	160 ns/121.2 ns

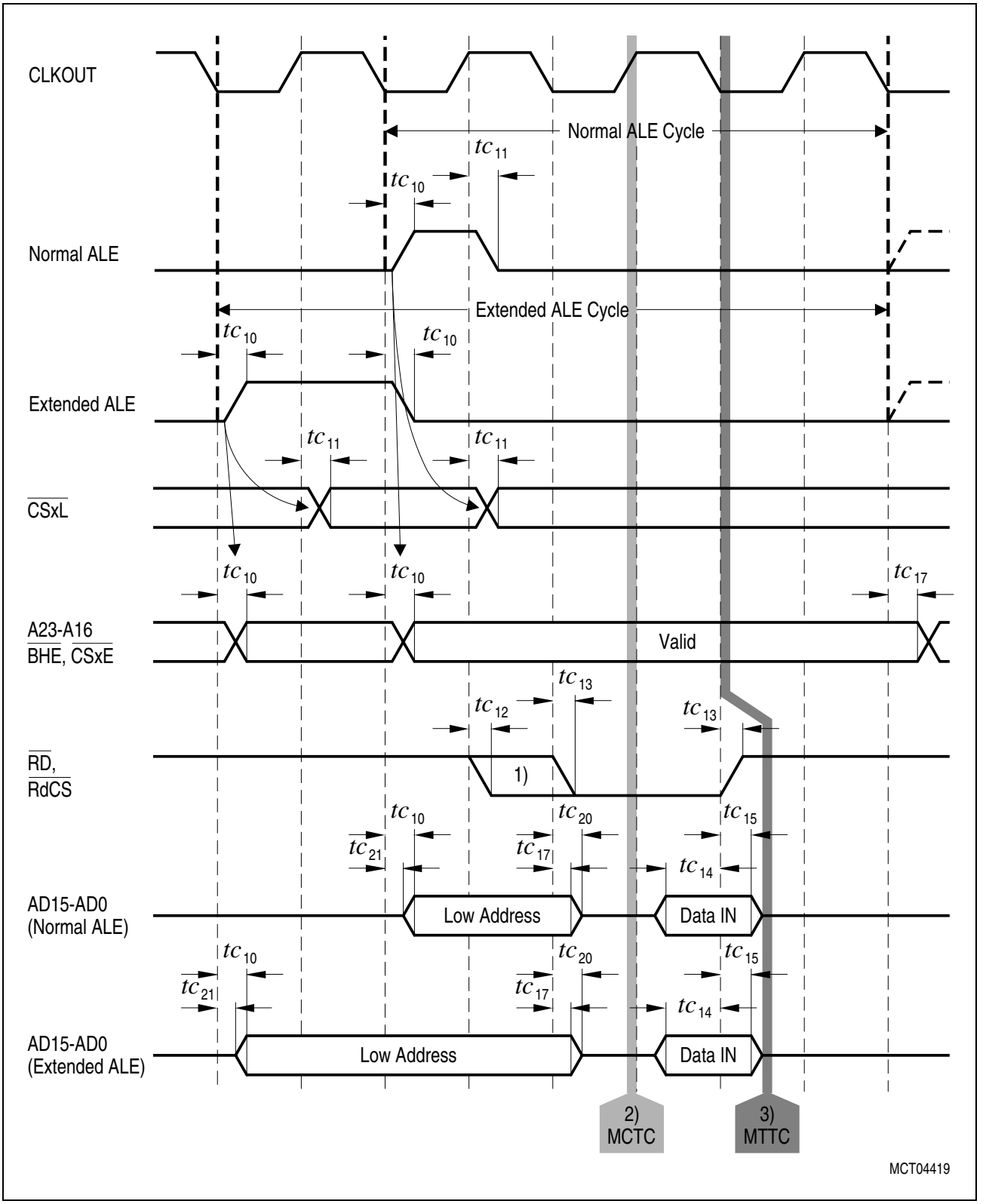

Figure 19 Multiplexed Bus, Read Access

w w w . i n f i n e o n . c o m

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