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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167crlmhakxqla2

C167CR
C167SR

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Table 3 Pin Definitions and Functions P-BGA-176-2

Symbol	Pin Num.	Input Outp.	Function
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	A5	I	AN0
P5.1	D5	I	AN1
P5.2	A4	I	AN2
P5.3	C5	I	AN3
P5.4	B4	I	AN4
P5.5	A3	I	AN5
P5.6	C4	I	AN6
P5.7	D4	I	AN7
P5.8	B3	I	AN8
P5.9	C3	I	AN9
P5.10	D3	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	C1	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	D1	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	D2	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	E3	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	E2	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	D7	O	POUT0 PWM Channel 0 Output
P7.1	C7	O	POUT1 PWM Channel 1 Output
P7.2	B7	O	POUT2 PWM Channel 2 Output
P7.3	A7	O	POUT3 PWM Channel 3 Output
P7.4	D6	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	C6	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	B6	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	A6	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	B10	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	A10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	D9	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	C9	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	B9	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	A9	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	D8	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	C8	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	A13	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	B12	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	D10	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	C11	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	A12	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	B11	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	C10	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	A11	O	$\overline{BREQ}$ Bus Request Output
$\overline{NMI}$	C14	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{NMI}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{NMI}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{NMI}$ should be pulled high externally.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
OWE (V_{PP})	N6	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	M1	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	K3	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	L2	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	M2	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	N1	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	P2	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	M3	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	N2	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	N3	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	P3	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	N4	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	M4	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	L4	O	$\overline{BHE}$	External Memory High Byte Enable Signal,
		O	$\overline{WRH}$	External Memory High Byte Write Strobe
P3.13	P4	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	N5	O	CLKOUT	System Clock Output (= CPU Clock)

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	F3	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	F2	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	F4	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	G4	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	G3	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	G2	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	G1	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	H1	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	H4	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	J1	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	J2	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	J4	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	J3	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	K1	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	K2	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	L1	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input
V_{AREF}	B2	–	Reference voltage for the A/D converter.	
V_{AGND}	C2	–	Reference ground for the A/D converter.	

3.4 Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C167CR is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CR supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CR has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible C167CR interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 C167CR Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H

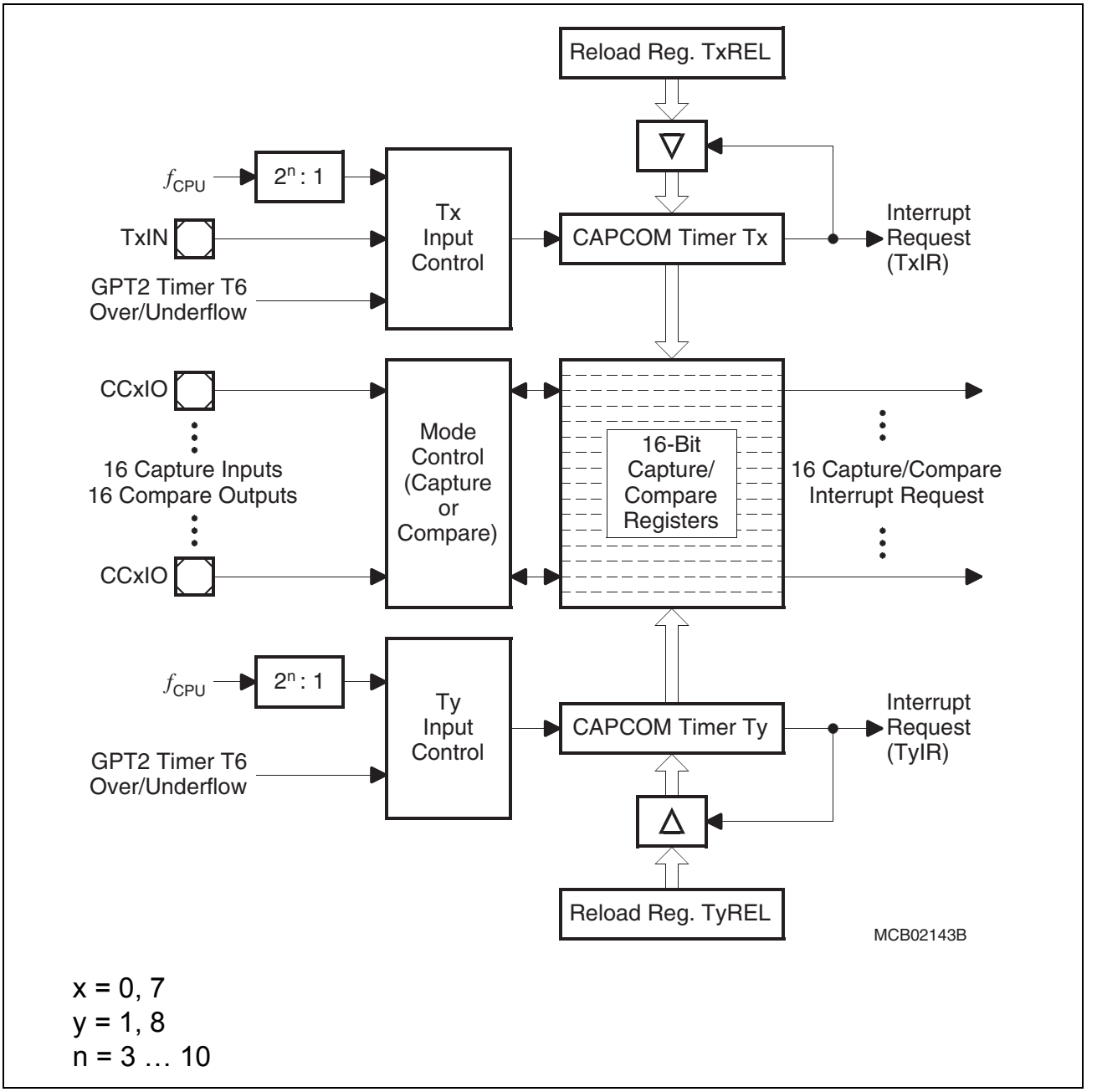

Figure 6 CAPCOM Unit Block Diagram

3.6 PWM Module

The Pulse Width Modulation Module can generate up to four PWM output signals using edge-aligned or center-aligned PWM. In addition the PWM module can generate PWM burst signals and single shot outputs. The frequency range of the PWM signals covers 4 Hz to 16.5 MHz (referred to a CPU clock of 33 MHz), depending on the resolution of the PWM output signal. The level of the output signals is selectable and the PWM module can generate interrupt requests.

3.8 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

Table 7 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC19IC b	$F166_H$ **E**	$B3_H$	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000_H
CC1IC b	$FF7A_H$	BD_H	CAPCOM Reg. 1 Interrupt Ctrl. Reg.	0000_H
CC2	$FE84_H$	42_H	CAPCOM Register 2	0000_H
CC20	$FE68_H$	34_H	CAPCOM Register 20	0000_H
CC20IC b	$F168_H$ **E**	$B4_H$	CAPCOM Reg. 20 Interrupt Ctrl. Reg.	0000_H
CC21	$FE6A_H$	35_H	CAPCOM Register 21	0000_H
CC21IC b	$F16A_H$ **E**	$B5_H$	CAPCOM Reg. 21 Interrupt Ctrl. Reg.	0000_H
CC22	$FE6C_H$	36_H	CAPCOM Register 22	0000_H
CC22IC b	$F16C_H$ **E**	$B6_H$	CAPCOM Reg. 22 Interrupt Ctrl. Reg.	0000_H
CC23	$FE6E_H$	37_H	CAPCOM Register 23	0000_H
CC23IC b	$F16E_H$ **E**	$B7_H$	CAPCOM Reg. 23 Interrupt Ctrl. Reg.	0000_H
CC24	$FE70_H$	38_H	CAPCOM Register 24	0000_H
CC24IC b	$F170_H$ **E**	$B8_H$	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000_H
CC25	$FE72_H$	39_H	CAPCOM Register 25	0000_H
CC25IC b	$F172_H$ **E**	$B9_H$	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000_H
CC26	$FE74_H$	$3A_H$	CAPCOM Register 26	0000_H
CC26IC b	$F174_H$ **E**	BA_H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000_H
CC27	$FE76_H$	$3B_H$	CAPCOM Register 27	0000_H
CC27IC b	$F176_H$ **E**	BB_H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000_H
CC28	$FE78_H$	$3C_H$	CAPCOM Register 28	0000_H
CC28IC b	$F178_H$ **E**	BC_H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000_H
CC29	$FE7A_H$	$3D_H$	CAPCOM Register 29	0000_H
CC29IC b	$F184_H$ **E**	$C2_H$	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000_H
CC2IC b	$FF7C_H$	BE_H	CAPCOM Reg. 2 Interrupt Ctrl. Reg.	0000_H
CC3	$FE86_H$	43_H	CAPCOM Register 3	0000_H
CC30	$FE7C_H$	$3E_H$	CAPCOM Register 30	0000_H
CC30IC b	$F18C_H$ **E**	$C6_H$	CAPCOM Reg. 30 Interrupt Ctrl. Reg.	0000_H
CC31	$FE7E_H$	$3F_H$	CAPCOM Register 31	0000_H
CC31IC b	$F194_H$ **E**	CA_H	CAPCOM Reg. 31 Interrupt Ctrl. Reg.	0000_H
CC3IC b	$FF7E_H$	BF_H	CAPCOM Reg. 3 Interrupt Ctrl. Reg.	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
S0EIC	**b**	$FF70_H$		$B8_H$	Serial Chan. 0 Error Interrupt Ctrl. Reg.	0000_H
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Reg. (read only)	XX_H
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Reg. (write only)	00_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP		$FE12_H$		09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR		$F0B4_H$	**E**	$5A_H$	SSC Baudrate Register	0000_H
SSCCON	**b**	$FFB2_H$		$D9_H$	SSC Control Register	0000_H
SSCEIC	**b**	$FF76_H$		BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB		$F0B2_H$	**E**	59_H	SSC Receive Buffer	$XXXX_H$
SSCRIC	**b**	$FF74_H$		BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB		$F0B0_H$	**E**	58_H	SSC Transmit Buffer	0000_H
SSCTIC	**b**	$FF72_H$		$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV		$FE14_H$		$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN		$FE16_H$		$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON	**b**	$FF12_H$		89_H	CPU System Configuration Register	[1]$0xx0_H$
T0		$FE50_H$		28_H	CAPCOM Timer 0 Register	0000_H
T01CON	**b**	$FF50_H$		$A8_H$	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000_H
T0IC	**b**	$FF9C_H$		CE_H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000_H
T0REL		$FE54_H$		$2A_H$	CAPCOM Timer 0 Reload Register	0000_H
T1		$FE52_H$		29_H	CAPCOM Timer 1 Register	0000_H
T1IC	**b**	$FF9E_H$		CF_H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000_H
T1REL		$FE56_H$		$2B_H$	CAPCOM Timer 1 Reload Register	0000_H
T2		$FE40_H$		20_H	GPT1 Timer 2 Register	0000_H
T2CON	**b**	$FF40_H$		$A0_H$	GPT1 Timer 2 Control Register	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
T2IC	**b**	$FF60_H$		$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3		$FE42_H$		21_H	GPT1 Timer 3 Register	0000_H
T3CON	**b**	$FF42_H$		$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC	**b**	$FF62_H$		$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4		$FE44_H$		22_H	GPT1 Timer 4 Register	0000_H
T4CON	**b**	$FF44_H$		$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC	**b**	$FF64_H$		$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5		$FE46_H$		23_H	GPT2 Timer 5 Register	0000_H
T5CON	**b**	$FF46_H$		$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC	**b**	$FF66_H$		$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6		$FE48_H$		24_H	GPT2 Timer 6 Register	0000_H
T6CON	**b**	$FF48_H$		$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC	**b**	$FF68_H$		$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
T7		$F050_H$	**E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON	**b**	$FF20_H$		90_H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000_H
T7IC	**b**	$F17A_H$	**E**	BE_H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000_H
T7REL		$F054_H$	**E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H
T8		$F052_H$	**E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC	**b**	$F17C_H$	**E**	BF_H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000_H
T8REL		$F056_H$	**E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR	**b**	$FFAC_H$		$D6_H$	Trap Flag Register	0000_H
WDT		$FEAE_H$		57_H	Watchdog Timer Register (read only)	0000_H
WDTCON		$FFAE_H$		$D7_H$	Watchdog Timer Control Register	[2] $00XX_H$
XP0IC	**b**	$F186_H$	**E**	$C3_H$	CAN1 Module Interrupt Control Register	0000_H
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Unassigned Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Unassigned Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	PLL/OWD Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CR and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C167CR will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C167CR.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	0.2 V_{DD} - 0.1	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	0.3 V_{DD}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	2.0	V	–
Input high voltage (TTL, all except RSTIN and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage RSTIN (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	–	mV	Series resistance = 0 Ω
Output low voltage (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, CLKOUT, RSTOUT, RSTIN[2)])	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL} = 1.6 mA

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Output high voltage[3] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage[3] (all other outputs)	V_{OH1} CC	2.4	–	V	I_{OH} = -1.6 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)[4]	I_{OZ2} CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ inactive current[5]	I_{RSTH}[6]	–	-10	µA	V_{IN} = V_{IH1}
$\overline{RSTIN}$ active current[5]	I_{RSTL}[7]	-100	–	µA	V_{IN} = V_{IL}
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ inact. current[8]	I_{RWH}[6]	–	-40	µA	V_{OUT} = 2.4 V
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ active current[8]	I_{RWL}[7]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current[8]	I_{ALEL}[6]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current[8]	I_{ALEH}[7]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[8]	I_{P6H}[6]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current[8]	I_{P6L}[7]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current[9]	I_{P0H}[6]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L}[7]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[10] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz; T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) This parameter is not valid for pins $\overline{READY}$, ALE, $\overline{RD}$, and $\overline{WR}$ while the respective pull device is on.

5) These parameters describe the $\overline{RSTIN}$ pull-up, which equals a resistance of ca. 50 to 250 kΩ.

6) The maximum current may be drawn while the respective signal line remains inactive.

7) The minimum current must be drawn in order to drive the respective signal line active.

8) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{CS}$ output and the open drain function is not enabled. The $\overline{READY}$-pull-up is always active, except for Power-down mode.

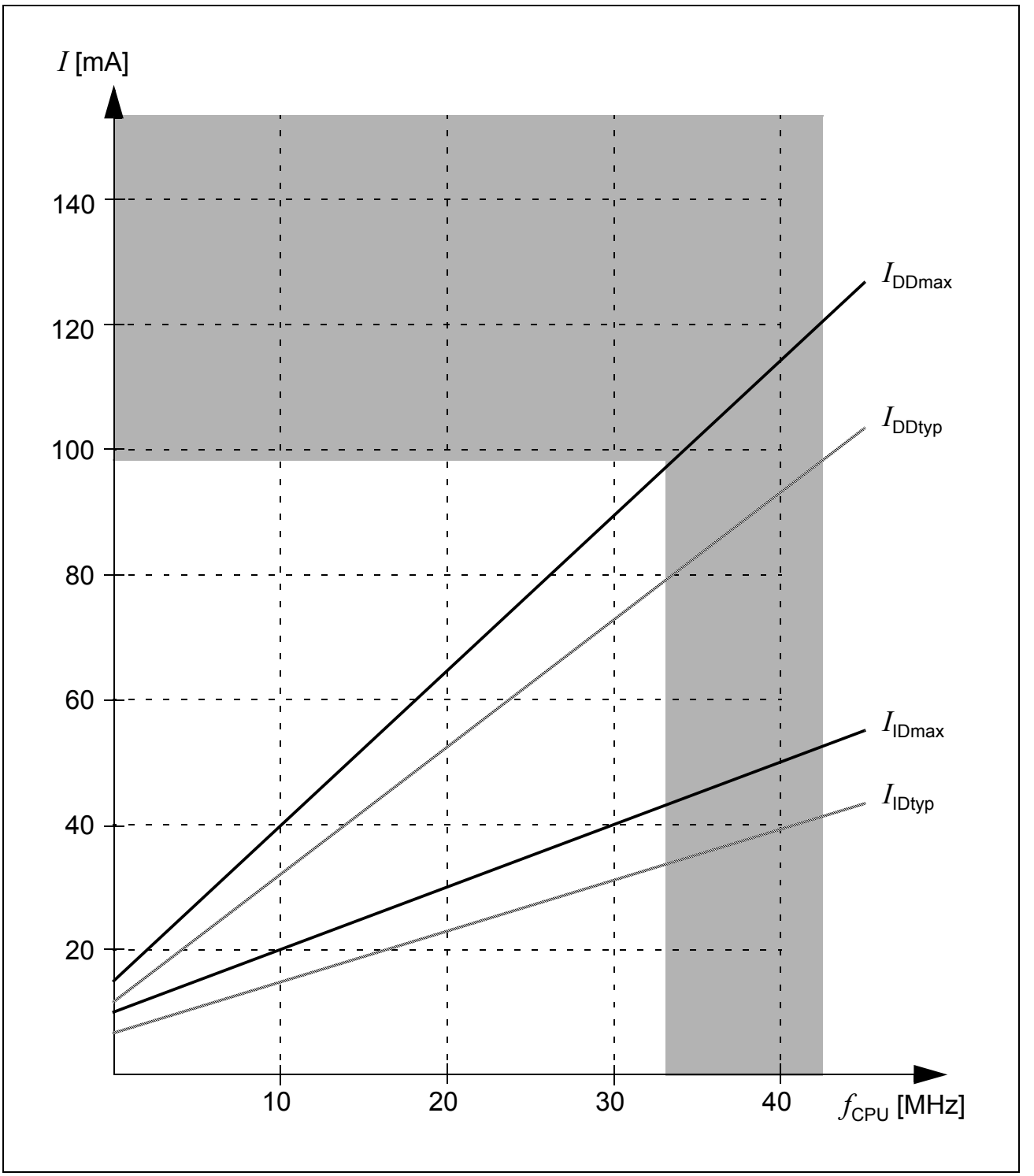

Figure 9 Supply/Idle Current as a Function of Operating Frequency

upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins P0.15-13 (P0H.7-5).

Table 15 associates the combinations of these three bits with the respective clock generation mode.

Table 15 C167CR Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[1)]	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 8.25 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 11 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 16.5 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 6.6 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 33 MHz	Direct drive[2)]
0 1 0	$f_{OSC} \times 1.5$	6.66 to 22 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 66 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 13.2 MHz	–

1) The external clock input range refers to a CPU clock range of 10 … 33 MHz (PLL operation).

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times$ **F**). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

General Notes for the Following Timing Figures

These standard notes apply to all subsequent timing figures. Additional individual notes are placed at the respective figure.

1. *The falling edge of signals $\overline{RD}$ and $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$/$\overline{WrCS}$ is controlled by the Read/Write delay feature (bit BUSCON.RWDCx).*
2. *A bus cycle is extended here, if MCTC waitstates are selected or if the $\overline{READY}$ input is sampled inactive.*
3. *A bus cycle is extended here, if an MTTC waitstate is selected.*

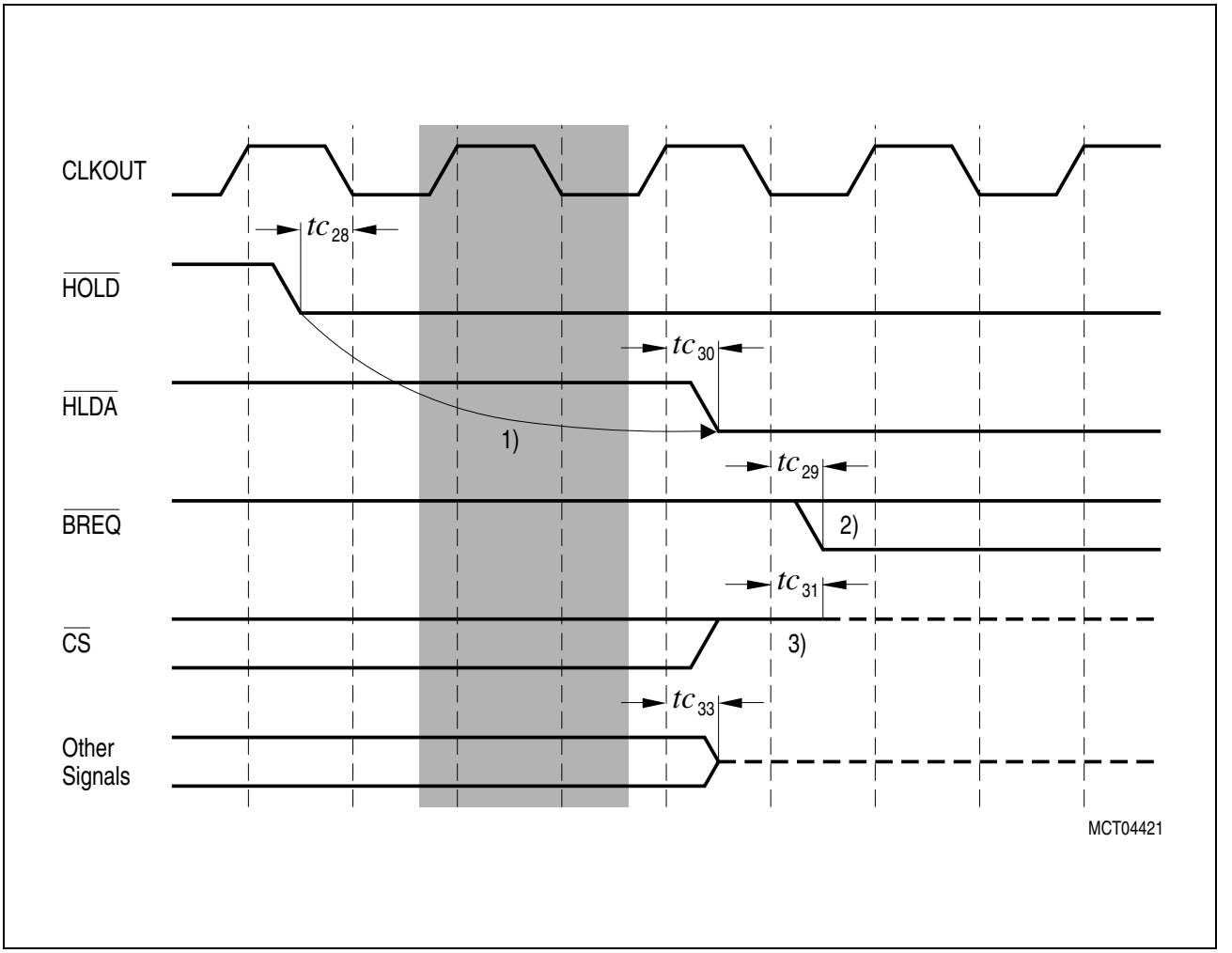

Figure 21 External Bus Arbitration, Releasing the Bus

Notes

1. *The C167CR will complete the currently running bus cycle before granting bus access.*
2. *This is the first possibility for $\overline{BREQ}$ to get active.*
3. *The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{33}. Latched $\overline{CS}$ outputs are driven high for 1 TCL before the output drivers are switched off.*

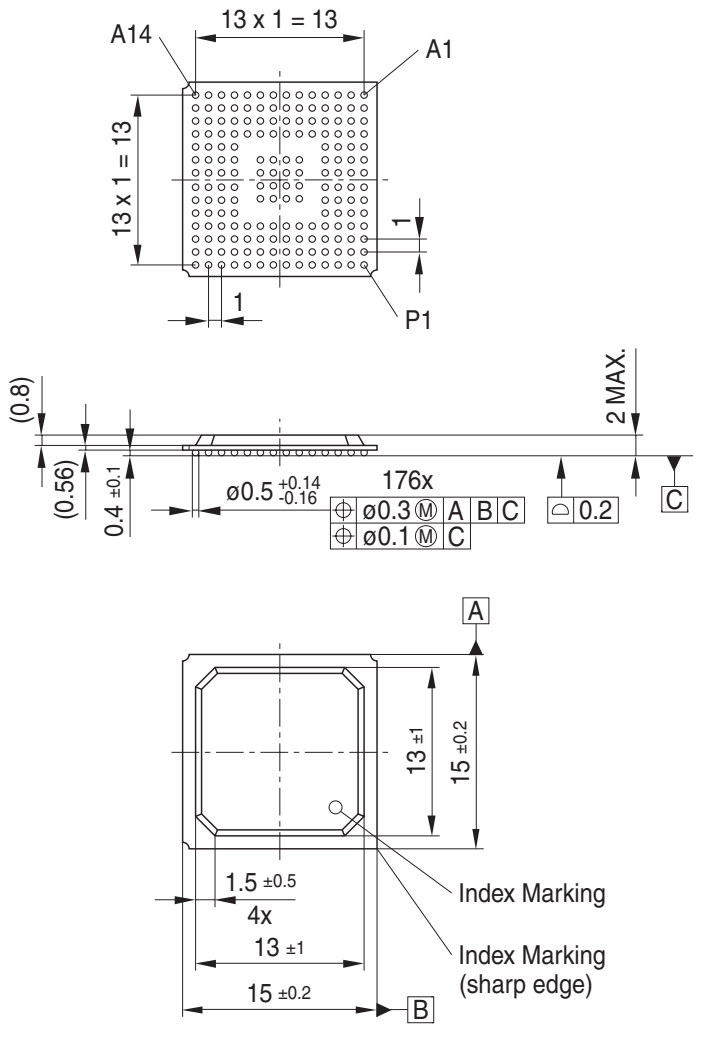

Figure 25 **P-BGA-176-2** (Plastic Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm