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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167srlmhabxuma2

2 General Device Information

2.1 Introduction

The C167CR derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 16.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

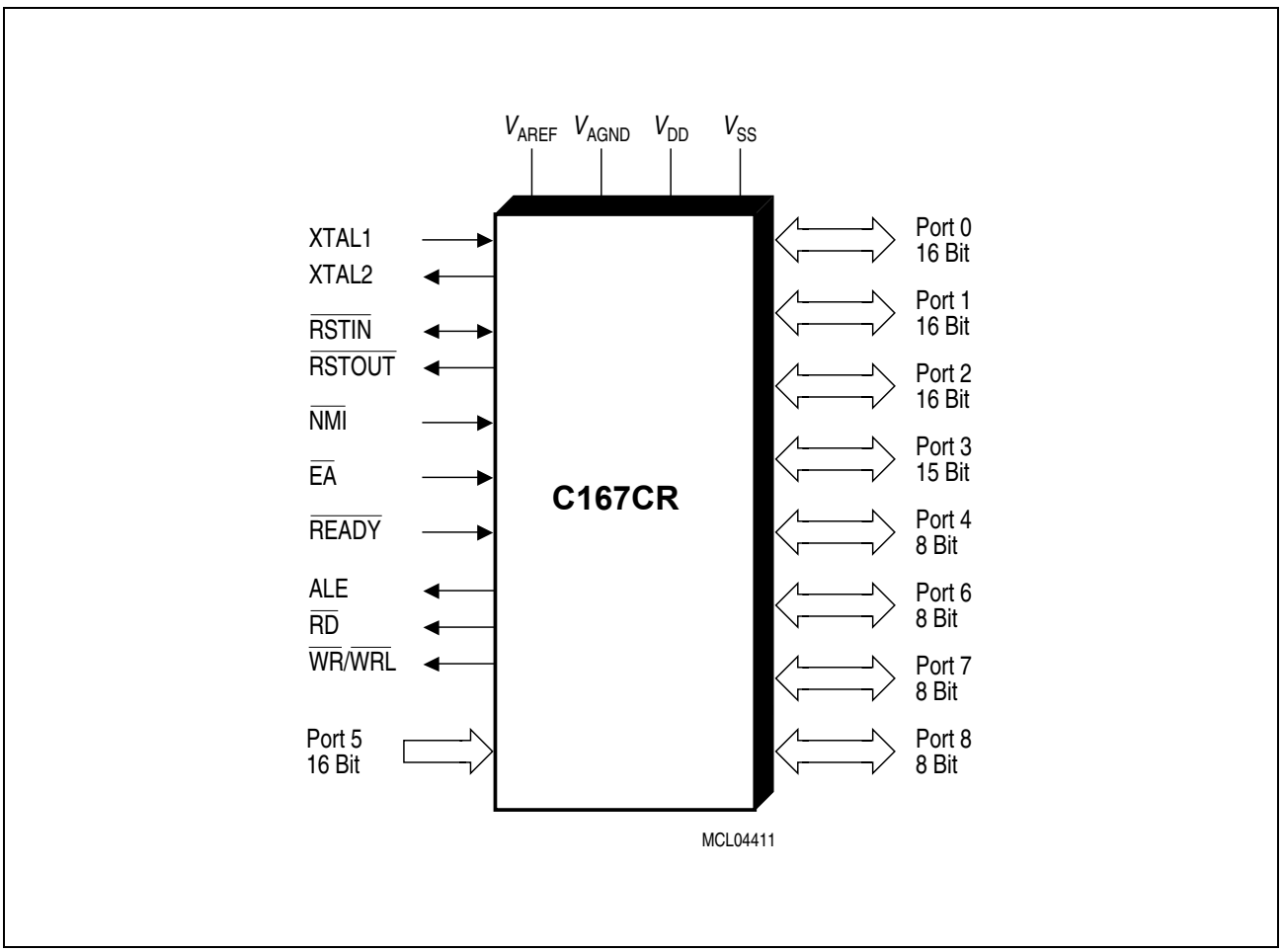


Figure 1 Logic Symbol

2.2 Pin Configuration and Definition for P-MQFP-144-8

The pins of the C167CR are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package.

*Note: The P-BGA-176-2 is described in **Table 3** and **Figure 3**.*

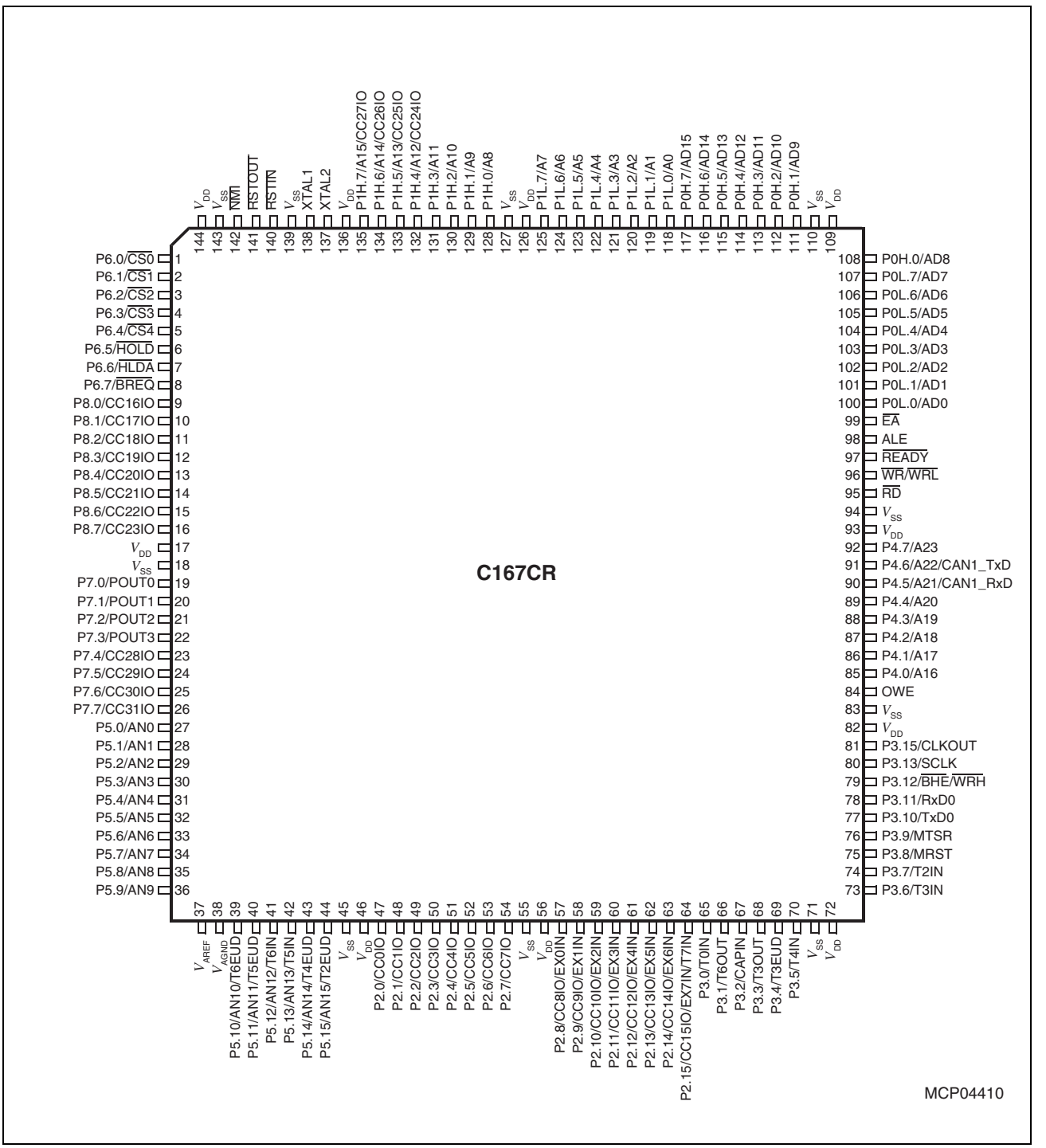


Figure 2 Pin Configuration P-MQFP-144-8 (top view)

Table 2 Pin Definitions and Functions P-MQFP-144-8

Symbol	Pin No.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	7	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	$\overline{BREQ}$ Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	9	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	11	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	12	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	D13 C13	O I	XTAL2: Output of the oscillator amplifier circuit. XTAL1: Input to the oscillator amplifier and input to the internal clock generator. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTOUT}}$	D12	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{RSTIN}}$	E11	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{EA}$	M9	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
$\overline{WR}$/ $\overline{WRL}$	N9	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	P9	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	P10	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	P6	O	A16 Least Significant Segment Address Line
P4.1	M6	O	A17 Segment Address Line
P4.2	L6	O	A18 Segment Address Line
P4.3	N7	O	A19 Segment Address Line
P4.4	P7	O	A20 Segment Address Line
P4.5	M7	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	L7	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	N8	O	A23 Most Significant Segment Address Line

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	F3	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	F2	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	F4	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	G4	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	G3	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	G2	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	G1	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	H1	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	H4	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	J1	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	J2	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	J4	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	J3	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	K1	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	K2	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	L1	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input
V_{AREF}	B2	–	Reference voltage for the A/D converter.	
V_{AGND}	C2	–	Reference ground for the A/D converter.	

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C167CR offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 Mbytes of external memory space, this address space can be restricted to 1 Mbyte, 256 Kbyte, or to 64 Kbyte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 Mbytes is used.

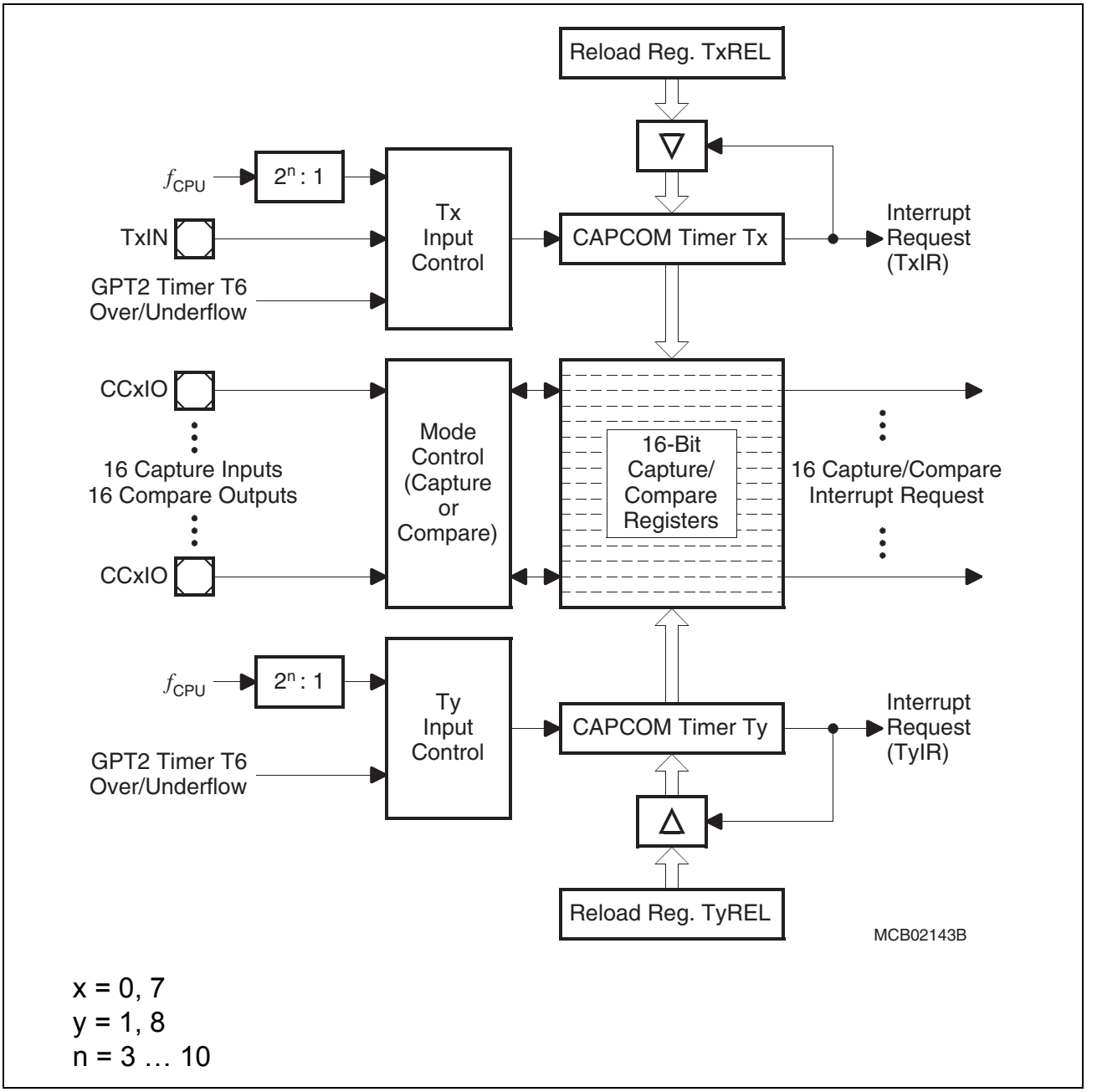


Figure 6 CAPCOM Unit Block Diagram

3.6 PWM Module

The Pulse Width Modulation Module can generate up to four PWM output signals using edge-aligned or center-aligned PWM. In addition the PWM module can generate PWM burst signals and single shot outputs. The frequency range of the PWM signals covers 4 Hz to 16.5 MHz (referred to a CPU clock of 33 MHz), depending on the resolution of the PWM output signal. The level of the output signals is selectable and the PWM module can generate interrupt requests.

3.12 Parallel Ports

The C167CR provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 6, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 Kbytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output (CLKOUT).
Port 5 is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) of the C167CR's port drivers can be selected via the Port Driver Control Register (PDCR). Two bits select fast edges ('0') or reduced edges ('1') for bus interface pins and non-bus pins separately.
PDCR.0 = BIPEC controls PORT0, PORT1, Port 4, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE, CLKOUT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$.
PDCR.4 = NBPEC controls Port 3, Port 8, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$ (bidir. reset mode).

Table 7 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4

3.15 Special Function Registers Overview

The following table lists all SFRs which are implemented in the C167CR in alphabetical order.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Note: Registers within device specific interface modules (CAN) are only present in the corresponding device, of course.

Table 8 C167CR Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	–	CAN1 Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	–	CAN1 Control / Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	–	CAN1 Global Mask Short	$UFUU_H$

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
C1IR	$EF02_H$ **X**	–	CAN1 Interrupt Register	XX_H
C1LGML	$EF0A_H$ **X**	–	CAN1 Lower Global Mask Long	$UUUU_H$
C1LMLM	$EF0E_H$ **X**	–	CAN1 Lower Mask of Last Message	$UUUU_H$
C1UAR	$EFn2_H$ **X**	–	CAN1 Upper Arbitration Register (message **n**)	$UUUU_H$
C1UGML	$EF08_H$ **X**	–	CAN1 Upper Global Mask Long	$UUUU_H$
C1UMLM	$EF0C_H$ **X**	–	CAN1 Upper Mask of Last Message	$UUUU_H$
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC0	$FE80_H$	40_H	CAPCOM Register 0	0000_H
CC0IC **b**	$FF78_H$	BC_H	CAPCOM Register 0 Interrupt Ctrl. Reg.	0000_H
CC1	$FE82_H$	41_H	CAPCOM Register 1	0000_H
CC10	$FE94_H$	$4A_H$	CAPCOM Register 10	0000_H
CC10IC **b**	$FF8C_H$	$C6_H$	CAPCOM Reg. 10 Interrupt Ctrl. Reg.	0000_H
CC11	$FE96_H$	$4B_H$	CAPCOM Register 11	0000_H
CC11IC **b**	$FF8E_H$	$C7_H$	CAPCOM Reg. 11 Interrupt Ctrl. Reg.	0000_H
CC12	$FE98_H$	$4C_H$	CAPCOM Register 12	0000_H
CC12IC **b**	$FF90_H$	$C8_H$	CAPCOM Reg. 12 Interrupt Ctrl. Reg.	0000_H
CC13	$FE9A_H$	$4D_H$	CAPCOM Register 13	0000_H
CC13IC **b**	$FF92_H$	$C9_H$	CAPCOM Reg. 13 Interrupt Ctrl. Reg.	0000_H
CC14	$FE9C_H$	$4E_H$	CAPCOM Register 14	0000_H
CC14IC **b**	$FF94_H$	CA_H	CAPCOM Reg. 14 Interrupt Ctrl. Reg.	0000_H
CC15	$FE9E_H$	$4F_H$	CAPCOM Register 15	0000_H
CC15IC **b**	$FF96_H$	CB_H	CAPCOM Reg. 15 Interrupt Ctrl. Reg.	0000_H
CC16	$FE60_H$	30_H	CAPCOM Register 16	0000_H
CC16IC **b**	$F160_H$ **E**	$B0_H$	CAPCOM Reg. 16 Interrupt Ctrl. Reg.	0000_H
CC17	$FE62_H$	31_H	CAPCOM Register 17	0000_H
CC17IC **b**	$F162_H$ **E**	$B1_H$	CAPCOM Reg. 17 Interrupt Ctrl. Reg.	0000_H
CC18	$FE64_H$	32_H	CAPCOM Register 18	0000_H
CC18IC **b**	$F164_H$ **E**	$B2_H$	CAPCOM Reg. 18 Interrupt Ctrl. Reg.	0000_H
CC19	$FE66_H$	33_H	CAPCOM Register 19	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC19IC b	$F166_H$ **E**	$B3_H$	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000_H
CC1IC b	$FF7A_H$	BD_H	CAPCOM Reg. 1 Interrupt Ctrl. Reg.	0000_H
CC2	$FE84_H$	42_H	CAPCOM Register 2	0000_H
CC20	$FE68_H$	34_H	CAPCOM Register 20	0000_H
CC20IC b	$F168_H$ **E**	$B4_H$	CAPCOM Reg. 20 Interrupt Ctrl. Reg.	0000_H
CC21	$FE6A_H$	35_H	CAPCOM Register 21	0000_H
CC21IC b	$F16A_H$ **E**	$B5_H$	CAPCOM Reg. 21 Interrupt Ctrl. Reg.	0000_H
CC22	$FE6C_H$	36_H	CAPCOM Register 22	0000_H
CC22IC b	$F16C_H$ **E**	$B6_H$	CAPCOM Reg. 22 Interrupt Ctrl. Reg.	0000_H
CC23	$FE6E_H$	37_H	CAPCOM Register 23	0000_H
CC23IC b	$F16E_H$ **E**	$B7_H$	CAPCOM Reg. 23 Interrupt Ctrl. Reg.	0000_H
CC24	$FE70_H$	38_H	CAPCOM Register 24	0000_H
CC24IC b	$F170_H$ **E**	$B8_H$	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000_H
CC25	$FE72_H$	39_H	CAPCOM Register 25	0000_H
CC25IC b	$F172_H$ **E**	$B9_H$	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000_H
CC26	$FE74_H$	$3A_H$	CAPCOM Register 26	0000_H
CC26IC b	$F174_H$ **E**	BA_H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000_H
CC27	$FE76_H$	$3B_H$	CAPCOM Register 27	0000_H
CC27IC b	$F176_H$ **E**	BB_H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000_H
CC28	$FE78_H$	$3C_H$	CAPCOM Register 28	0000_H
CC28IC b	$F178_H$ **E**	BC_H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000_H
CC29	$FE7A_H$	$3D_H$	CAPCOM Register 29	0000_H
CC29IC b	$F184_H$ **E**	$C2_H$	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000_H
CC2IC b	$FF7C_H$	BE_H	CAPCOM Reg. 2 Interrupt Ctrl. Reg.	0000_H
CC3	$FE86_H$	43_H	CAPCOM Register 3	0000_H
CC30	$FE7C_H$	$3E_H$	CAPCOM Register 30	0000_H
CC30IC b	$F18C_H$ **E**	$C6_H$	CAPCOM Reg. 30 Interrupt Ctrl. Reg.	0000_H
CC31	$FE7E_H$	$3F_H$	CAPCOM Register 31	0000_H
CC31IC b	$F194_H$ **E**	CA_H	CAPCOM Reg. 31 Interrupt Ctrl. Reg.	0000_H
CC3IC b	$FF7E_H$	BF_H	CAPCOM Reg. 3 Interrupt Ctrl. Reg.	0000_H

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 33 MHz
		2.5[1]	5.5	V	Power Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2][3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3]
External Load Capacitance	C_L	–	50	pF	Pin drivers in **fast edge** mode (PDCR.BIPEC = '0')
		–	30	pF	Pin drivers in **reduced edge** mode (PDCR.BIPEC = '1')[3]
		–	100	pF	Pin drivers in **fast edge** mode, f_{CPUmax} = 25 MHz[4]
Ambient temperature	T_A	0	70	°C	SAB-C167CR …
		-40	85	°C	SAF-C167CR …
		-40	125	°C	SAK-C167CR …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not subject to production test - verified by design/characterization.

4) The increased capacitive load is valid for the 25 MHz-derivatives up to a CPU clock frequency of 25 MHz. Under these circumstances the timing parameters as specified in the "C167CR Data Sheet 1999-06" are valid.

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Output high voltage[3] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage[3] (all other outputs)	V_{OH1} CC	2.4	–	V	I_{OH} = -1.6 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)[4]	I_{OZ2} CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ inactive current[5]	I_{RSTH}[6]	–	-10	µA	V_{IN} = V_{IH1}
$\overline{RSTIN}$ active current[5]	I_{RSTL}[7]	-100	–	µA	V_{IN} = V_{IL}
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ inact. current[8]	I_{RWH}[6]	–	-40	µA	V_{OUT} = 2.4 V
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ active current[8]	I_{RWL}[7]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current[8]	I_{ALEL}[6]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current[8]	I_{ALEH}[7]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[8]	I_{P6H}[6]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current[8]	I_{P6L}[7]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current[9]	I_{P0H}[6]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L}[7]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[10] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz; T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) This parameter is not valid for pins $\overline{READY}$, ALE, $\overline{RD}$, and $\overline{WR}$ while the respective pull device is on.

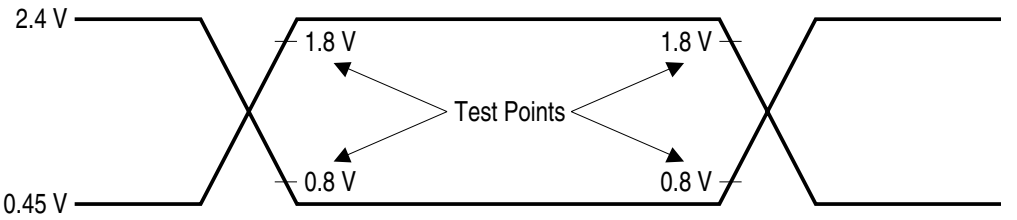
5) These parameters describe the $\overline{RSTIN}$ pull-up, which equals a resistance of ca. 50 to 250 kΩ.

6) The maximum current may be drawn while the respective signal line remains inactive.

7) The minimum current must be drawn in order to drive the respective signal line active.

8) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{CS}$ output and the open drain function is not enabled. The $\overline{READY}$-pull-up is always active, except for Power-down mode.

4.4.3 Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.45 V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

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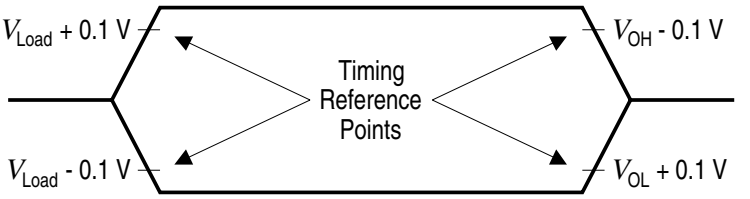
Figure 13 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

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Figure 14 Float Waveforms

4.4.4 External Bus Timing

Table 17 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	30[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter.
For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for f_{CPU} > 25 MHz).
For longer periods the relative deviation decreases (see PLL deviation formula).

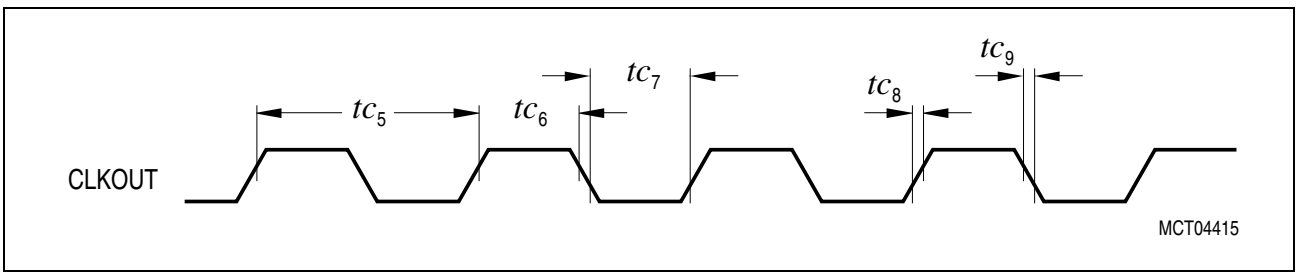

Figure 15 CLKOUT Signal Timing

Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

Table 18 Variable Memory Cycles

Bus Cycle Type	Bus Cycle Duration	Unit	25/33 MHz, 0 Waitstates
Demultiplexed bus cycle with normal ALE	4 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	80 ns/60.6 ns
Demultiplexed bus cycle with extended ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with normal ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns/90.9 ns
Multiplexed bus cycle with extended ALE	8 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	160 ns/121.2 ns

General Notes for the Following Timing Figures

These standard notes apply to all subsequent timing figures. Additional individual notes are placed at the respective figure.

1. *The falling edge of signals $\overline{RD}$ and $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$/$\overline{WrCS}$ is controlled by the Read/Write delay feature (bit BUSCON.RWDCx).*
2. *A bus cycle is extended here, if MCTC waitstates are selected or if the $\overline{READY}$ input is sampled inactive.*
3. *A bus cycle is extended here, if an MTTC waitstate is selected.*

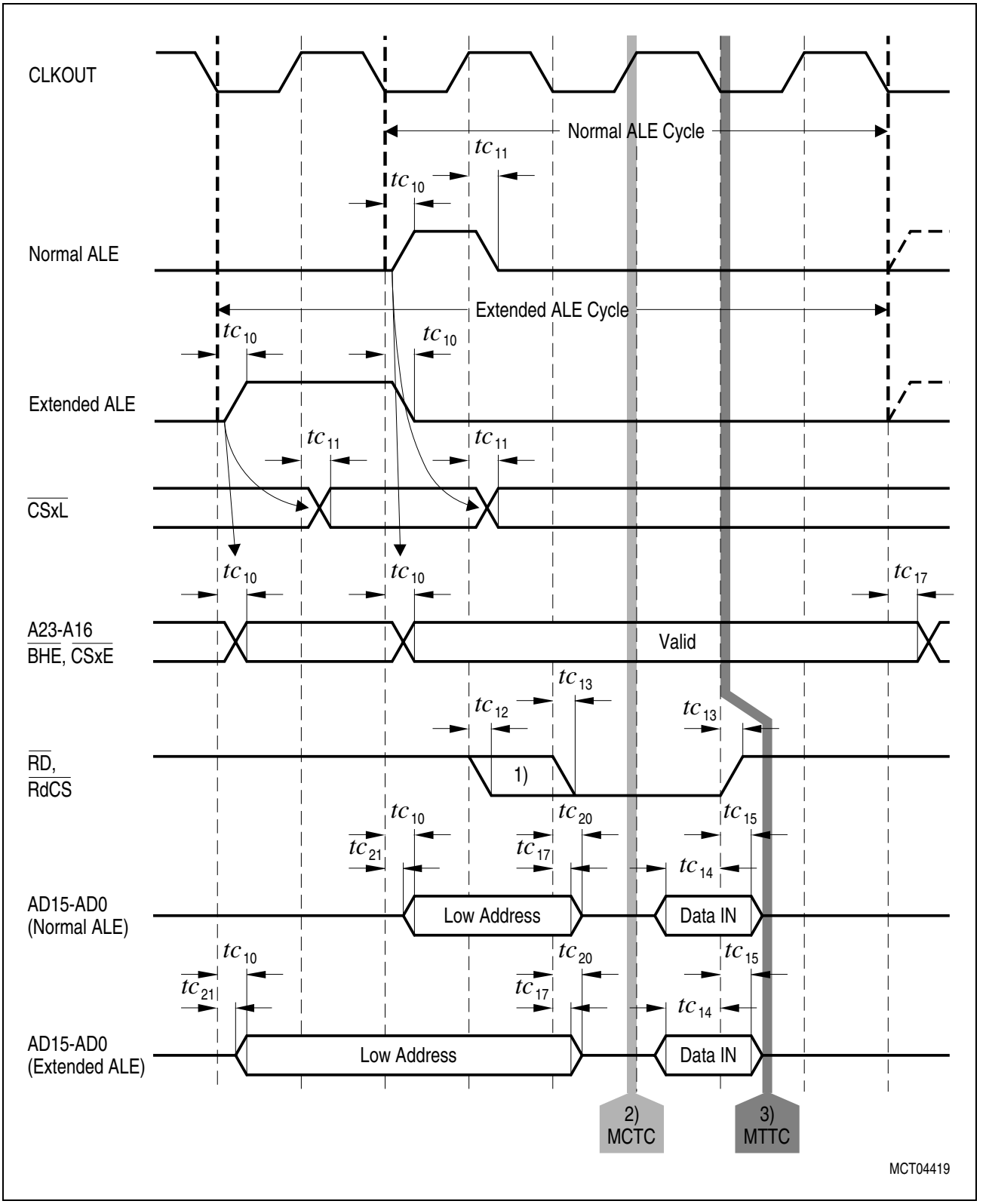

Figure 19 Multiplexed Bus, Read Access

5 Package Outlines

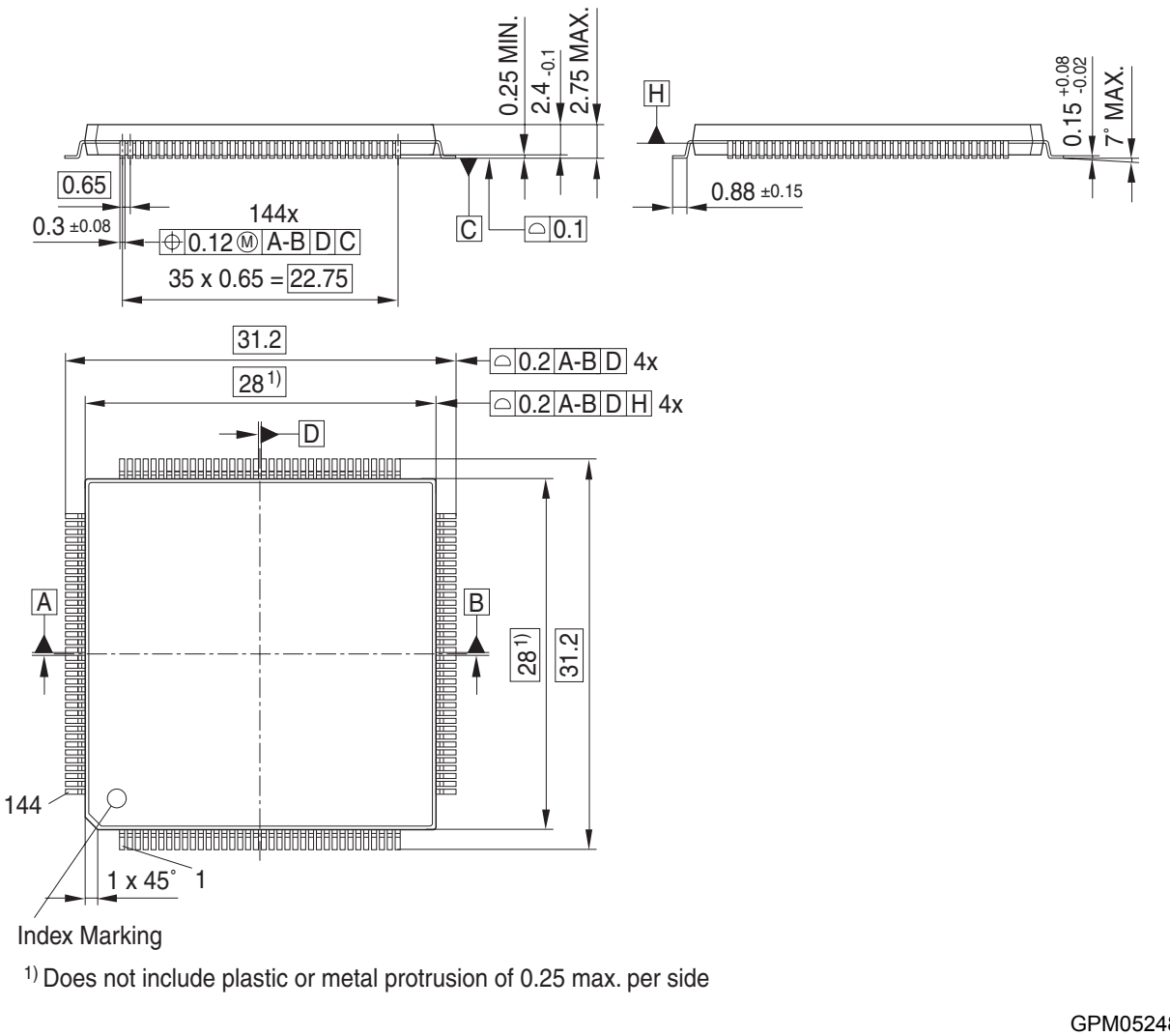

Figure 24 **P-MQFP-144-8** (Plastic Metric Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm