Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167srlmhakxqla2

Table of Contents

Table 2 Pin Definitions and Functions P-MQFP-144-8

Symbol	Pin No.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	7	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	$\overline{BREQ}$ Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	9	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	11	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	12	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	47	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	48	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	49	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	50	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	51	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	52	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	53	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	54	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	57	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	58	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	59	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	60	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	61	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	62	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	63	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	64	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
OWE (V_{PP})	84	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Table 3 Pin Definitions and Functions P-BGA-176-2

Symbol	Pin Num.	Input Outp.	Function
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	A5	I	AN0
P5.1	D5	I	AN1
P5.2	A4	I	AN2
P5.3	C5	I	AN3
P5.4	B4	I	AN4
P5.5	A3	I	AN5
P5.6	C4	I	AN6
P5.7	D4	I	AN7
P5.8	B3	I	AN8
P5.9	C3	I	AN9
P5.10	D3	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	C1	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	D1	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	D2	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	E3	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	E2	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	D7	O	POUT0 PWM Channel 0 Output
P7.1	C7	O	POUT1 PWM Channel 1 Output
P7.2	B7	O	POUT2 PWM Channel 2 Output
P7.3	A7	O	POUT3 PWM Channel 3 Output
P7.4	D6	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	C6	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	B6	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	A6	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{EA}$	M9	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
$\overline{WR}$/ $\overline{WRL}$	N9	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	P9	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	P10	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	P6	O	A16 Least Significant Segment Address Line
P4.1	M6	O	A17 Segment Address Line
P4.2	L6	O	A18 Segment Address Line
P4.3	N7	O	A19 Segment Address Line
P4.4	P7	O	A20 Segment Address Line
P4.5	M7	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	L7	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	N8	O	A23 Most Significant Segment Address Line

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C167CR offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 Mbytes of external memory space, this address space can be restricted to 1 Mbyte, 256 Kbyte, or to 64 Kbyte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 Mbytes is used.

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C167CR instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

The C167CR also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	$00'0000_H$	00_H	III
• Software Reset		RESET	$00'0000_H$	00_H	III
• W-dog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
• Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
• Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
• Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved	–	–	$[2C_H - 3C_H]$	$[0B_H - 0F_H]$	–
Software Traps • TRAP Instruction	–	–	Any $[00'0000_H - 00'01FC_H]$ in steps of 4_H	Any $[00_H - 7F_H]$	Current CPU Priority

Table 6 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

3.12 Parallel Ports

The C167CR provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 6, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 Kbytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output (CLKOUT).
Port 5 is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) of the C167CR's port drivers can be selected via the Port Driver Control Register (PDCR). Two bits select fast edges ('0') or reduced edges ('1') for bus interface pins and non-bus pins separately.
PDCR.0 = BIPEC controls PORT0, PORT1, Port 4, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE, CLKOUT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$.
PDCR.4 = NBPEC controls Port 3, Port 8, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$ (bidir. reset mode).

3.14 Instruction Set Summary

Table 7 lists the instructions of the C167CR in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C166 Family Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 7 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16 × 16 bits)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16 / 16 bits)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32 / 16 bits)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DP7	**b**	$FFD2_H$		$E9_H$	Port 7 Direction Control Register	00_H
DP8	**b**	$FFD6_H$		EB_H	Port 8 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7	**b**	$F1D2_H$	**E**	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8	**b**	$F1D6_H$	**E**	EB_H	Port 8 Open Drain Control Register	00_H
ONES		$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
P7	**b**	$FFD0_H$		$E8_H$	Port 7 Register (8 bits)	00_H
P8	**b**	$FFD4_H$		EA_H	Port 8 Register (8 bits)	00_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
S0EIC	**b**	$FF70_H$		$B8_H$	Serial Chan. 0 Error Interrupt Ctrl. Reg.	0000_H
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Reg. (read only)	XX_H
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Reg. (write only)	00_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP		$FE12_H$		09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR		$F0B4_H$	**E**	$5A_H$	SSC Baudrate Register	0000_H
SSCCON	**b**	$FFB2_H$		$D9_H$	SSC Control Register	0000_H
SSCEIC	**b**	$FF76_H$		BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB		$F0B2_H$	**E**	59_H	SSC Receive Buffer	$XXXX_H$
SSCRIC	**b**	$FF74_H$		BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB		$F0B0_H$	**E**	58_H	SSC Transmit Buffer	0000_H
SSCTIC	**b**	$FF72_H$		$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV		$FE14_H$		$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN		$FE16_H$		$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON	**b**	$FF12_H$		89_H	CPU System Configuration Register	[1]$0xx0_H$
T0		$FE50_H$		28_H	CAPCOM Timer 0 Register	0000_H
T01CON	**b**	$FF50_H$		$A8_H$	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000_H
T0IC	**b**	$FF9C_H$		CE_H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000_H
T0REL		$FE54_H$		$2A_H$	CAPCOM Timer 0 Reload Register	0000_H
T1		$FE52_H$		29_H	CAPCOM Timer 1 Register	0000_H
T1IC	**b**	$FF9E_H$		CF_H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000_H
T1REL		$FE56_H$		$2B_H$	CAPCOM Timer 1 Reload Register	0000_H
T2		$FE40_H$		20_H	GPT1 Timer 2 Register	0000_H
T2CON	**b**	$FF40_H$		$A0_H$	GPT1 Timer 2 Control Register	0000_H

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 33 MHz
		2.5[1]	5.5	V	Power Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2][3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3]
External Load Capacitance	C_L	–	50	pF	Pin drivers in **fast edge** mode (PDCR.BIPEC = '0')
		–	30	pF	Pin drivers in **reduced edge** mode (PDCR.BIPEC = '1')[3]
		–	100	pF	Pin drivers in **fast edge** mode, f_{CPUmax} = 25 MHz[4]
Ambient temperature	T_A	0	70	°C	SAB-C167CR …
		-40	85	°C	SAF-C167CR …
		-40	125	°C	SAK-C167CR …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not subject to production test - verified by design/characterization.

4) The increased capacitive load is valid for the 25 MHz-derivatives up to a CPU clock frequency of 25 MHz. Under these circumstances the timing parameters as specified in the "C167CR Data Sheet 1999-06" are valid.

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Output high voltage[3] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage[3] (all other outputs)	V_{OH1} CC	2.4	–	V	I_{OH} = -1.6 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)[4]	I_{OZ2} CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ inactive current[5]	I_{RSTH}[6]	–	-10	µA	V_{IN} = V_{IH1}
$\overline{RSTIN}$ active current[5]	I_{RSTL}[7]	-100	–	µA	V_{IN} = V_{IL}
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ inact. current[8]	I_{RWH}[6]	–	-40	µA	V_{OUT} = 2.4 V
$\overline{READY}$/$\overline{RD}$/$\overline{WR}$ active current[8]	I_{RWL}[7]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current[8]	I_{ALEL}[6]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current[8]	I_{ALEH}[7]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[8]	I_{P6H}[6]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current[8]	I_{P6L}[7]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current[9]	I_{P0H}[6]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L}[7]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[10] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz; T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) This parameter is not valid for pins $\overline{READY}$, ALE, $\overline{RD}$, and $\overline{WR}$ while the respective pull device is on.

5) These parameters describe the $\overline{RSTIN}$ pull-up, which equals a resistance of ca. 50 to 250 kΩ.

6) The maximum current may be drawn while the respective signal line remains inactive.

7) The minimum current must be drawn in order to drive the respective signal line active.

8) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{CS}$ output and the open drain function is not enabled. The $\overline{READY}$-pull-up is always active, except for Power-down mode.

4.3 Analog/Digital Converter Parameters

Table 13 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2 t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} + 0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not subject to production test - verified by design/characterization.

Table 19 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Output delay from CLKOUT falling edge Valid for: address, BHE, early CS, write data out, ALE	tc_{10}	CC	-2	11	ns
Output delay from CLKOUT rising edge Valid for: latched CS, ALE low	tc_{11}	CC	-2	6	ns
Output delay from CLKOUT rising edge Valid for: WR low (no RW delay), RD low (no RW delay)	tc_{12}	CC	-2	8	ns
Output delay from CLKOUT falling edge Valid for: RD/WR low (with RW delay), RD high (with RW delay)	tc_{13}	CC	-2	6	ns
Input setup time to CLKOUT falling edge Valid for: read data in	tc_{14}	SR	14	–	ns
Input hold time after CLKOUT falling edge Valid for: read data in[1)]	tc_{15}	SR	0	–	ns
Output hold time after CLKOUT falling edge Valid for: address, BHE, early CS[2)]	tc_{17}	CC	-2	6	ns
Output hold time after CLKOUT edge[3)] Valid for: write data out	tc_{18}	CC	-2	–	ns
Output delay from CLKOUT falling edge Valid for: WR high	tc_{19}	CC	-2	4	ns
Turn off delay after CLKOUT edge[3)] Valid for: write data out	tc_{20}	CC	–	7	ns
Turn on delay after CLKOUT falling edge[3)] Valid for: write data out	tc_{21}	CC	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore the read data may be removed immediately after the rising edge of RD. Address changes before the end of RD have also no impact on (demultiplexed) read cycles.

2) Due to comparable propagation delays (at comparable capacitive loads) the address does not change before WR goes high. The minimum output delay (tc_{17min}) is therefore the actual value of tc_{19}.

3) Not subject to production test - verified by design/characterization.

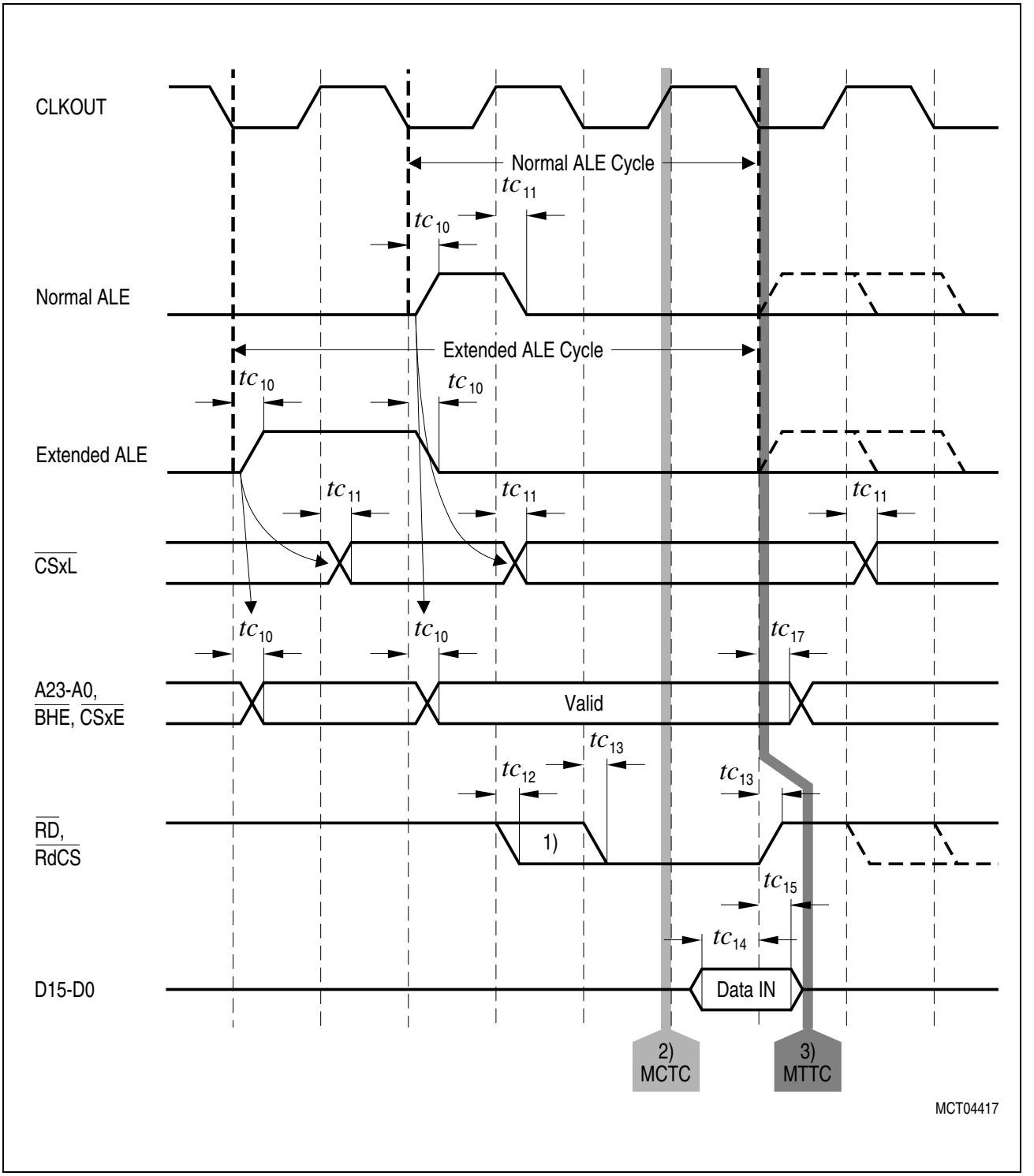

Figure 17 Demultiplexed Bus, Read Access