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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sab-c167cr-16rm-ha

Revision History:	**2005-02**	V3.3
Previous Version:	V3.2, 2001-07 V3.1, 2000-04 V3.0, 2000-02 1999-10 (Introduction of clock-related timing) 1999-06 1999-03 (Summarizes and replaces all older docs) 1998-03 (C167SR/CR, 25 MHz Addendum) 07.97 / 12.96 (C167CR-4RM) 12.96 (C167CR-16RM) 06.95 (C167CR, C167SR) 06.94 / 05.93 (C167)	

Page	Subjects (major changes since last revision)
all	The layout of several graphics and text structures has been adapted to company documentation rules, obvious typographical errors have been corrected.
all	The contents of this document have been re-arranged into numbered sections and a table of contents has been added.
6	BGA-type added to product list
8	Pin designation corrected (pin 78)
9	Input threshold control added to Port 6
17 ... 25	Pin diagram and pin description for BGA package added
45	Port 6 added to input-threshold controlled ports
85	Mechanical package drawing corrected (P-MQFP-144-8)
86	Mechanical package drawing added (P-BGA-176-2)

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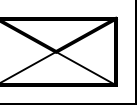

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
OWE (V_{PP})	84	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	85	O	A16 Least Significant Segment Address Line
P4.1	86	O	A17 Segment Address Line
P4.2	87	O	A18 Segment Address Line
P4.3	88	O	A19 Segment Address Line
P4.4	89	O	A20 Segment Address Line
P4.5	90	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	91	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	92	O	A23 Most Significant Segment Address Line
RD	95	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	96	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	D13 C13	O I	XTAL2: Output of the oscillator amplifier circuit. XTAL1: Input to the oscillator amplifier and input to the internal clock generator. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTOUT}}$	D12	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{RSTIN}}$	E11	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CR's instructions can be executed in just one machine cycle which requires 60 ns at 33 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

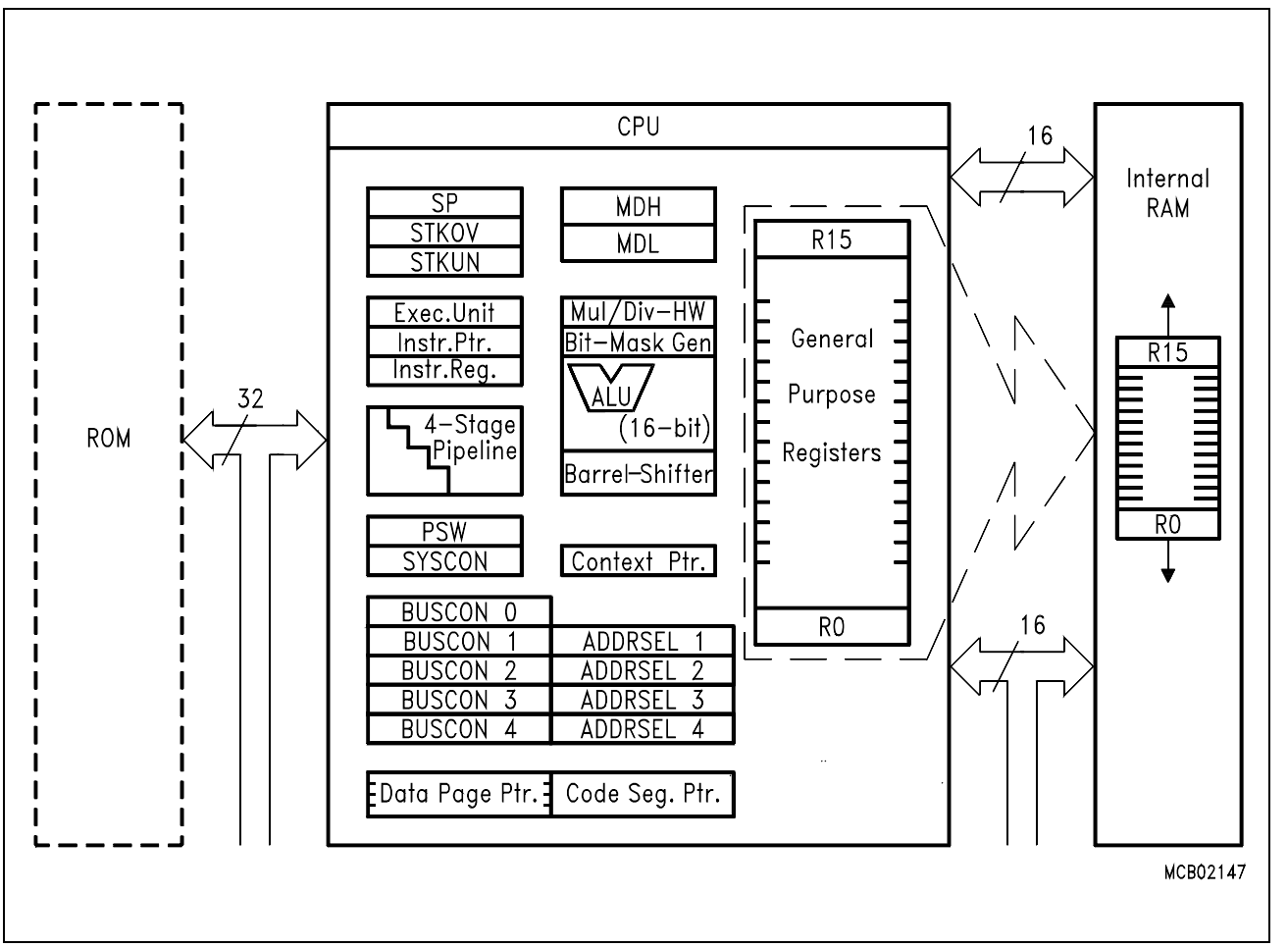

Figure 5 CPU Block Diagram

Table 4 C167CR Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H

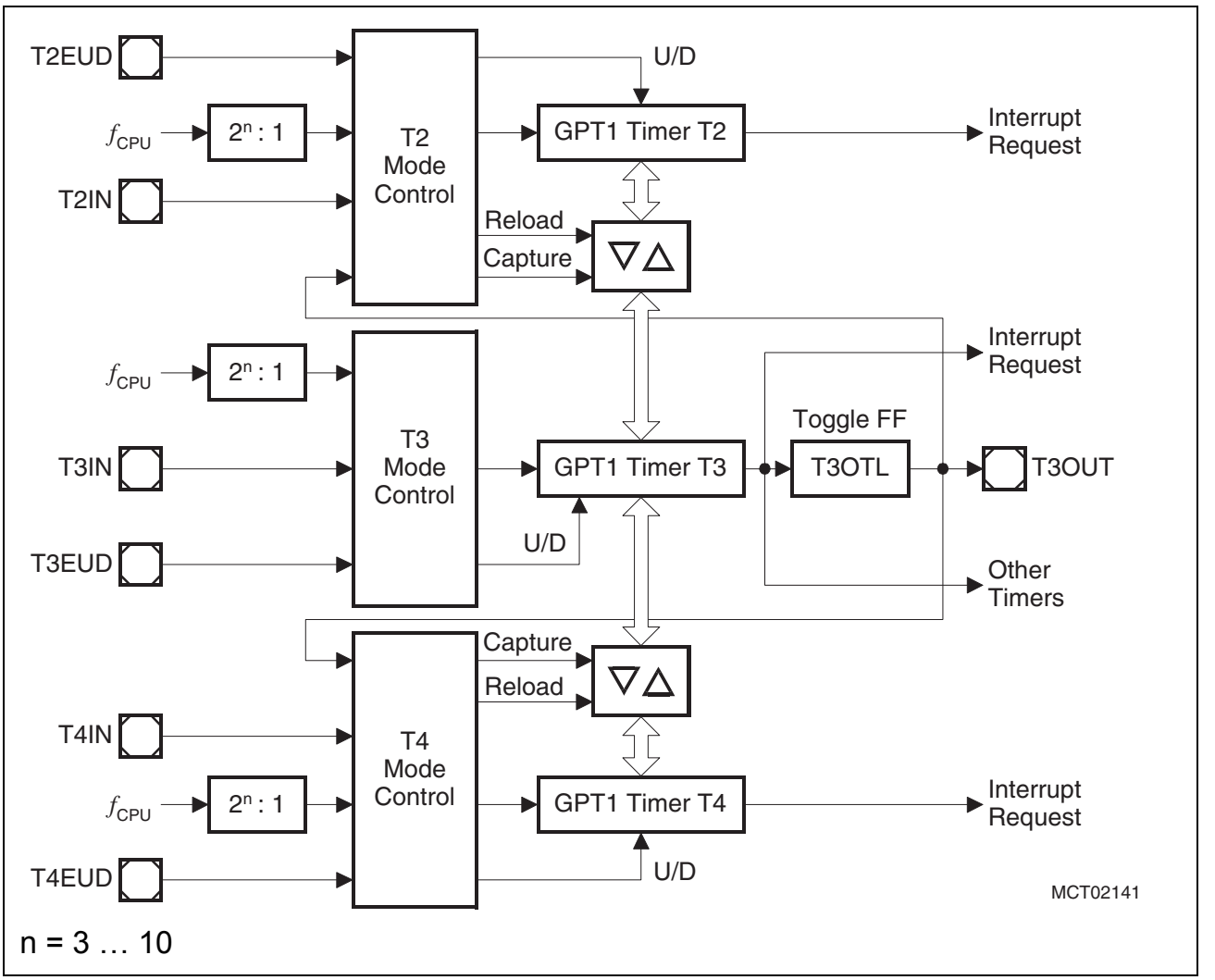

Figure 7 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C167CR to measure absolute time differences or to perform pulse multiplication without software overhead.

Table 7 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
CC4		$FE88_H$		44_H	CAPCOM Register 4	0000_H
CC4IC	**b**	$FF80_H$		$C0_H$	CAPCOM Reg. 4 Interrupt Ctrl. Reg.	0000_H
CC5		$FE8A_H$		45_H	CAPCOM Register 5	0000_H
CC5IC	**b**	$FF82_H$		$C1_H$	CAPCOM Register 5 Interrupt Ctrl. Reg.	0000_H
CC6		$FE8C_H$		46_H	CAPCOM Register 6	0000_H
CC6IC	**b**	$FF84_H$		$C2_H$	CAPCOM Reg. 6 Interrupt Ctrl. Reg.	0000_H
CC7		$FE8E_H$		47_H	CAPCOM Register 7	0000_H
CC7IC	**b**	$FF86_H$		$C3_H$	CAPCOM Reg. 7 Interrupt Ctrl. Reg.	0000_H
CC8		$FE90_H$		48_H	CAPCOM Register 8	0000_H
CC8IC	**b**	$FF88_H$		$C4_H$	CAPCOM Reg. 8 Interrupt Ctrl. Reg.	0000_H
CC9		$FE92_H$		49_H	CAPCOM Register 9	0000_H
CC9IC	**b**	$FF8A_H$		$C5_H$	CAPCOM Reg. 9 Interrupt Ctrl. Reg.	0000_H
CCM0	**b**	$FF52_H$		$A9_H$	CAPCOM Mode Control Register 0	0000_H
CCM1	**b**	$FF54_H$		AA_H	CAPCOM Mode Control Register 1	0000_H
CCM2	**b**	$FF56_H$		AB_H	CAPCOM Mode Control Register 2	0000_H
CCM3	**b**	$FF58_H$		AC_H	CAPCOM Mode Control Register 3	0000_H
CCM4	**b**	$FF22_H$		91_H	CAPCOM Mode Control Register 4	0000_H
CCM5	**b**	$FF24_H$		92_H	CAPCOM Mode Control Register 5	0000_H
CCM6	**b**	$FF26_H$		93_H	CAPCOM Mode Control Register 6	0000_H
CCM7	**b**	$FF28_H$		94_H	CAPCOM Mode Control Register 7	0000_H
CP		$FE10_H$		08_H	CPU Context Pointer Register	$FC00_H$
CRIC	**b**	$FF6A_H$		$B5_H$	GPT2 CAPREL Interrupt Ctrl. Register	0000_H
CSP		$FE08_H$		04_H	CPU Code Segment Pointer Register (read only)	0000_H
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP2	**b**	$FFC2_H$		$E1_H$	Port 2 Direction Control Register	0000_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DP7	**b**	$FFD2_H$		$E9_H$	Port 7 Direction Control Register	00_H
DP8	**b**	$FFD6_H$		EB_H	Port 8 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7	**b**	$F1D2_H$	**E**	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8	**b**	$F1D6_H$	**E**	EB_H	Port 8 Open Drain Control Register	00_H
ONES		$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
P7	**b**	$FFD0_H$		$E8_H$	Port 7 Register (8 bits)	00_H
P8	**b**	$FFD4_H$		EA_H	Port 8 Register (8 bits)	00_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
PECC0	$FEC0_H$	60_H	PEC Channel 0 Control Register	0000_H
PECC1	$FEC2_H$	61_H	PEC Channel 1 Control Register	0000_H
PECC2	$FEC4_H$	62_H	PEC Channel 2 Control Register	0000_H
PECC3	$FEC6_H$	63_H	PEC Channel 3 Control Register	0000_H
PECC4	$FEC8_H$	64_H	PEC Channel 4 Control Register	0000_H
PECC5	$FECA_H$	65_H	PEC Channel 5 Control Register	0000_H
PECC6	$FECC_H$	66_H	PEC Channel 6 Control Register	0000_H
PECC7	$FECE_H$	67_H	PEC Channel 7 Control Register	0000_H
PICON b	$F1C4_H$ **E**	$E2_H$	Port Input Threshold Control Register	0000_H
PDCR	$F0AA_H$ **E**	55_H	Pin Driver Control Register	0000_H
PP0	$F038_H$ **E**	$1C_H$	PWM Module Period Register 0	0000_H
PP1	$F03A_H$ **E**	$1D_H$	PWM Module Period Register 1	0000_H
PP2	$F03C_H$ **E**	$1E_H$	PWM Module Period Register 2	0000_H
PP3	$F03E_H$ **E**	$1F_H$	PWM Module Period Register 3	0000_H
PSW b	$FF10_H$	88_H	CPU Program Status Word	0000_H
PT0	$F030_H$ **E**	18_H	PWM Module Up/Down Counter 0	0000_H
PT1	$F032_H$ **E**	19_H	PWM Module Up/Down Counter 1	0000_H
PT2	$F034_H$ **E**	$1A_H$	PWM Module Up/Down Counter 2	0000_H
PT3	$F036_H$ **E**	$1B_H$	PWM Module Up/Down Counter 3	0000_H
PW0	$FE30_H$	18_H	PWM Module Pulse Width Register 0	0000_H
PW1	$FE32_H$	19_H	PWM Module Pulse Width Register 1	0000_H
PW2	$FE34_H$	$1A_H$	PWM Module Pulse Width Register 2	0000_H
PW3	$FE36_H$	$1B_H$	PWM Module Pulse Width Register 3	0000_H
PWMCON0 b	$FF30_H$	98_H	PWM Module Control Register 0	0000_H
PWMCON1 b	$FF32_H$	99_H	PWM Module Control Register 1	0000_H
PWMIC b	$F17E_H$ **E**	BF_H	PWM Module Interrupt Control Register	0000_H
RP0H b	$F108_H$ **E**	84_H	System Start-up Config. Reg. (Rd. only)	XX_H
S0BG	$FEB4_H$	$5A_H$	Serial Channel 0 Baudrate Generator Reload Register	0000_H
S0CON b	$FFB0_H$	$D8_H$	Serial Channel 0 Control Register	0000_H

Table 8 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
T2IC	**b**	$FF60_H$		$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3		$FE42_H$		21_H	GPT1 Timer 3 Register	0000_H
T3CON	**b**	$FF42_H$		$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC	**b**	$FF62_H$		$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4		$FE44_H$		22_H	GPT1 Timer 4 Register	0000_H
T4CON	**b**	$FF44_H$		$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC	**b**	$FF64_H$		$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5		$FE46_H$		23_H	GPT2 Timer 5 Register	0000_H
T5CON	**b**	$FF46_H$		$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC	**b**	$FF66_H$		$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6		$FE48_H$		24_H	GPT2 Timer 6 Register	0000_H
T6CON	**b**	$FF48_H$		$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC	**b**	$FF68_H$		$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
T7		$F050_H$	**E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON	**b**	$FF20_H$		90_H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000_H
T7IC	**b**	$F17A_H$	**E**	BE_H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000_H
T7REL		$F054_H$	**E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H
T8		$F052_H$	**E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC	**b**	$F17C_H$	**E**	BF_H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000_H
T8REL		$F056_H$	**E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR	**b**	$FFAC_H$		$D6_H$	Trap Flag Register	0000_H
WDT		$FEAE_H$		57_H	Watchdog Timer Register (read only)	0000_H
WDTCON		$FFAE_H$		$D7_H$	Watchdog Timer Control Register	[2] $00XX_H$
XP0IC	**b**	$F186_H$	**E**	$C3_H$	CAN1 Module Interrupt Control Register	0000_H
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Unassigned Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Unassigned Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	PLL/OWD Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 33 MHz
		2.5[1]	5.5	V	Power Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2][3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3]
External Load Capacitance	C_L	–	50	pF	Pin drivers in **fast edge** mode (PDCR.BIPEC = '0')
		–	30	pF	Pin drivers in **reduced edge** mode (PDCR.BIPEC = '1')[3]
		–	100	pF	Pin drivers in **fast edge** mode, f_{CPUmax} = 25 MHz[4]
Ambient temperature	T_A	0	70	°C	SAB-C167CR …
		-40	85	°C	SAF-C167CR …
		-40	125	°C	SAK-C167CR …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not subject to production test - verified by design/characterization.

4) The increased capacitive load is valid for the 25 MHz-derivatives up to a CPU clock frequency of 25 MHz. Under these circumstances the timing parameters as specified in the "C167CR Data Sheet 1999-06" are valid.

4.3 Analog/Digital Converter Parameters

Table 13 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2 t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} + 0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not subject to production test - verified by design/characterization.

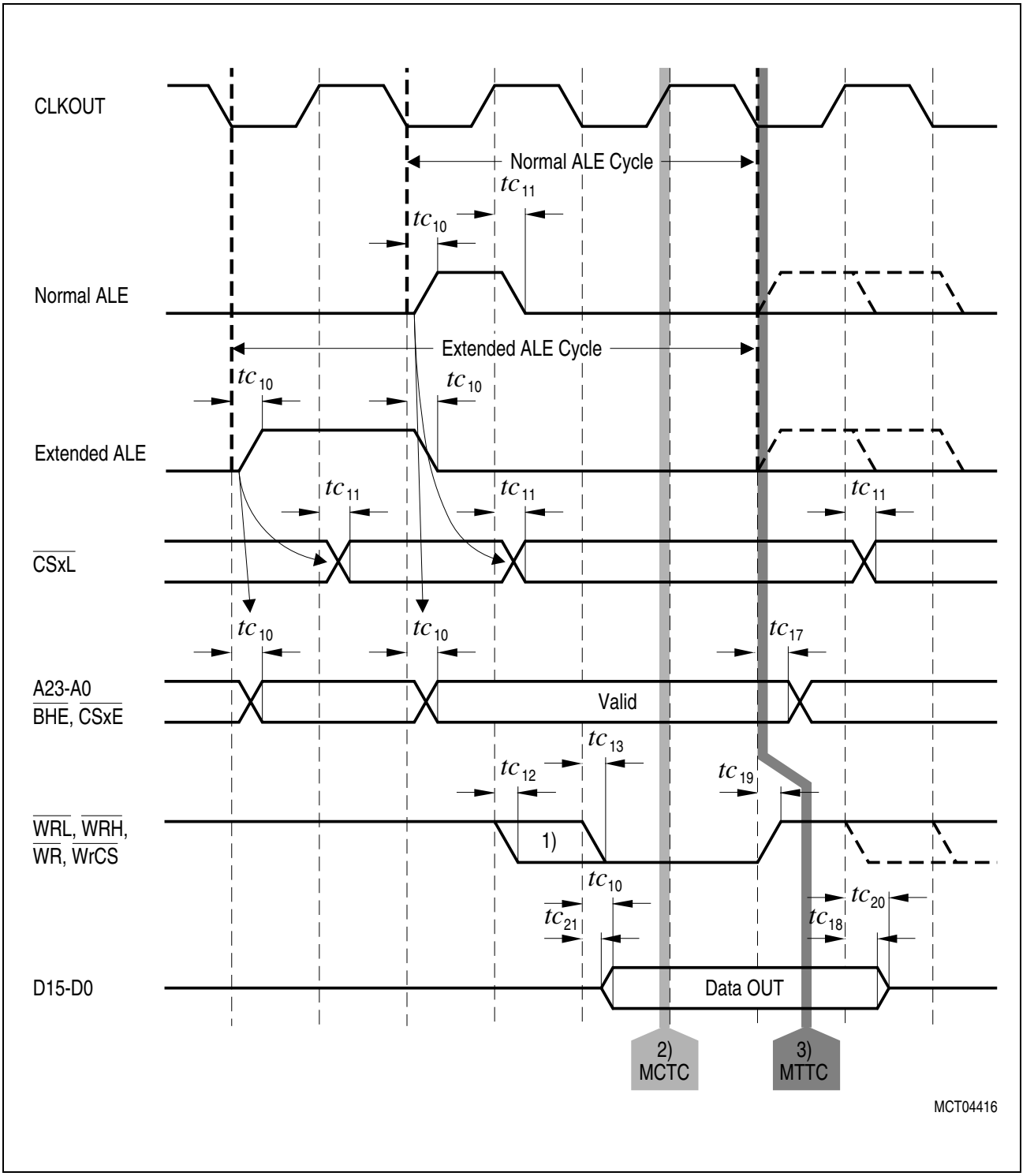

Figure 16 Demultiplexed Bus, Write Access

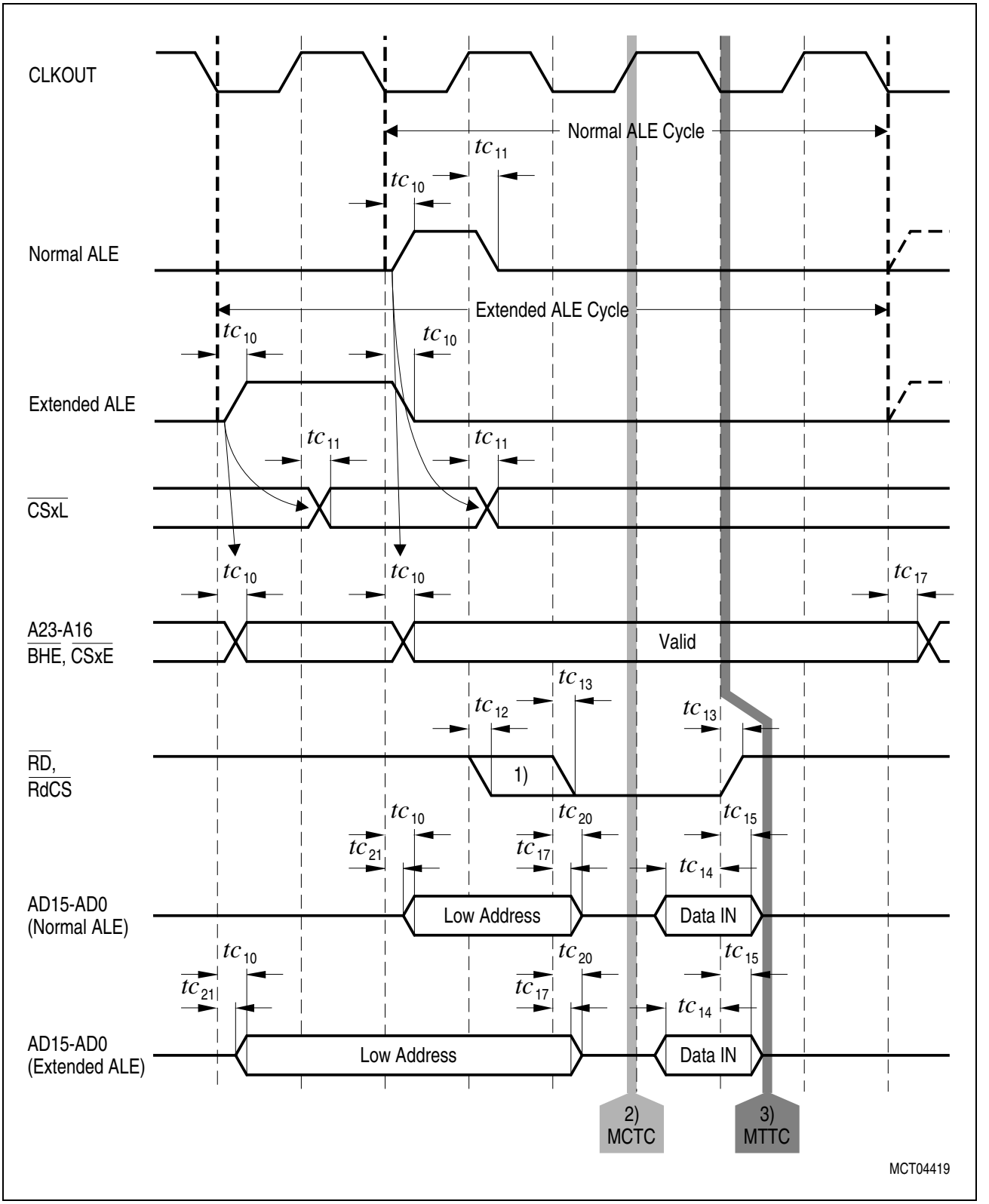

Figure 19 Multiplexed Bus, Read Access

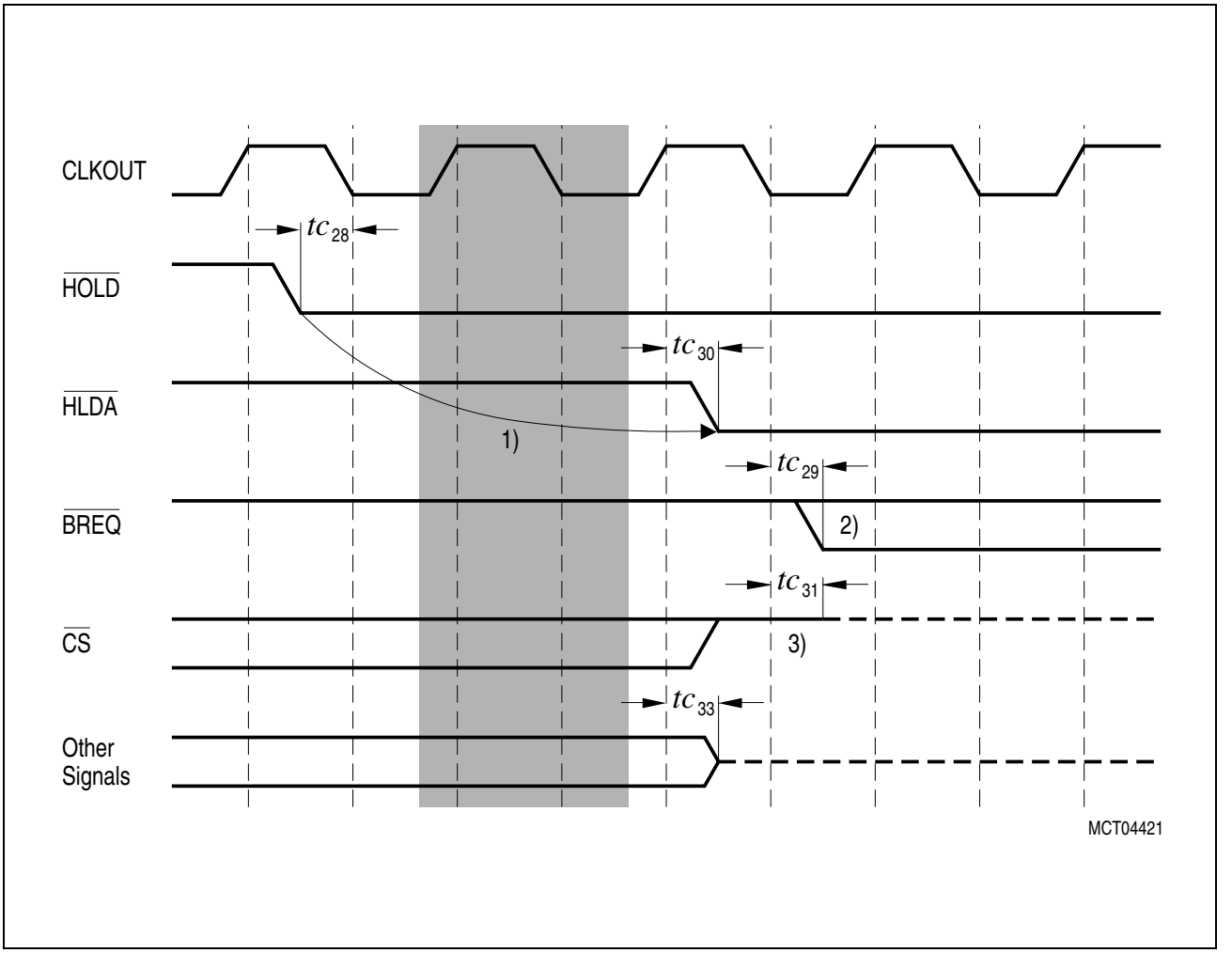

Figure 21 External Bus Arbitration, Releasing the Bus

Notes

1. *The C167CR will complete the currently running bus cycle before granting bus access.*
2. *This is the first possibility for $\overline{BREQ}$ to get active.*
3. *The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{33}. Latched $\overline{CS}$ outputs are driven high for 1 TCL before the output drivers are switched off.*

External XRAM Access

If XPER-Share mode is enabled the on-chip XRAM of the C167CR can be accessed (during hold states) by an external master like an asynchronous SRAM.

Table 22 XRAM Access Timing (Operating Conditions apply)[1)]

Parameter		Symbol		Limits		Unit
				Min.	Max.	
Address setup time before $\overline{RD}$/$\overline{WR}$ falling edge		t_{40}	SR	4	–	ns
Address hold time after $\overline{RD}$/$\overline{WR}$ rising edge		t_{41}	SR	0	–	ns
Data turn on delay after $\overline{RD}$ falling edge	Read	t_{42}	CC	1	–	ns
Data output valid delay after address latched	Read	t_{43}	CC	–	40	ns
Data turn off delay after $\overline{RD}$ rising edge	Read	t_{44}	CC	1	14	ns
Write data setup time before $\overline{WR}$ rising edge	Write	t_{45}	SR	10	–	ns
Write data hold time after $\overline{WR}$ rising edge	Write	t_{46}	SR	2	–	ns
$\overline{WR}$ pulse width	Write	t_{47}	SR	20	–	ns
$\overline{WR}$ signal recovery time	Write	t_{48}	SR	t_{40}	–	ns

1) The minimum access cycle time is 60 ns.

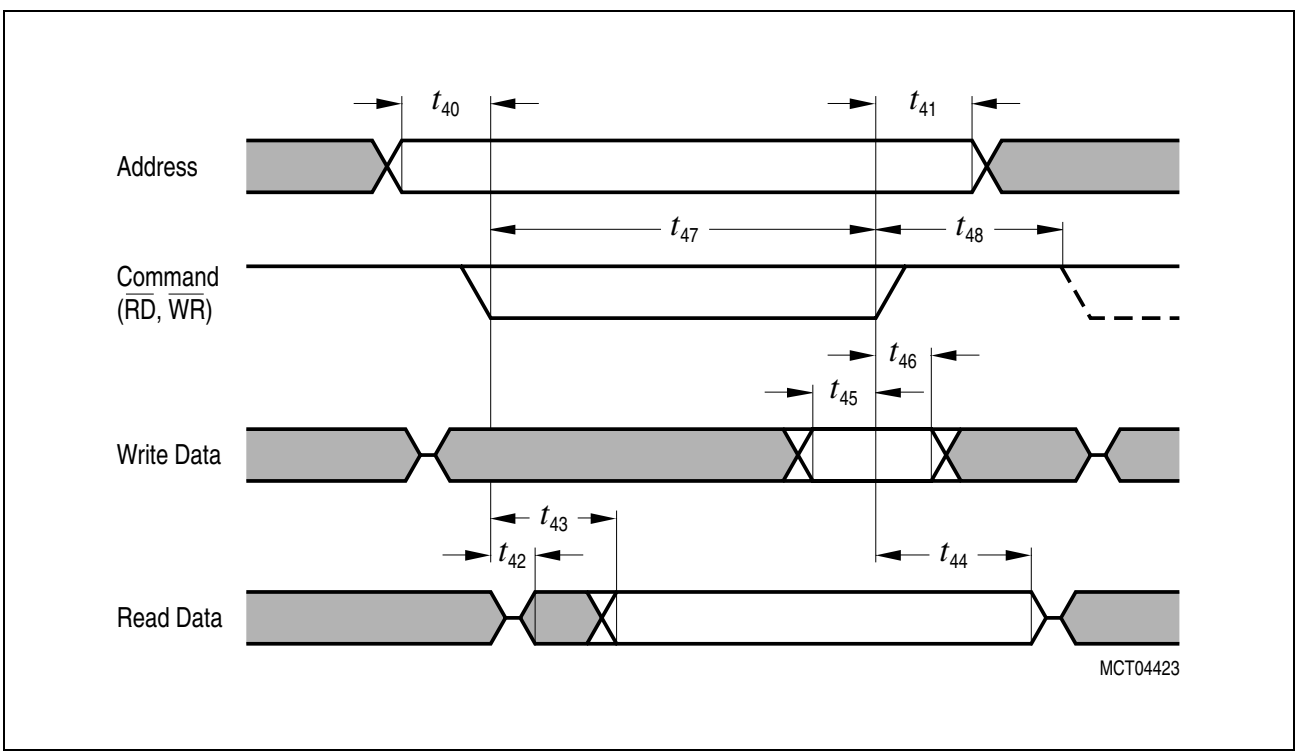

Figure 23 External Access to the XRAM

w w w . i n f i n e o n . c o m

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