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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (2.55x2.55)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a02uk-118

6. Pinning information

6.1 Pinning

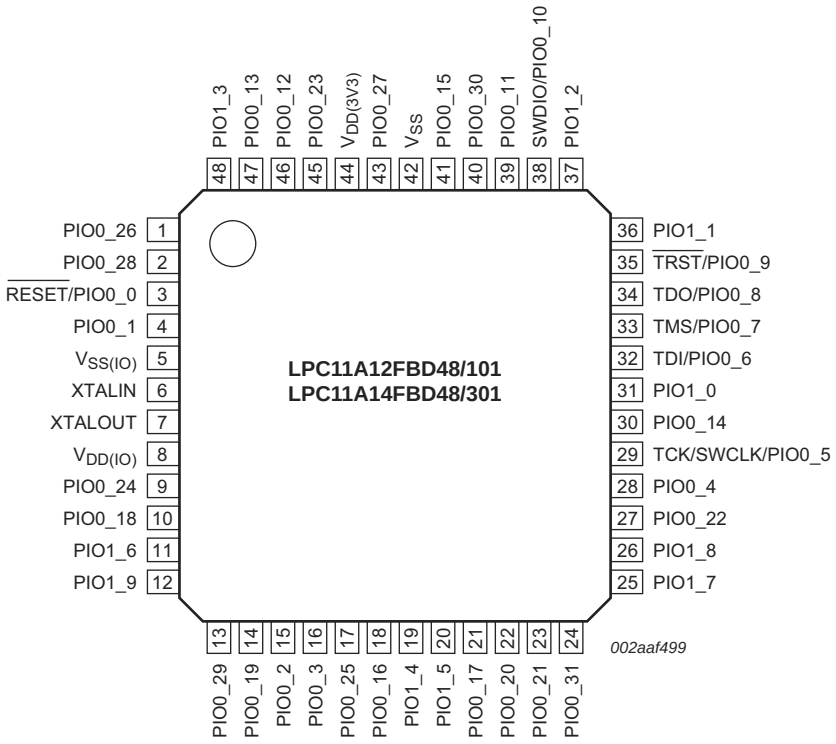


Fig 2. Pin configuration LQFP48 package

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_3/SDA/ACMP_O/ SWDIO/CT16B1_CAP0	16	11	B1	[4][6]	I/O	I; IA	**PIO0_3 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SDA —** I^2C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I/O	-	**SWDIO —** Serial Wire Debug I/O (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWDIO function by the boot loader after reset.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. Input glitch filter (50 ns) capable.
PIO0_4/R/AOUT/ CT16B0_MAT1/MOSI0	28	18	A4	[7]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**AOUT —** D/A converter output.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ R/CT16B0_MAT2/ SCK0	29	19	-	[9]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ VDDCMP/ CT16B0_MAT2/ SCK0	-	-	B3	[7][8]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and secondary Serial Wire Debug ClocK. Use PIO0_2 for the default TCK/SWCLK function. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
TDI/PIO0_6/AD0/ CT32B0_MAT3/MISO0	32	21	C3	[9]	I	I; PU	**TDI —** Test Data In for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_6 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD0 —** A/D converter input 0.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I/O	-	**MISO0 —** Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
TMS/PIO0_7/AD1/ CT32B1_CAP0/ CT16B0_MAT0	33	22	C4	[9]	I	I; PU	**TMS —** Test Mode Select for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_7 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD1 —** A/D converter input 1.
					I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0 —** Match output 2 for 16-bit timer 0.
TDO/PIO0_8/AD2/ CT32B1_MAT0/SCK1	34	23	C2	[9]	O	I; PU	**TDO —** Test Data Out for JTAG interface.
					I/O	-	**PIO0_8 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD2 —** A/D converter input 2.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I/O	-	**SCK1 —** Serial clock for SSP1. Input glitch filter (10 ns) capable.
$\overline{\text{TRST}}$/PIO0_9/AD3/ CT32B1_MAT1/ CT16B0_MAT1/$\overline{\text{CTS}}$	35	24	D4	[9]	I	I; PU	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_9 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD3 —** A/D converter, input 3.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1/ VDDCMP	30	20	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1	-	-	B4	[9]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO0_15/TXD/AD7/ CT32B0_CAP2/SDA	41	27	E4	[9]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					O	-	**TXD —** Transmitter data output for USART.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
PIO0_16/ ATRG0/ACMP_I3/ CT16B0_CAP1/SCL	18	13	A2	[9]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**ATRG0 —** Conversion trigger 0 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I3 —** Analog comparator input 3.
					I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/$\overline{\text{RTS}}$/ ACMP_O/ CT32B0_CAP0/SCLK	45	30	-	[3]	I/O	I; PU	**PIO0_23 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					I/O	-	**SCLK —** Serial clock for USART.
PIO0_24/SCL/CLKIN/ CT16B1_CAP0	9	7	-	[3]	I/O	I; PU	**PIO0_24 —** General purpose digital input/output pin.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN —** External clock input.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/ CT16B1_MAT0	17	12	-	[3]	I/O	I; PU	**PIO0_25 —** General purpose digital input/output pin.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10].
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/ CT16B1_CAP1/ CT32B0_CAP2	1	1	-	[3]	I/O	I; PU	**PIO0_26 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/ CT32B1_MAT1/ CT16B1_CAP2	43	28	-	[9]	I/O	I; PU	**PIO0_27 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I1 —** Analog comparator input 1.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/$\overline{\text{DTR}}$/SSEL1/ CT32B0_CAP0	2	-	-	[3]	I/O	I; PU	**PIO0_28 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO0_29/$\overline{\text{DSR}}$/SCK1/ CT32B0_CAP1	13	-	-	[3]	I/O	I; PU	**PIO0_29 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO1_5/TXD/SCK1/ CT32B0_MAT2/ CT32B1_CAP1/ CT16B0_CAP2	20	-	-	[3]	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					I	-	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_6/$\overline{\text{RTS}}$/MOSI1/ CT32B0_MAT3/ CT32B1_CAP2/ CT16B0_MAT0	11	-	-	[3]	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I	-	**CT32B1_CAP2 —** Capture input 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_7/$\overline{\text{CTS}}$/MOSI0/ CT32B1_MAT1/ CT16B0_MAT2/ CT16B1_CAP2	25	-	-	[3]	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1.
PIO1_8/RXD / MISO1/ CT32B1_MAT0/ CT16B1_MAT1	26	-	-	[3]	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
					I	-	**RXD —** Receiver data input for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_9/$\overline{\text{DCD}}$/R/ CT32B1_MAT2 / CT16B1_MAT2	12	-	-	[3]	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	-	**R —** Reserved.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					O	-	**CT16B1_MAT2 —** Match output 2 for 16-bit timer 1.
XTALIN	6	4	-	[11]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	5	-	[11]	-	-	Output from the oscillator amplifier.
$V_{DD(IO)}$	8	6	E2	[12] [13]	-	-	3.3 V input/output supply voltage.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I^2C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.19 General purpose external event counter/timers

The LPC11Axx includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt. Up to three capture channels are pinned out. One channel is internally connected to the comparator output ACMP_O.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.20 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.21 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.22 Clocking and power control

7.22.1 Crystal and internal oscillators

The LPC11Axx include four independent oscillators.

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, Low-Frequency Oscillator (LFOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Each oscillator, except the WDOsc, can be used for more than one purpose as required in a particular application.

Following reset, the LPC11Axx will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC11Axx clock generation.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			2.6	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			2.6	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash; $V_{DD(3V3)} = V_{DD(IO)} = 3.3$ V; low-current mode (see Section 7.22.6.2)					
		system clock = 12 MHz; all peripherals disabled	[2][4][5]	-	3	-	mA
		system clock = 48 MHz; all peripherals disabled	[2][6][5]	-	8	-	mA
		Sleep mode; system clock = 12 MHz; $V_{DD(3V3)} = V_{DD(IO)} = 3.3$ V; low-current mode (see Section 7.22.6.2)					
		all peripherals disabled; 12 MHz	[2][4][5]	-	2	-	mA
		all peripherals disabled; 48 MHz	[2][4][5]	-	5	-	mA
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	$V_I = 0$ V; on-chip pull-up resistor disabled		-	0.5	1000	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	0.5	1000	nA
I_{OZ}	OFF-state output current	$V_O = 0$ V; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	0.5	1000	nA
V_I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
		5 V tolerant pins					
		3 V tolerant pins: PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package)	[7][8]			$V_{DD(IO)}$	
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	$3.0\text{ V} \leq V_{DD(IO)} \leq 3.6\text{ V}$		0.4	-	-	V

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−160	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−15	−50	−85	μA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_2 and PIO0_3)							
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3$V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.05$V_{DD(IO)}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as high-current sink pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[11]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; SysOsc disabled; system PLL disabled.

[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

[6] IRC disabled; SysOsc enabled; system PLL enabled.

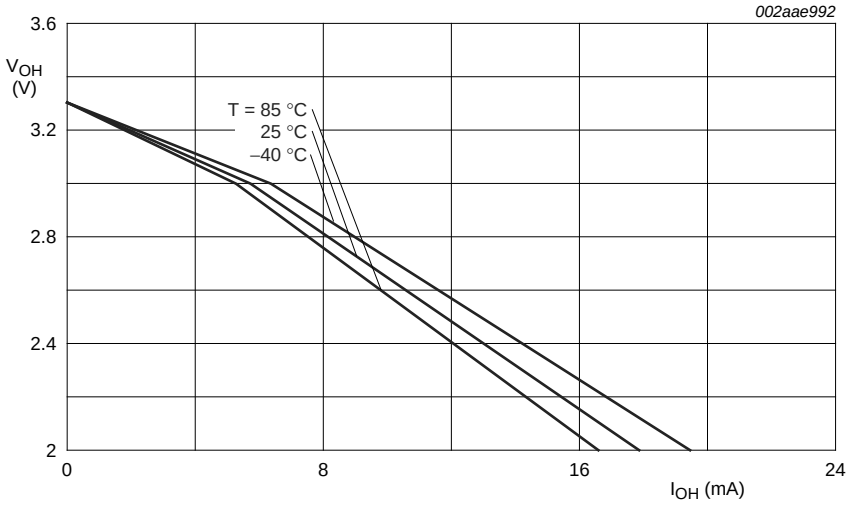
[7] Including voltage on outputs in 3-state mode.

[8] All supply voltages must be present.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

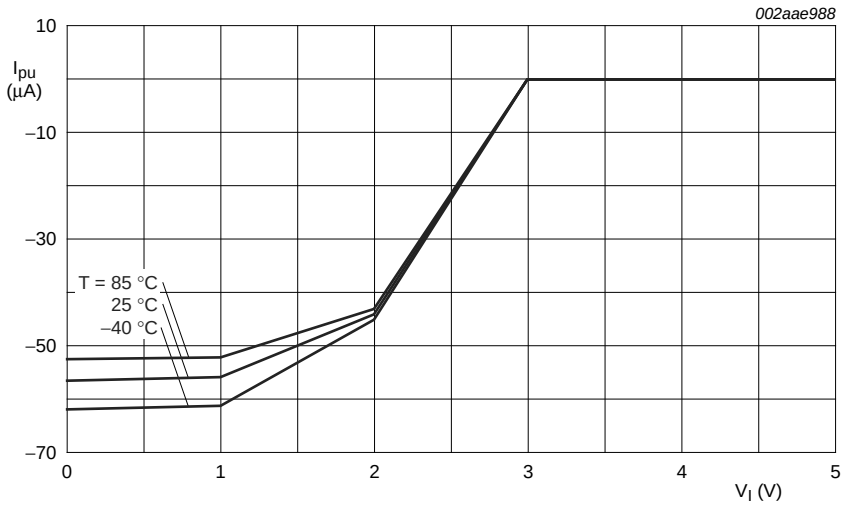
[10] Does not apply to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package).

[11] To V_{SS}.



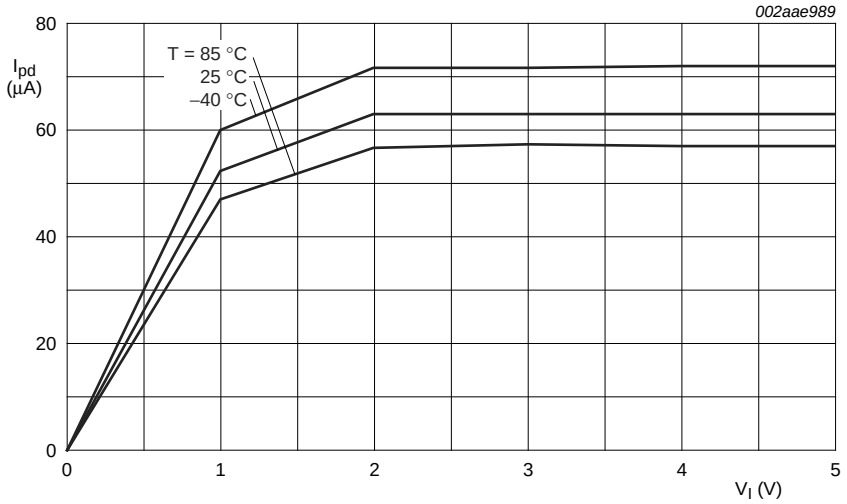
Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 17. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 18. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 19. Typical pull-down current I_{pd} versus input voltage V_I

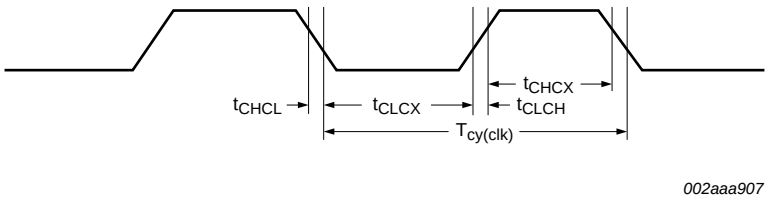


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.4 Internal oscillators

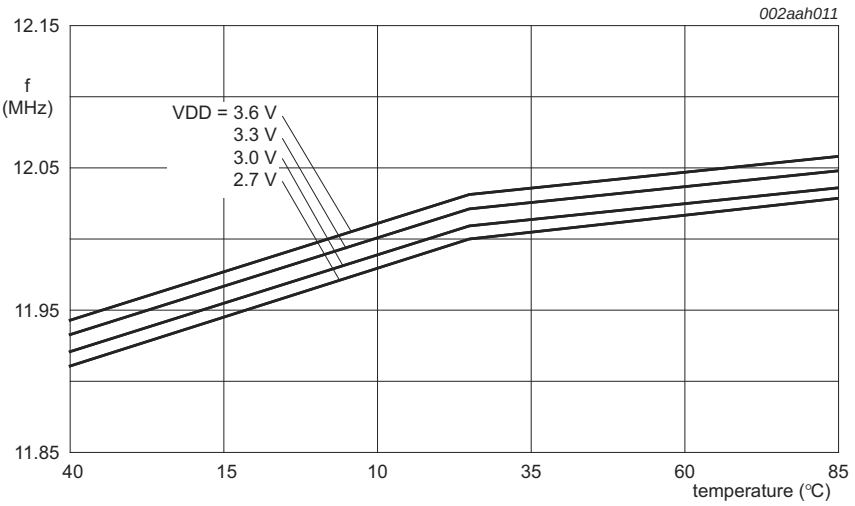
Table 12. Dynamic characteristic: IRC

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1% accuracy is guaranteed for 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1% accuracy specification for voltages below 2.7 V.

Fig 22. Internal IRC frequency vs. temperature

Table 13. Dynamic characteristics: WDOsc and LFOsc

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{osc}	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

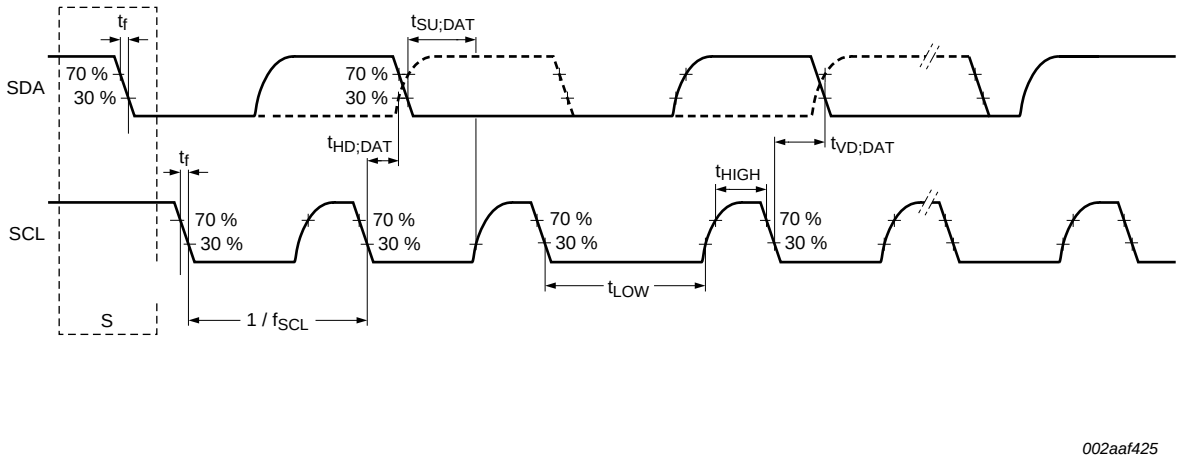


Fig 23. I^2C-bus pins clock timing

10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode
2.6 V <= $V_{DD(3V3)}$ = $V_{DD(IO)}$ <= 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1][1]	40			ns
t_{DS}	data set-up time	in SPI mode	[1][2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[1][2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[1][2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[1][2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)}$ = 3.3 V.

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC11Axx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

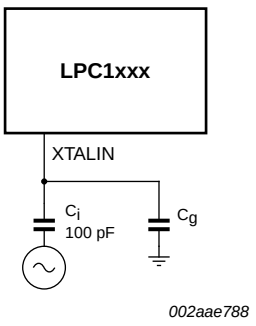


Fig 29. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 30 and in Table 27 and Table 28. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

R_S). Capacitance C_P in Figure 30 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 27).

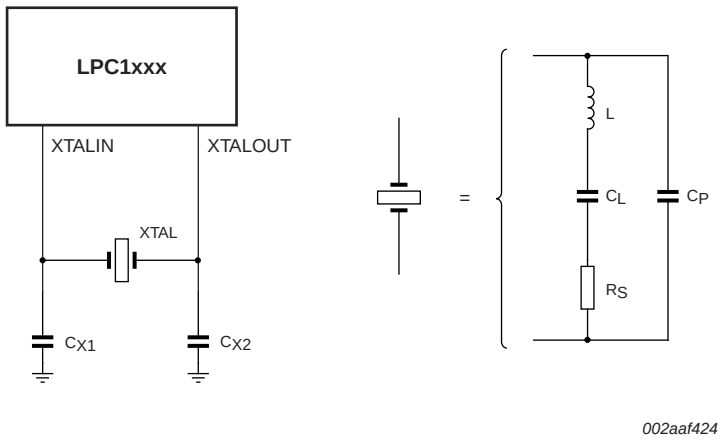


Fig 30. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

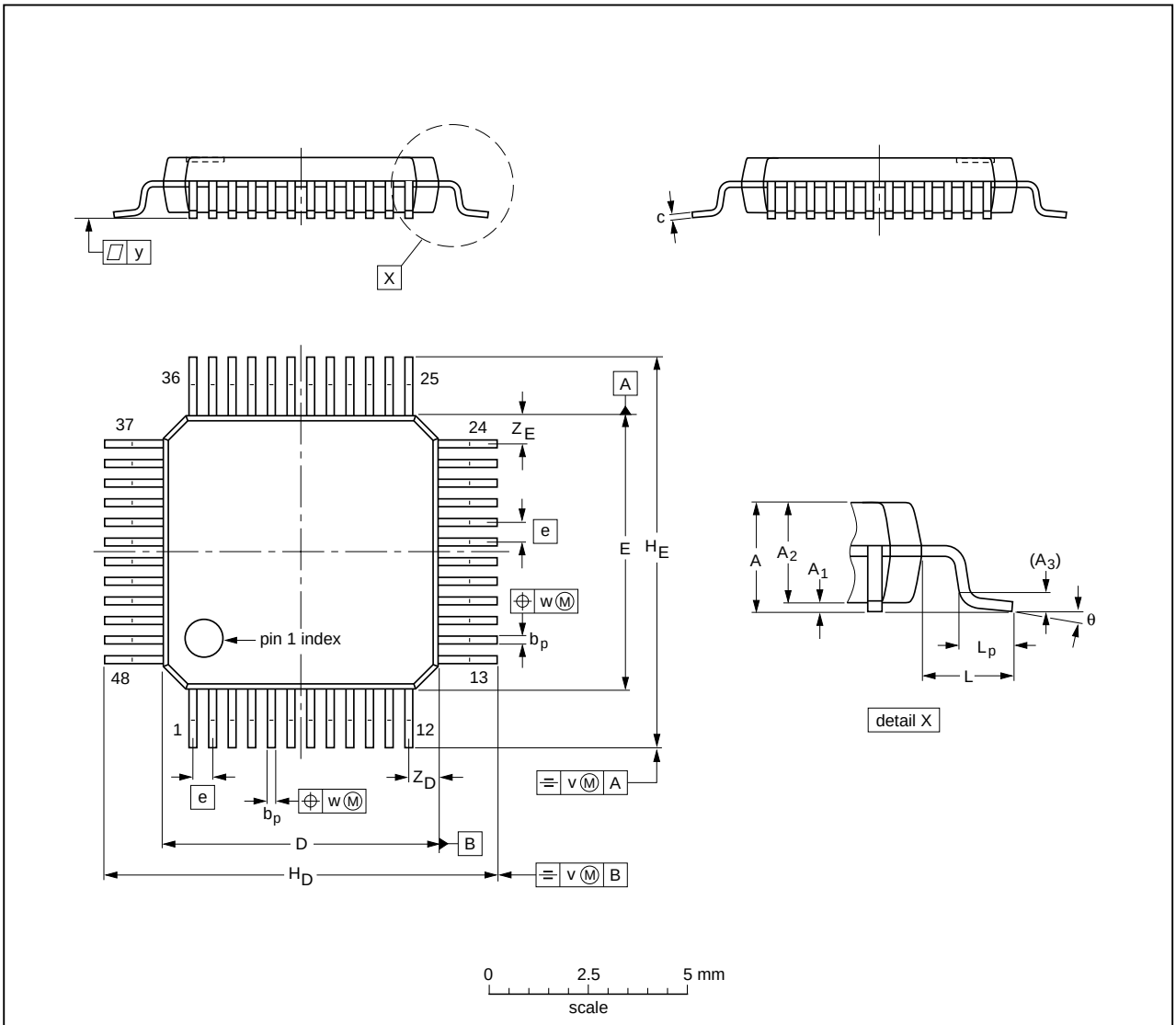
Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 28. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

13. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 34. Package outline LQFP48

Footprint information for reflow soldering of HVQFN33 package

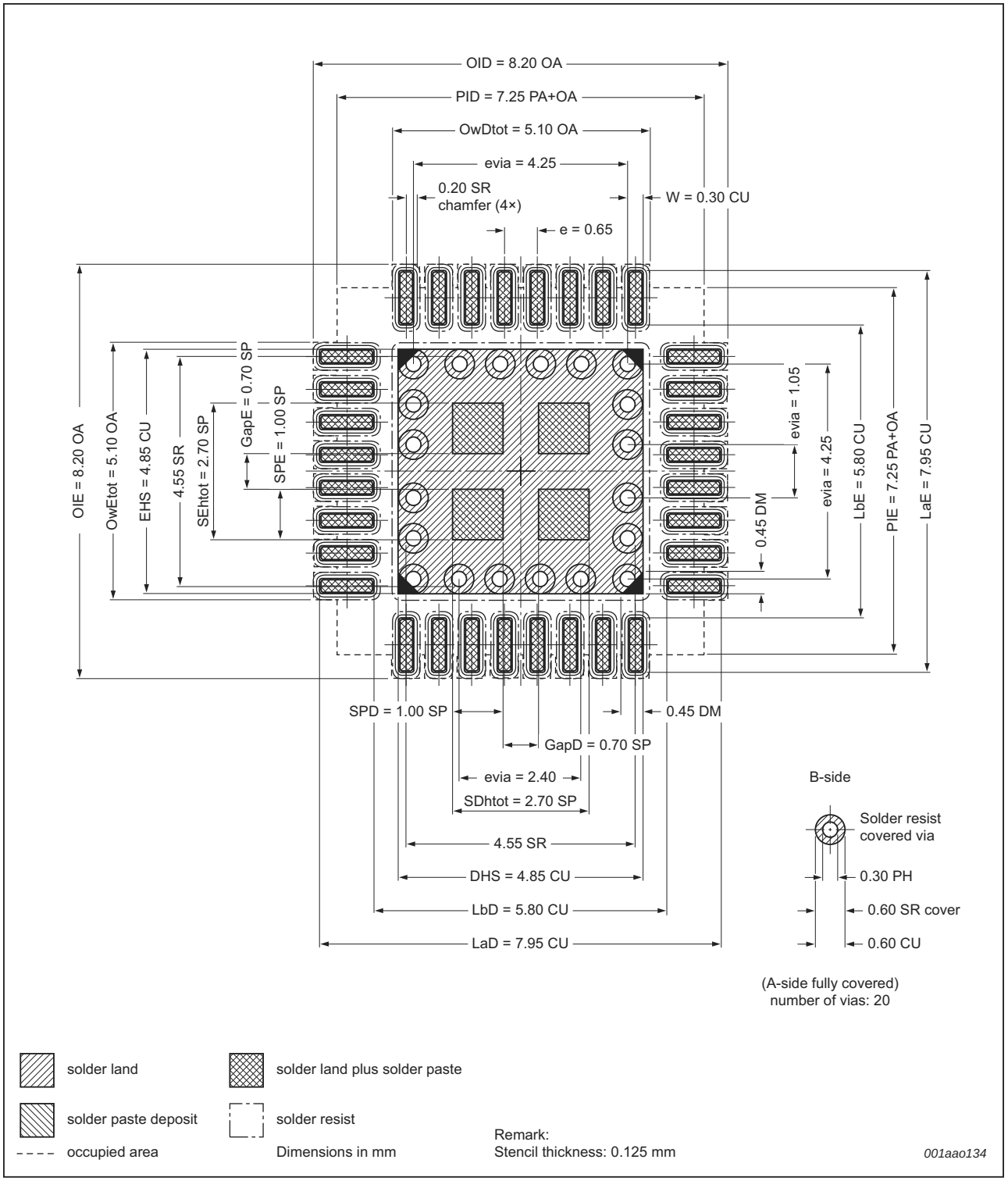


Fig 39. Reflow soldering of the HVQFN33(7x7) package

Table 30. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11AXX v.2	20120625	Preliminary data sheet	-	LPC11AXX v.1
	• Data sheet status changed to Preliminary. • Parameter f_{clk} removed from Table 11. • t_{er} removed in Table 11. • Writable EEPROM size specified in Section 7.3. • Section 10.3 “UVLO reset behavior” added. • Power consumption data updated for active mode and sleep mode (see Figure 11 to Figure 13). • Power consumption data for active and sleep modes with all peripherals enabled removed in Table 6 and Section 9.1. • Parameters $t_{s(pu)}$ and $t_{s(sw)}$ removed from Section 7.15. • Parameter t_{PD} updated in Table 25. • SSP dynamic characteristics added in Table 17. • WDOsc and LFOsc max and min frequency values updated throughout the data sheet. • Section 12.7 “UVLO protection circuit” added. • Typical values for parameters E_D, $E_{L(adj)}$, E_O, E_G, and C_L in Table 20 “DAC static and dynamic characteristics” changed to maximum values. • Parameter V_O corrected for condition T_{amb} = −40 °C to +85 °C in Table 22.		
LPC11AXX v.1	20120322	Objective data sheet	-	-