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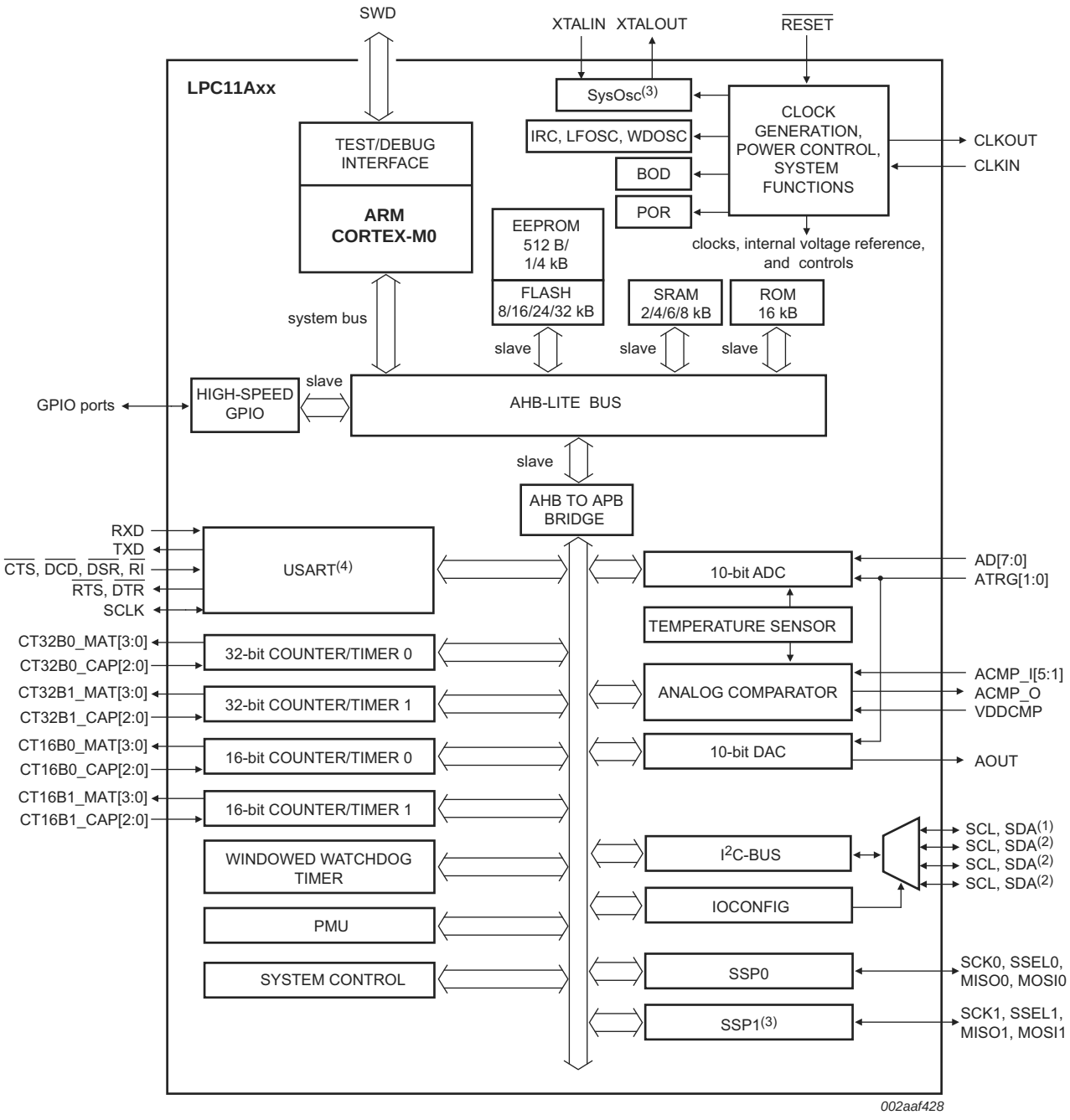
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (2.55x2.55)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a04uk-118

5. Block diagram



(1) Open-drain pins.

(2) Standard I/O pins.

(3) Not available on WLCSP packages.

(4) Modem control pins not available on WLCSP packages.

Fig 1. LPC11Axx block diagram

6. Pinning information

6.1 Pinning

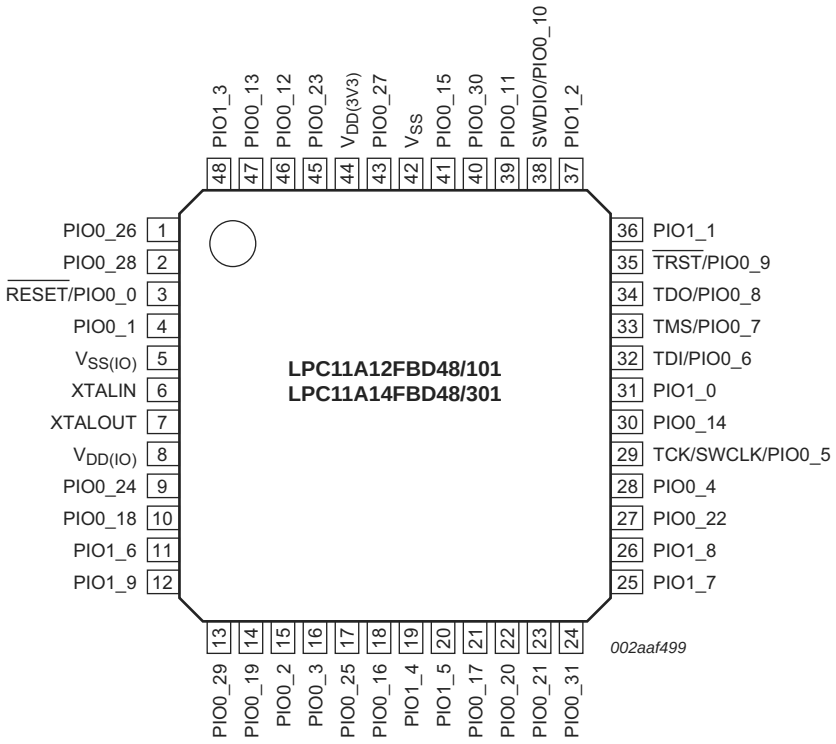


Fig 2. Pin configuration LQFP48 package

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
SWDIO/PIO0_10/AD4/ CT32B1_MAT2/ CT16B0_MAT2/RTS	38	25	D3	[9]	I/O	I; PU	**SWDIO —** Primary (default) Serial Wire Debug I/O for the LQFP48 and HVQFN33 packages. For the WLCSP20 package, use PIO0_3. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_10 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD4 —** A/D converter, input 4.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
PIO0_11/SCLK/ AD5/CT32B1_MAT3/ CT32B0_CAP0	39	26	D2	[9]	I/O	I; PU	**PIO0_11 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**SCLK —** Serial clock for USART. Input glitch filter (10 ns) capable.
					I	-	**AD5 —** A/D converter, input 5.
					O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. Input glitch filter (10 ns) capable.
PIO0_12/RXD/ ACMP_O/ CT32B0_MAT0/SCL/ CLKIN	46	31	E1	[3]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin.
					I	-	**RXD —** Receiver data input for USART. This pin is used for ISP communication.
					O	-	**ACMP_O —** Analog comparator output.
					O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN —** External clock input.
PIO0_13/TXD/ ACMP_I2/ CT32B0_MAT1/SDA	47	32	D1	[9]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					O	-	**TXD —** Transmitter data output for USART. This pin is used for ISP communication.
					I	-	**ACMP_I2 —** Analog comparator input 2.
					O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I^2C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

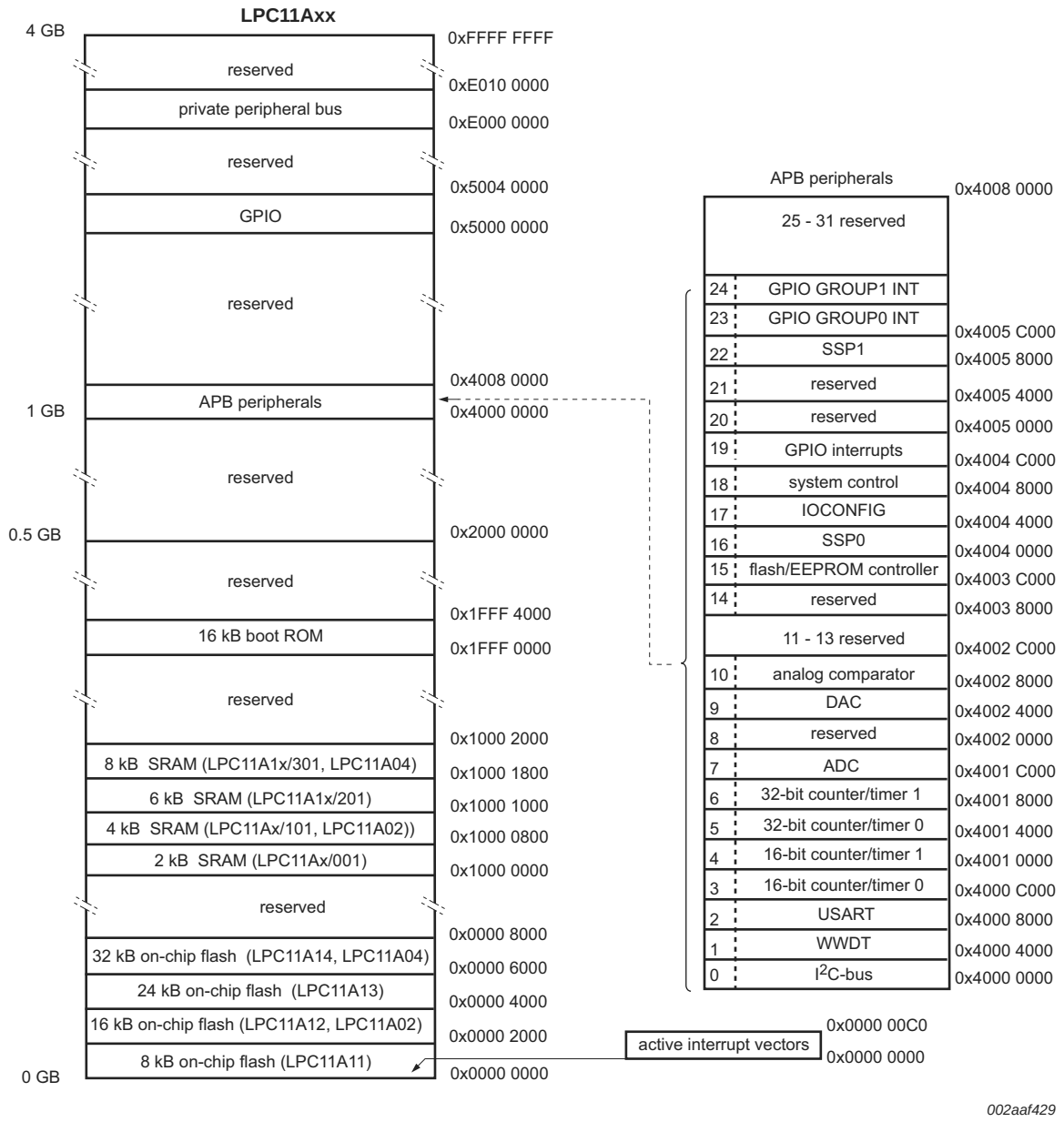


Fig 5. LPC11Axx memory map

7.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11Axx, the NVIC supports 32 vectored interrupts including up to 8 inputs to the start logic from the individual GPIO pins.

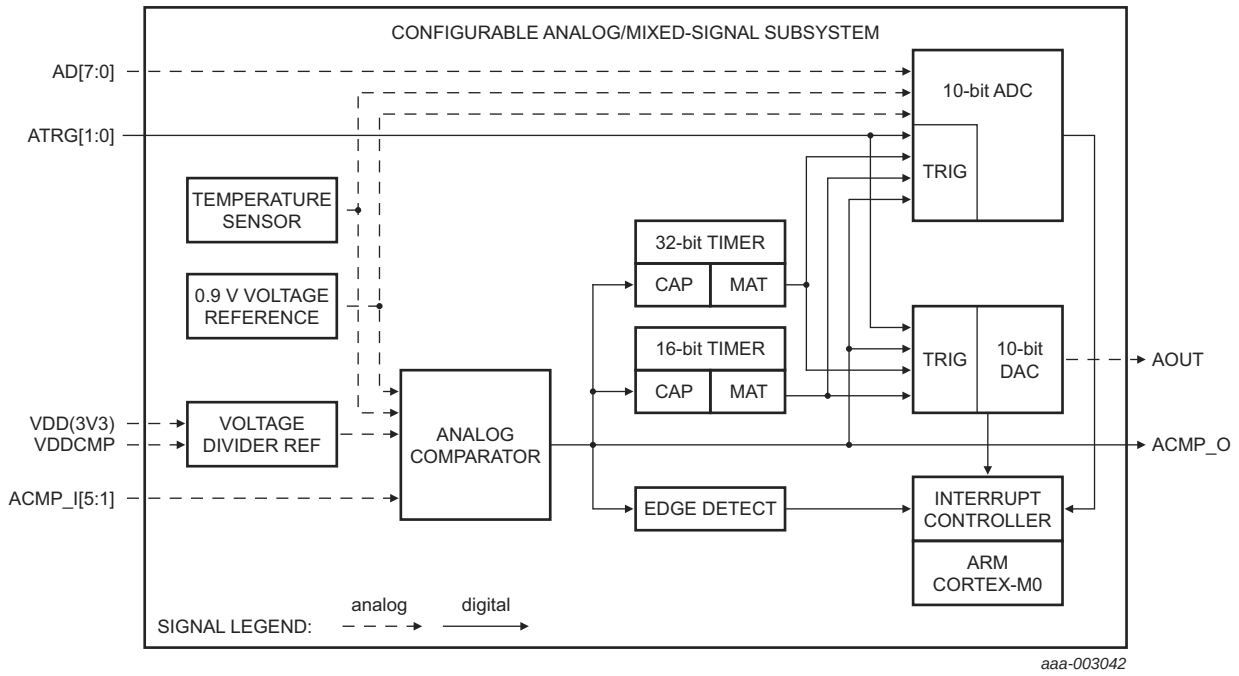


Fig 6. Configurable analog/mixed signal subsystem

7.14 10-bit ADC

The LPC11Axx contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

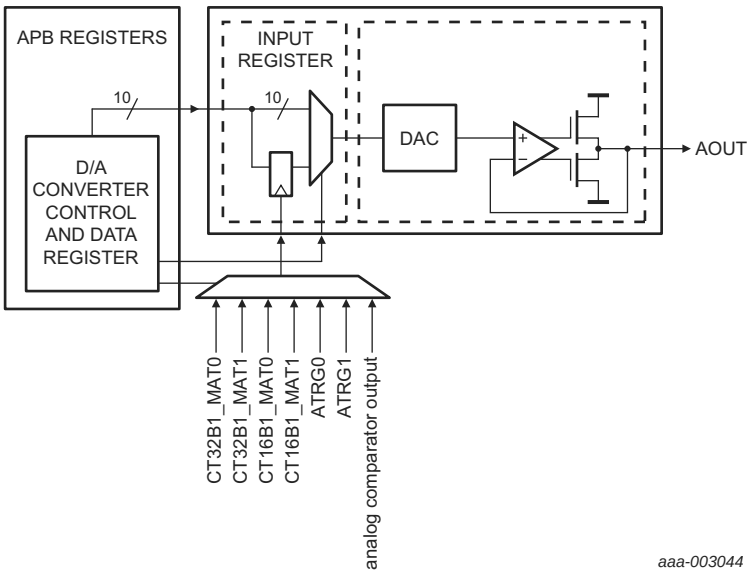


Fig 8. DAC block diagram

7.17.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
  - write operations to the DAC register.
  - a transition of pins ATRG0 or ATRG1. Input signals must be held for a minimum of three system clock periods.
  - a timer match signal.
  - a comparator output signal held for a minimum of two system clock periods.
- Holds output value during Sleep mode if the DAC is not powered down.

7.18 Analog comparator

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages. See Table 24.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	−0.5	4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	−0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	−0.5	+5.5	V
		on pins PIO0_2 and PIO0_3	[5]	−0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	−0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[11]	−6.5	+6.5	kV
V_{trig}	trigger voltage	for LVTSCR based ESD pin protection; 1 ns to 10 ns rise time	[12]	8.2	-	V
		> 10 ns rise time		> 8.5	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_2 and PIO0_3 and except the 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−160	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−15	−50	−85	μA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_2 and PIO0_3)							
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3$V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.05$V_{DD(IO)}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as high-current sink pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[11]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; SysOsc disabled; system PLL disabled.

[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

[6] IRC disabled; SysOsc enabled; system PLL enabled.

[7] Including voltage on outputs in 3-state mode.

[8] All supply voltages must be present.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Does not apply to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package).

[11] To V_{SS}.

9.2 Peripheral power consumption

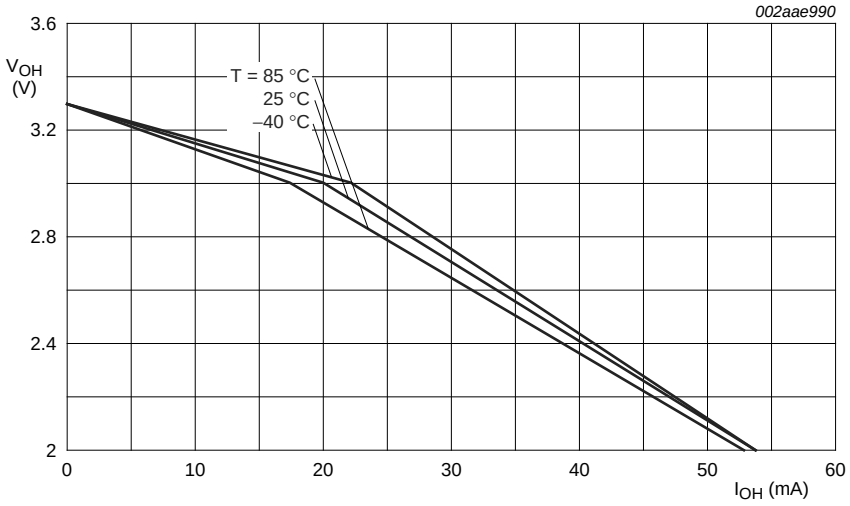
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

[1] IRC on; PLL off.

9.3 Electrical pin characteristics



Conditions: $V_{DD(IO)}$ = 3.3 V; on pin PIO0_21.

Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

Table 15. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

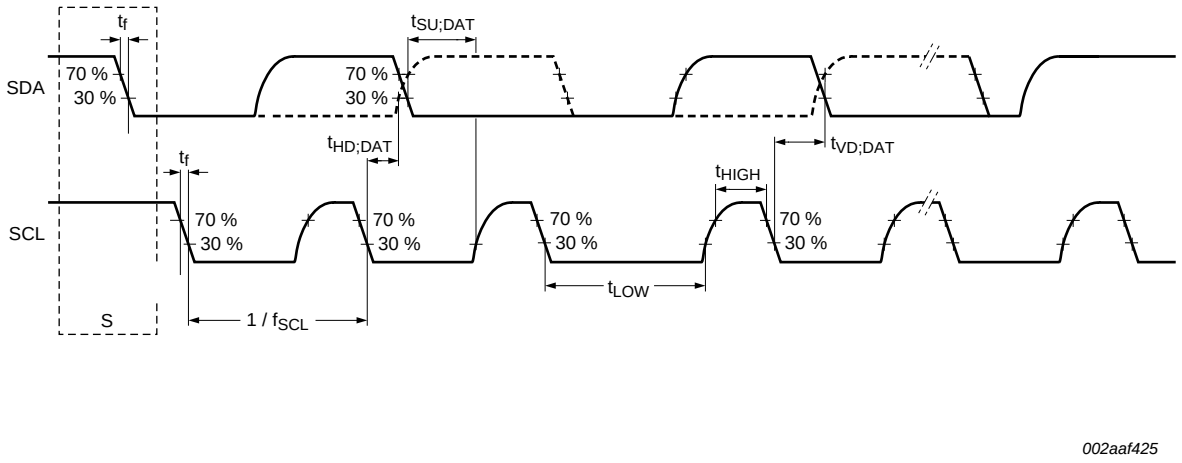


Fig 23. I^2C-bus pins clock timing

10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode
2.6 V <= $V_{DD(3V3)}$ = $V_{DD(IO)}$ <= 3.6 V.

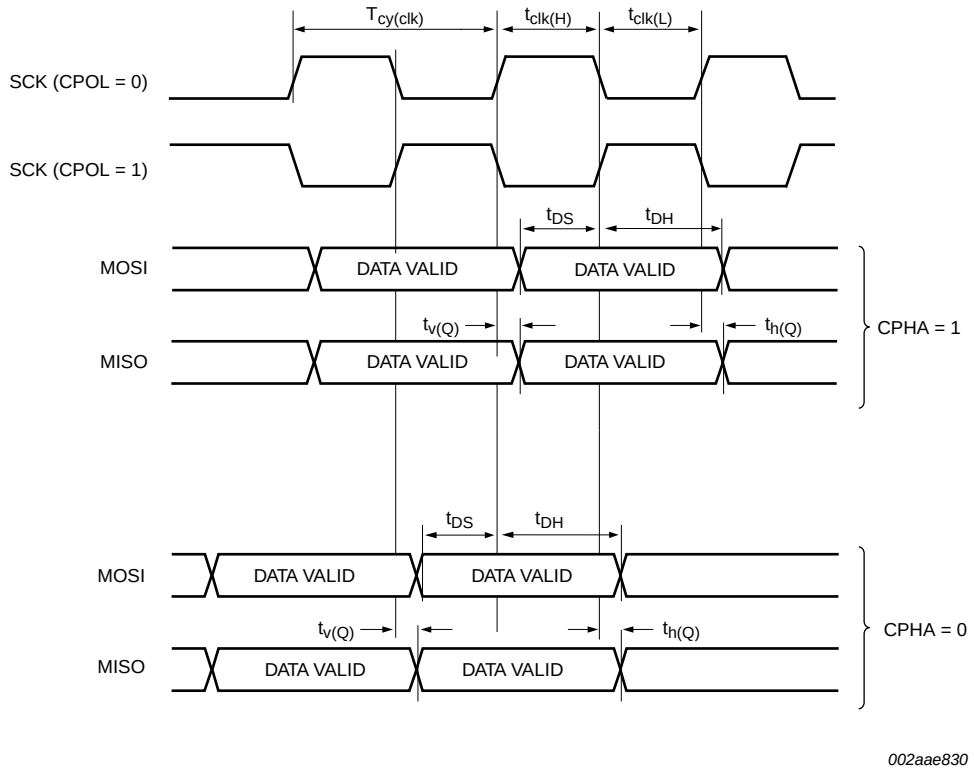
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1][1]	40			ns
t_{DS}	data set-up time	in SPI mode	[1][2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[1][2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[1][2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[1][2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)}$ = 3.3 V.



Pin names SCK, MISO, and MOSI refer to pins for both SSP peripherals, SSP0 and SSP1.

Fig 25. SSP slave timing in SPI mode

11. Characteristics of analog peripherals

Table 17. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage					
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC11Axx user manual*.

Table 18. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD(3V3)}$ = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	$V_{DD(3V3)}$	V
C_{ia}	analog input capacitance		-	-	4	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 20	mV
$V_{err(FS)}$	full-scale error voltage	[5]	-	-	± 20	mV
E_T	absolute error	[6]	-	-	± 4	LSB
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 26.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 26.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 26.

[5] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 26.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 26.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1pF.

[8] Input resistance R_i depends on the sampling frequency f_s: $R_i = 1 / (f_s \times C_{ia})$.

Table 25. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation ($V_{DD(3V3)}$ = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

Table 26. Comparator voltage ladder reference static characteristics
$V_{DD(3V3)}$ = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal $V_{DD(3V3)}$ supply					
		decimal code = 00	[2]	-	0	0	%
		decimal code = 08		-	0	±0.4	%
		decimal code = 16		-	–0.2	±0.2	%
		decimal code = 24		-	–0.2	±0.2	%
		decimal code = 30		-	–0.1	±0.1	%
		decimal code = 31		-	–0.1	±0.1	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		-	0	0	%
		decimal code = 08		-	–0.1	±0.5	%
		decimal code = 16		-	–0.2	±0.4	%
		decimal code = 24		-	–0.2	±0.3	%
		decimal code = 30		-	–0.2	±0.2	%
		decimal code = 31		-	–0.1	±0.1	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 µV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.

12.4 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.5 Standard I/O pad configuration

Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on 17 pins.
- Analog input

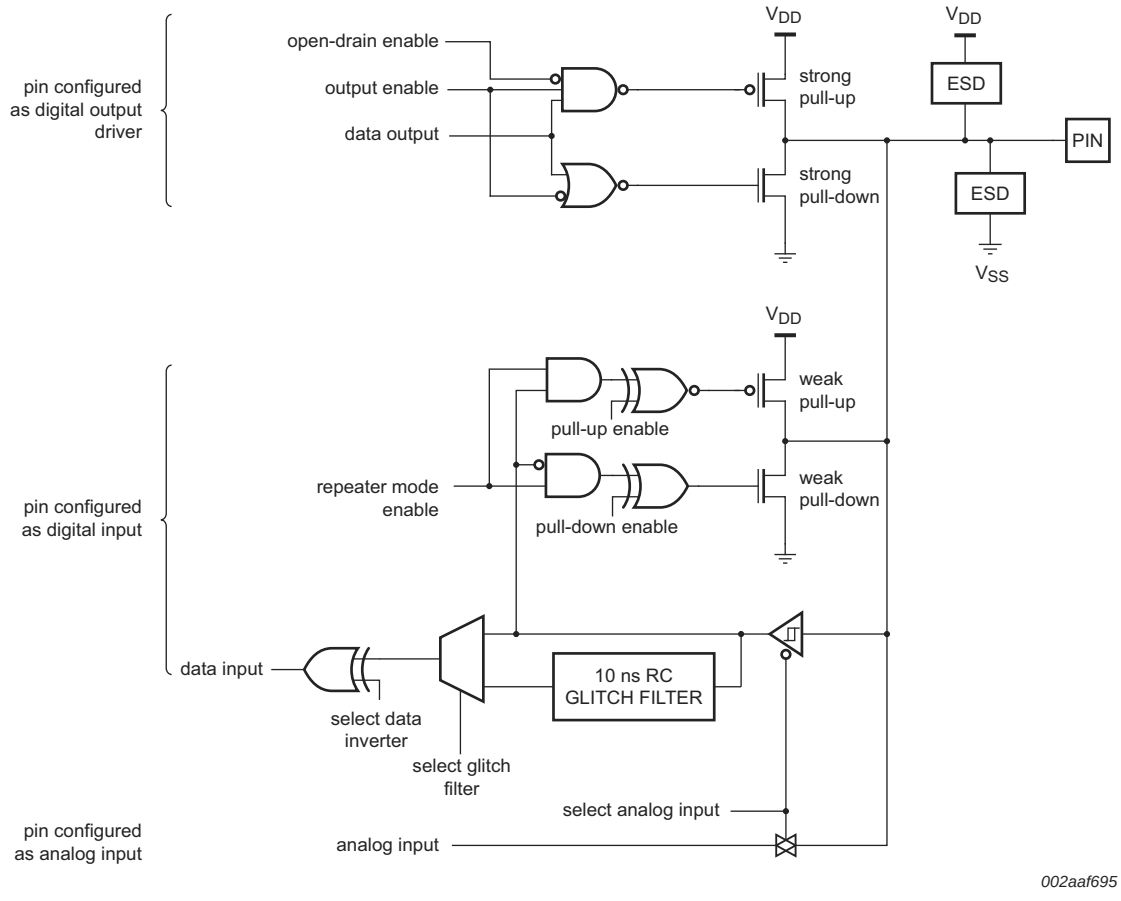
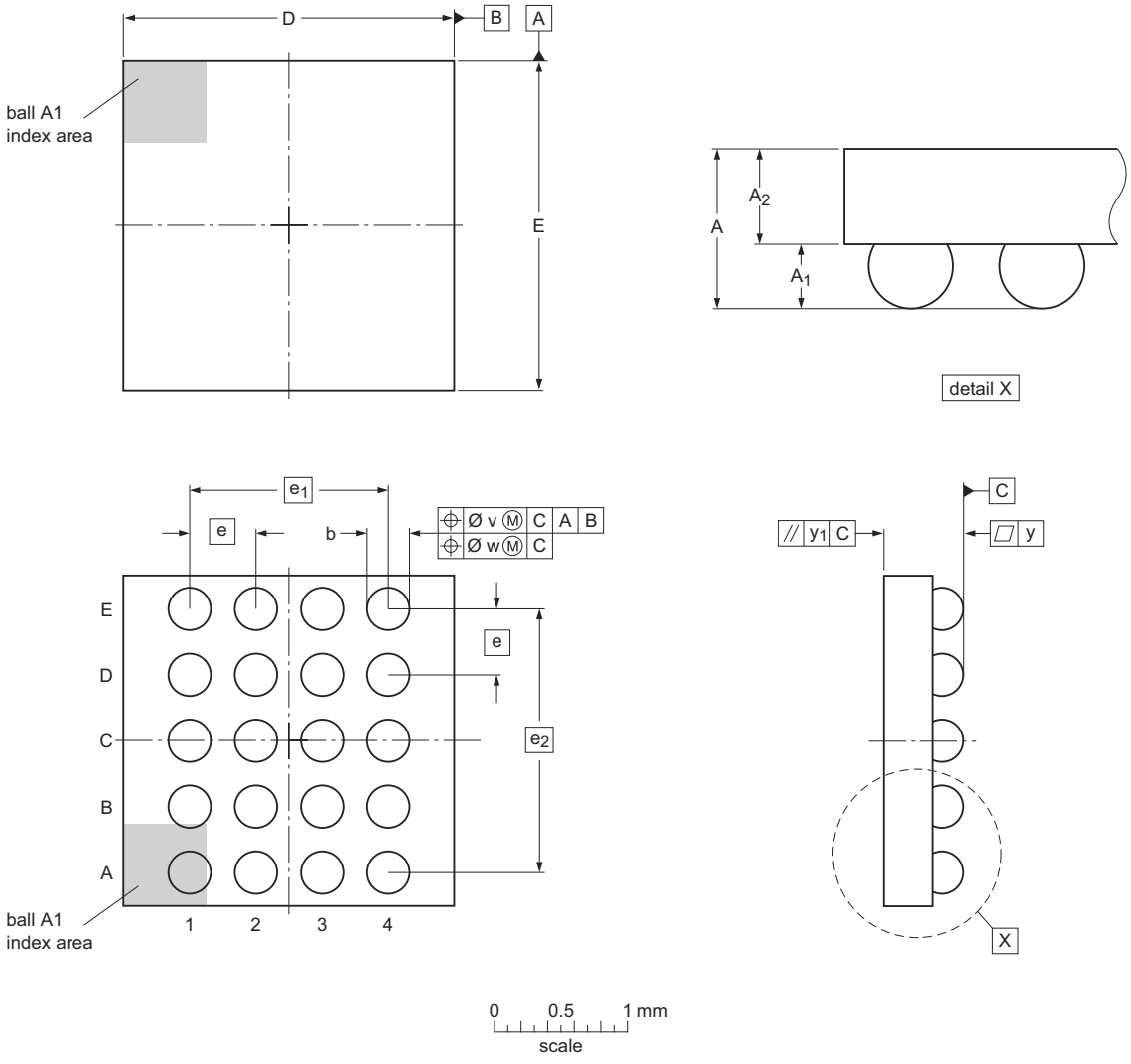


Fig 31. Standard I/O pad configuration

WLCSP20: wafer level chip-size package; 20 bumps; 2.5 x 2.5 x 0.6 mm **LPC11AxxUK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.65	0.27	0.38	0.35	2.60	2.60						
mm	nom	0.60	0.24	0.36	0.32	2.55	2.55	0.5	1.5	2.0	0.15	0.05	0.05
	min	0.55	0.21	0.34	0.29	2.50	2.50						

wlcsp20_lpc11axxuk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC11AxxUK						12-03-26

Fig 37. Package outline (WLCSP20)

Footprint information for reflow soldering of HVQFN33 package

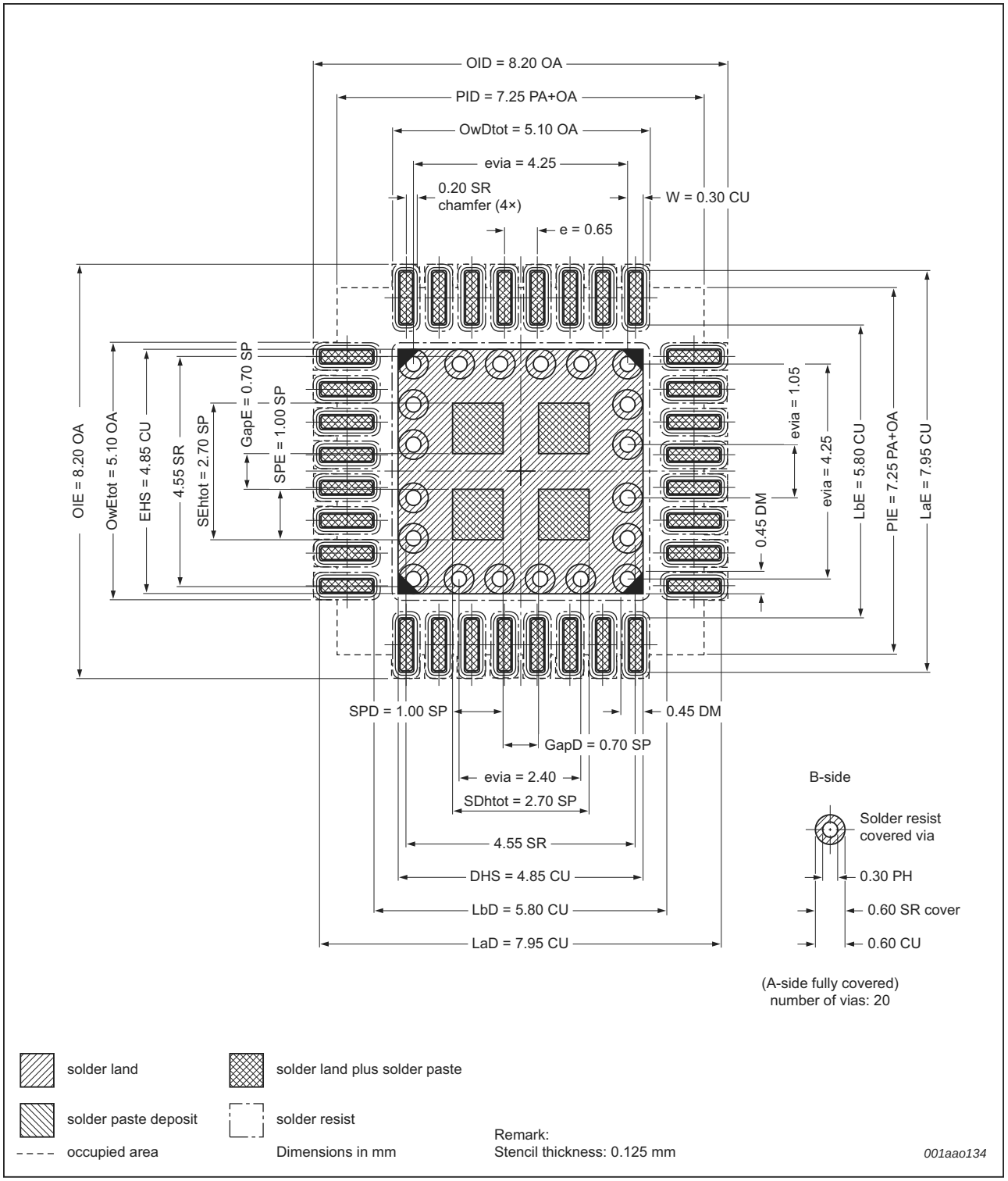
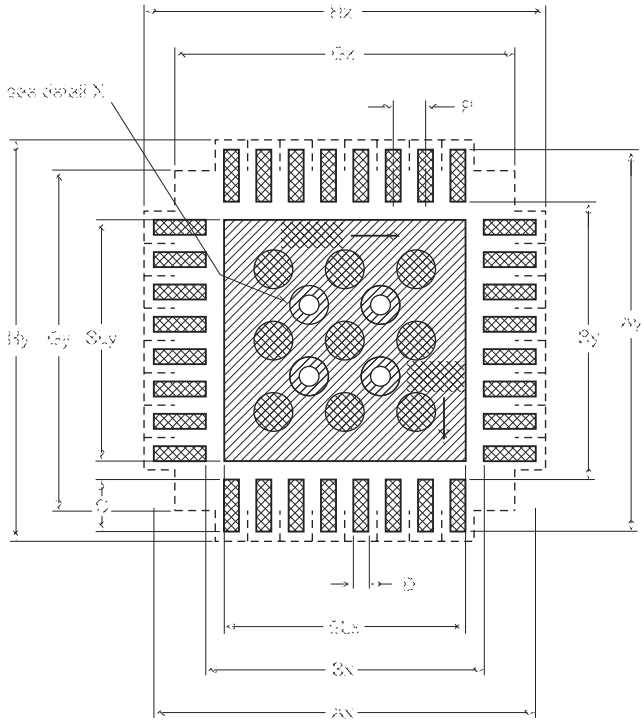
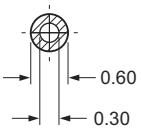


Fig 39. Reflow soldering of the HVQFN33(7x7) package

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 40. Reflow soldering of the HVQFN33(5x5) package

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