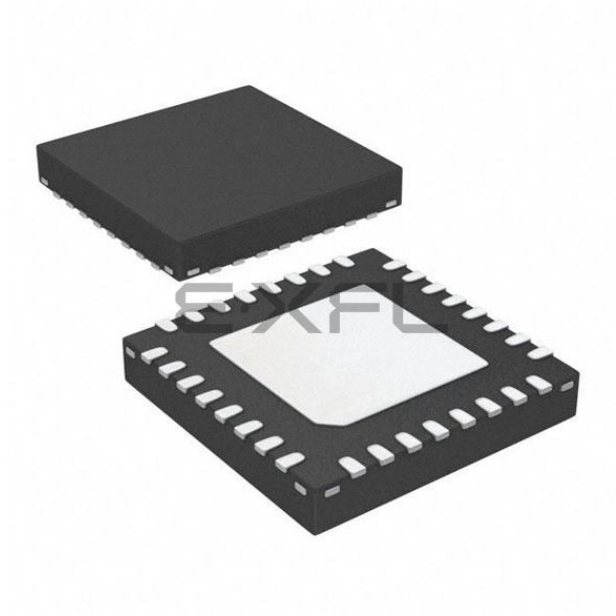

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a11fhn33-001

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$V_{DD(3V3)}$	Supply	-	-	44	29	E2
V_{SS}	Ground	-	-	42	33	E3
$V_{SS(IO)}$	Ground	-	-	5	33	E3

[1] Always on.

[2] Programmable on/off. By default, the glitch filter is disabled.

Table 4 shows all pins in order of their port number. The default function after reset is listed first. All port pins PIO0_0 to PIO1_9 have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_2 and PIO0_3.

Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON registers for each of the port pins.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
$\overline{\text{RESET}}$/PIO0_0	3	2	C1	[2]	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with fixed 20 ns glitch filter: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0.
					I/O	-	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/RXD/CLKOUT/ CT32B0_MAT2/SSEL0/ CLKIN	4	3	B2	[3]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	-	**RXD —** Receiver data input for USART.
					O	-	**CLKOUT —** Clock output.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I/O	-	**SSEL0 —** Slave Select for SSP0.
					I	-	**CLKIN —** External clock input.
PIO0_2/SCL/ACMP_O/ TCK/SWCLK/ CT16B0_CAP0	15	10	A1	[4][5]	I/O	I; IA	**PIO0_2 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**TCK/SWCLK —** Serial Wire Debug Clock (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWCLK function by the boot loader after reset.
					I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0. Input glitch filter (50 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_3/SDA/ACMP_O/ SWDIO/CT16B1_CAP0	16	11	B1	[4][6]	I/O	I; IA	**PIO0_3 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SDA —** I^2C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I/O	-	**SWDIO —** Serial Wire Debug I/O (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWDIO function by the boot loader after reset.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. Input glitch filter (50 ns) capable.
PIO0_4/R/AOUT/ CT16B0_MAT1/MOSI0	28	18	A4	[7]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**AOUT —** D/A converter output.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ R/CT16B0_MAT2/ SCK0	29	19	-	[9]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ VDDCMP/ CT16B0_MAT2/ SCK0	-	-	B3	[7][8]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and secondary Serial Wire Debug ClocK. Use PIO0_2 for the default TCK/SWCLK function. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/$\overline{\text{RTS}}$/ ACMP_O/ CT32B0_CAP0/SCLK	45	30	-	[3]	I/O	I; PU	**PIO0_23 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					I/O	-	**SCLK —** Serial clock for USART.
PIO0_24/SCL/CLKIN/ CT16B1_CAP0	9	7	-	[3]	I/O	I; PU	**PIO0_24 —** General purpose digital input/output pin.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN —** External clock input.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/ CT16B1_MAT0	17	12	-	[3]	I/O	I; PU	**PIO0_25 —** General purpose digital input/output pin.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10].
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/ CT16B1_CAP1/ CT32B0_CAP2	1	1	-	[3]	I/O	I; PU	**PIO0_26 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/ CT32B1_MAT1/ CT16B1_CAP2	43	28	-	[9]	I/O	I; PU	**PIO0_27 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I1 —** Analog comparator input 1.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/$\overline{\text{DTR}}$/SSEL1/ CT32B0_CAP0	2	-	-	[3]	I/O	I; PU	**PIO0_28 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO0_29/$\overline{\text{DSR}}$/SCK1/ CT32B0_CAP1	13	-	-	[3]	I/O	I; PU	**PIO0_29 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I^2C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

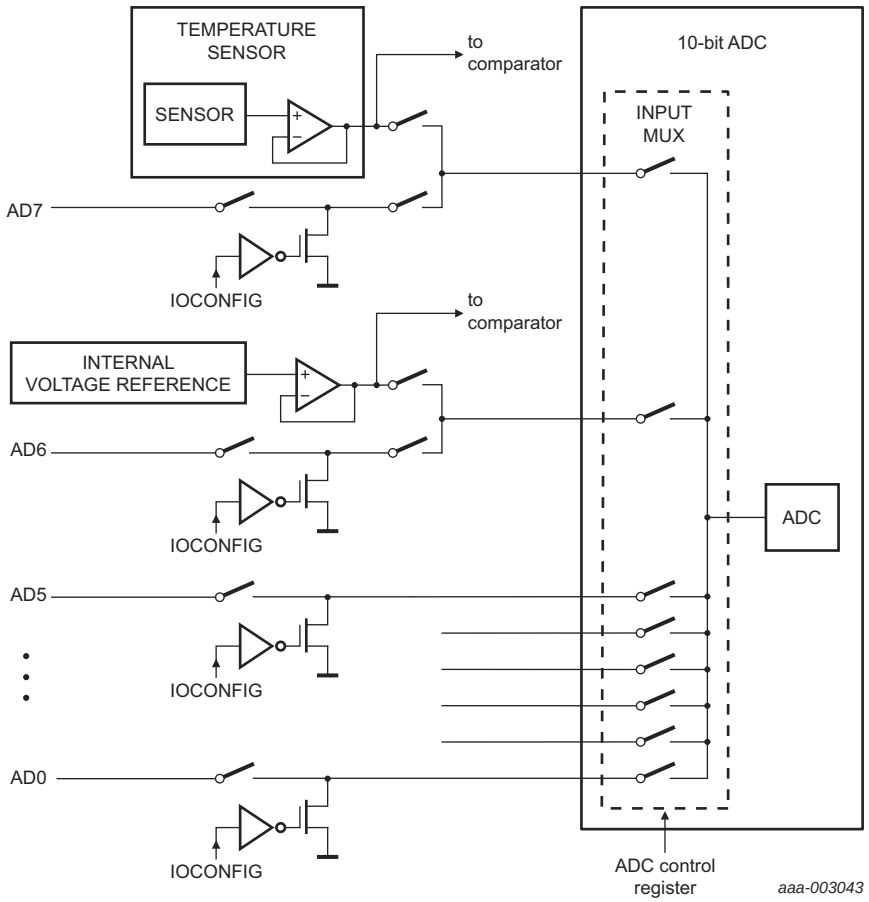


Fig 7. ADC block diagram

7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pins ATRG0 or ATRG1, timer match signal, or comparator output. (Input signals must be held for a minimum of three system clock periods). Also see Section 12.2.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.15 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V and varies typically only ±3 mV over the 0 °C to 85 °C temperature range (see Table 21 and Figure 27). The internal voltage reference can be used in the following applications:

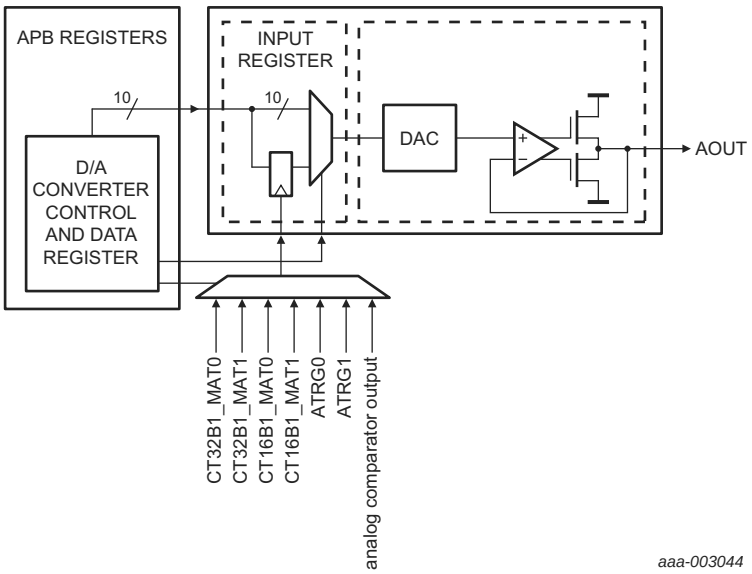


Fig 8. DAC block diagram

7.17.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
  - write operations to the DAC register.
  - a transition of pins ATRG0 or ATRG1. Input signals must be held for a minimum of three system clock periods.
  - a timer match signal.
  - a comparator output signal held for a minimum of two system clock periods.
- Holds output value during Sleep mode if the DAC is not powered down.

7.18 Analog comparator

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages. See Table 24.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

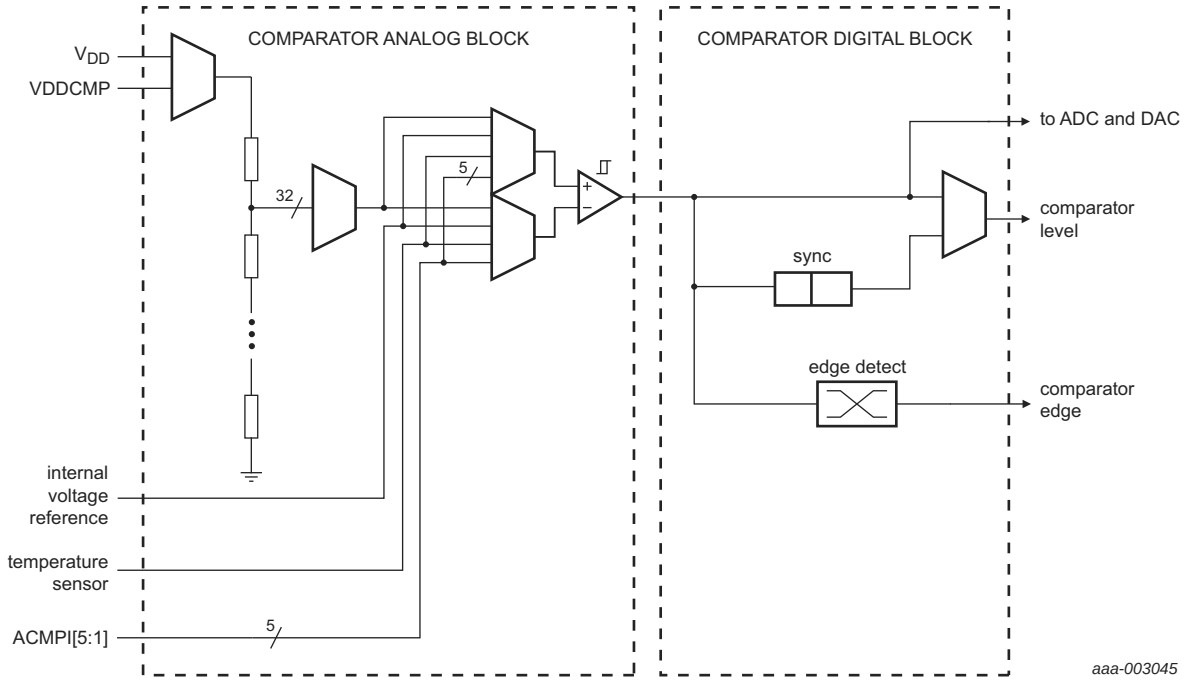


Fig 9. Comparator block diagram

7.18.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Five selectable external voltages; fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap and temperature sensor selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel. See Table 24 to Table 26.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- Comparator output is internally connected to the ADC and DAC and can be used to trigger a conversion.
- The comparator output is also connected internally to capture channel 3 on each of the 32-bit and 16-bit counter/timers.

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−160	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−15	−50	−85	μA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_2 and PIO0_3)							
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3$V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.05$V_{DD(IO)}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as high-current sink pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[11]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; SysOsc disabled; system PLL disabled.

[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

[6] IRC disabled; SysOsc enabled; system PLL enabled.

[7] Including voltage on outputs in 3-state mode.

[8] All supply voltages must be present.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Does not apply to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package).

[11] To V_{SS}.

9.2 Peripheral power consumption

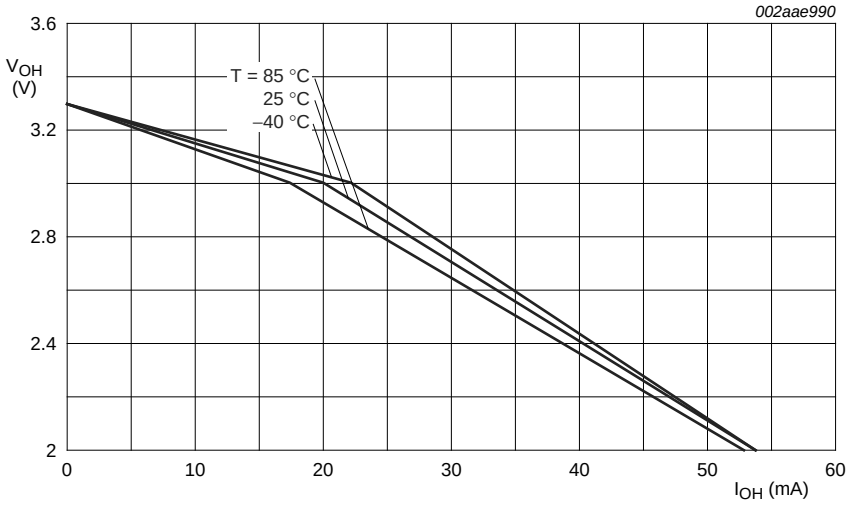
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

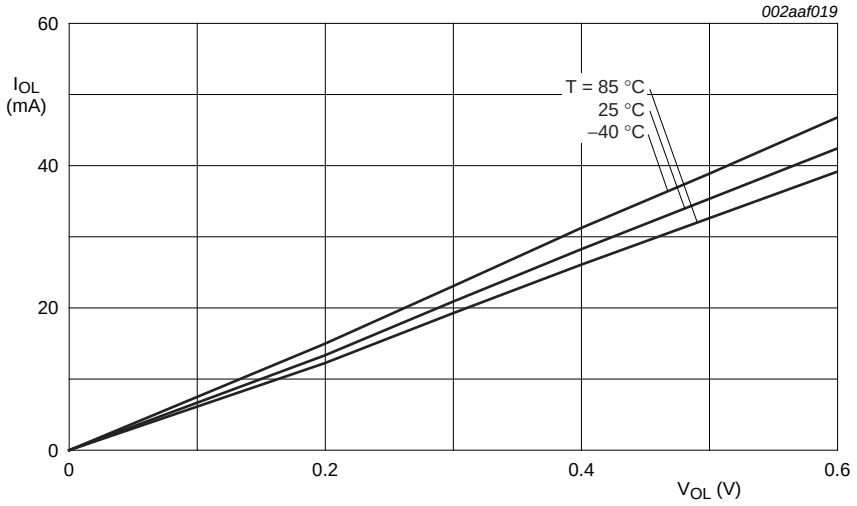
[1] IRC on; PLL off.

9.3 Electrical pin characteristics



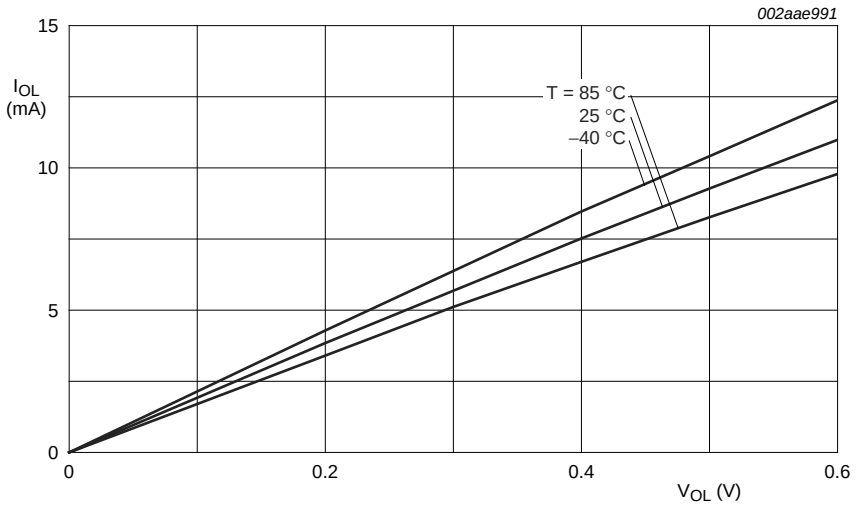
Conditions: $V_{DD(IO)}$ = 3.3 V; on pin PIO0_21.

Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; on pins PIO0_2 and PIO0_3.

Fig 15. High-current sink pins: Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins and PIO0_21.

Fig 16. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

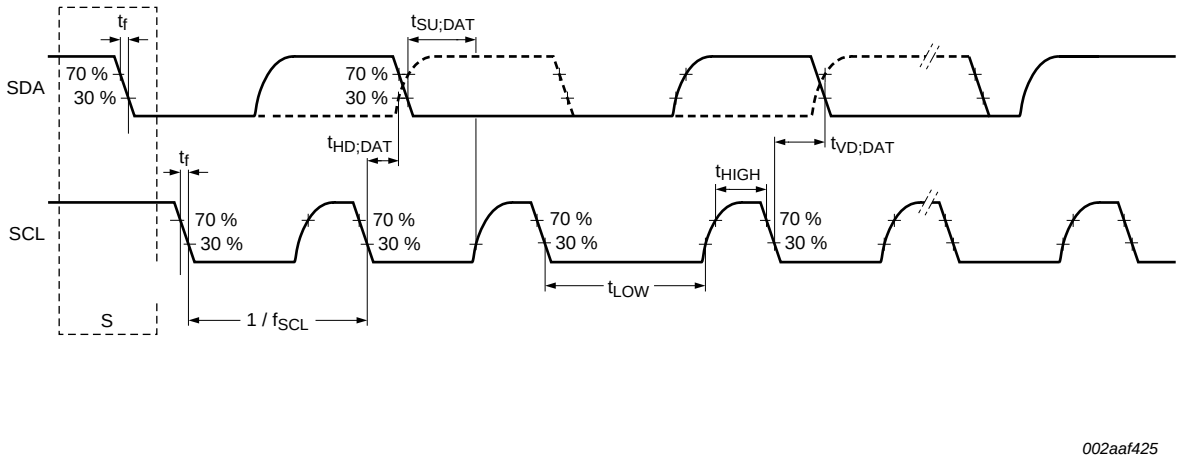


Fig 23. I^2C-bus pins clock timing

10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode
2.6 V <= $V_{DD(3V3)}$ = $V_{DD(IO)}$ <= 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1][1]	40			ns
t_{DS}	data set-up time	in SPI mode	[1][2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[1][2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[1][2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[1][2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)}$ = 3.3 V.

Table 22. Temperature sensor static and dynamic characteristics
$V_{DD(3V3)}$ = 2.6 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +85 °C	[1]	-	-	±3	°C
E_L	linearity error	T_{amb} = −40 °C to +85 °C		-	-	±1.1	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	81	85	µs
$t_{s(sw)}$	switching settling time	to 99% of temperature sensor output value	[2][3]	-	1.5	2	µs

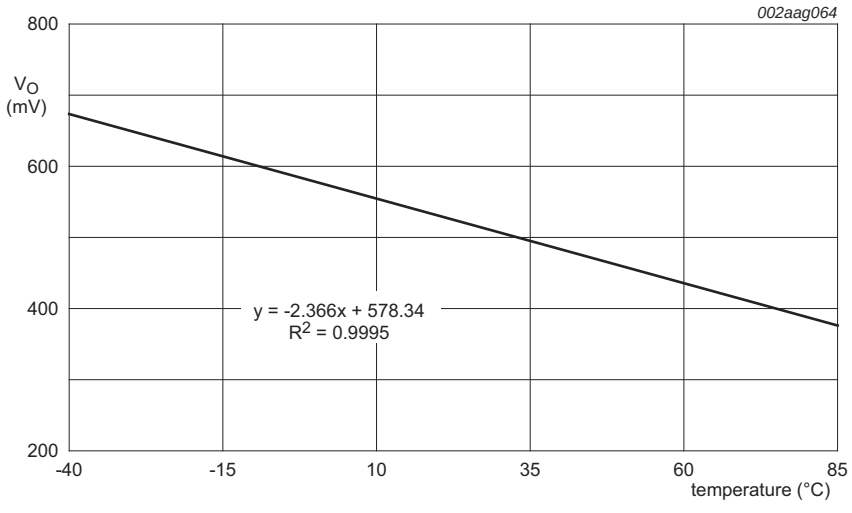
[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation ($V_{DD(3V3)}$ = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation ($V_{DD(3V3)}$ = 2.6 V; T_{amb} = 85 °C; slow process models).

[3] Settling time applies to switching between comparator and ADC channels.

Table 23. Temperature sensor Linear-Least-Square (LLS) fit parameters
$V_{DD(3V3)}$ = 2.6 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = 0 °C to 85 °C	-	−2.36	-	mV/°C
	T_{amb} = −40 °C to +85 °C	-	−2.36	-	mV/°C
LLS intercept	T_{amb} = 0 °C to 85 °C	-	577	-	mV
	T_{amb} = −40 °C to +85°C	-	576	-	mV



$V_{DD(3V3)}$ = 3.3 V; measured on a typical silicon sample.

Fig 28. Typical LLS fit of the temperature sensor output voltage

Table 25. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation ($V_{DD(3V3)}$ = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

Table 26. Comparator voltage ladder reference static characteristics
$V_{DD(3V3)}$ = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal $V_{DD(3V3)}$ supply					
		decimal code = 00	[2]	-	0	0	%
		decimal code = 08		-	0	±0.4	%
		decimal code = 16		-	–0.2	±0.2	%
		decimal code = 24		-	–0.2	±0.2	%
		decimal code = 30		-	–0.1	±0.1	%
		decimal code = 31		-	–0.1	±0.1	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		-	0	0	%
		decimal code = 08		-	–0.1	±0.5	%
		decimal code = 16		-	–0.2	±0.4	%
		decimal code = 24		-	–0.2	±0.3	%
		decimal code = 30		-	–0.2	±0.2	%
		decimal code = 31		-	–0.1	±0.1	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 µV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC11Axx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

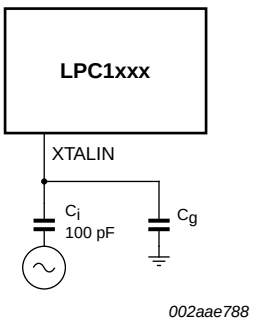


Fig 29. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 30 and in Table 27 and Table 28. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

12.6 Reset pad configuration

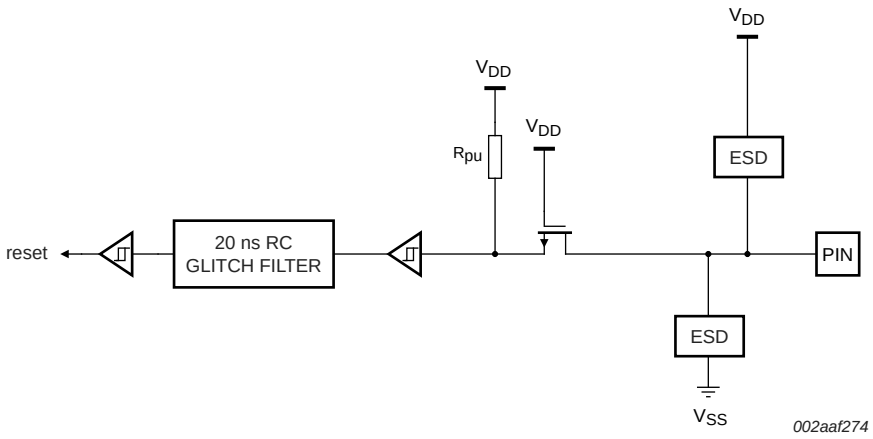


Fig 32. Reset pad configuration

12.7 UVLO protection and reset timer circuit

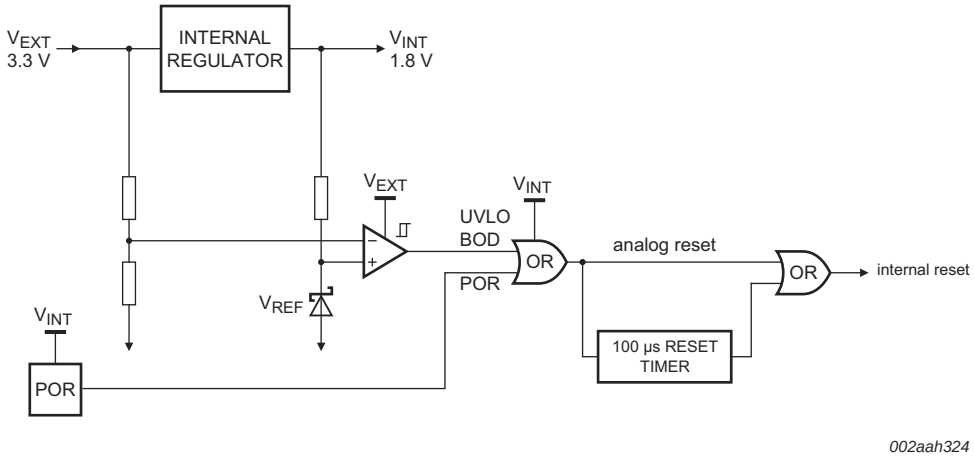


Fig 33. Functional diagram of the UVLO protection and reset timer circuit

12.8 Guidelines for selecting a power supply filter for UVLO protection

For the UVLO circuits to hold the part in reset during shallow and deep brown-out conditions, you must filter the power supply line to allow for the BOD and POR circuits to settle when short voltage drops occur (see Section 10.1 “Power supply fluctuations”).

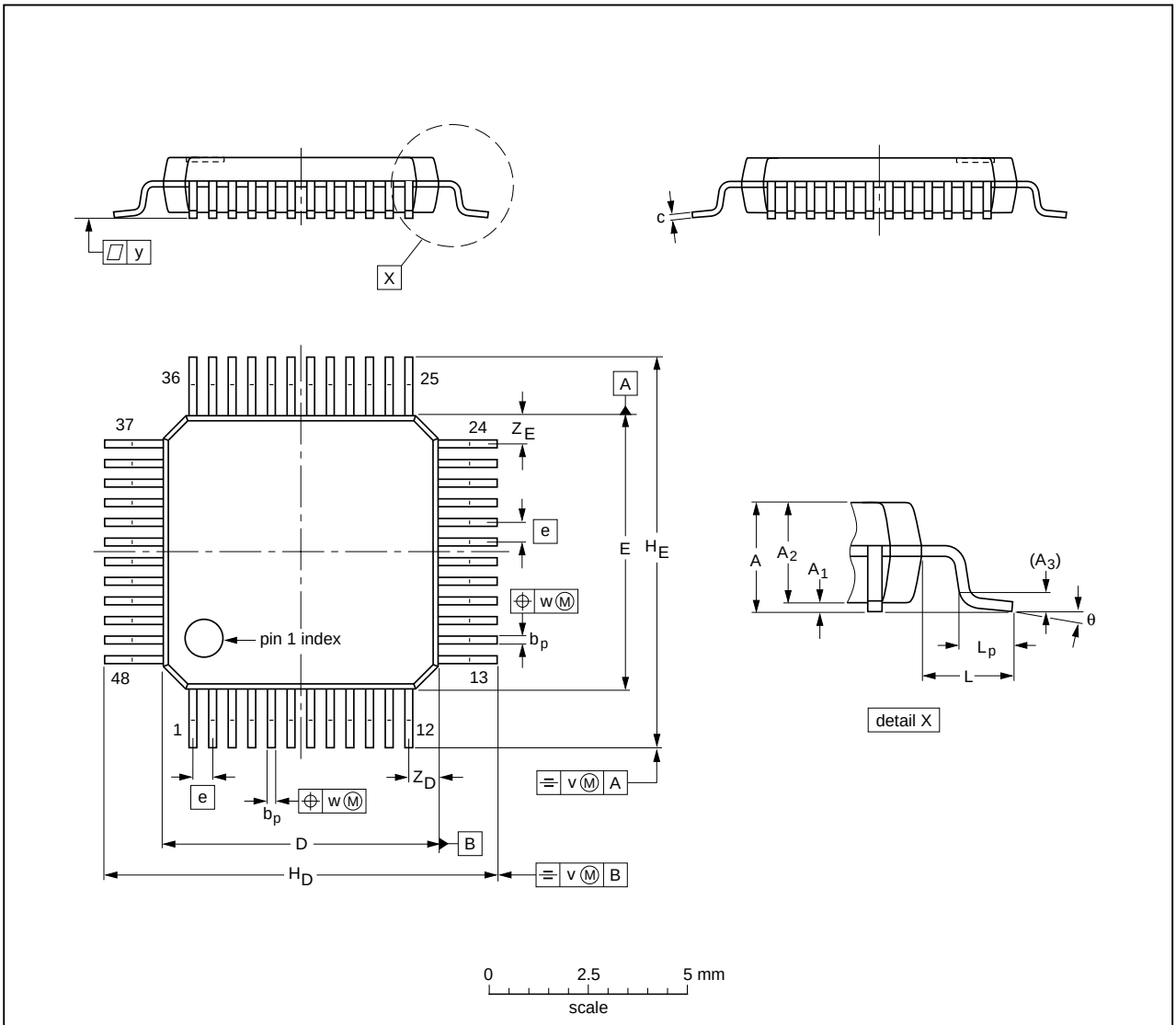
Select the capacitance of the decoupling/bypass capacitor according to the following guidelines:

$C >> I_{DD} \times t_s/\Delta V_{DD(3V3)}$ with

- $\Delta V_{DD(3V3)} \approx 100$ mV for the voltage drop below the BOD or POR trip points.
- $I_{DD} \approx 3$ mA with the IRC running and PLL/SysOsc off (see Figure 12).

13. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

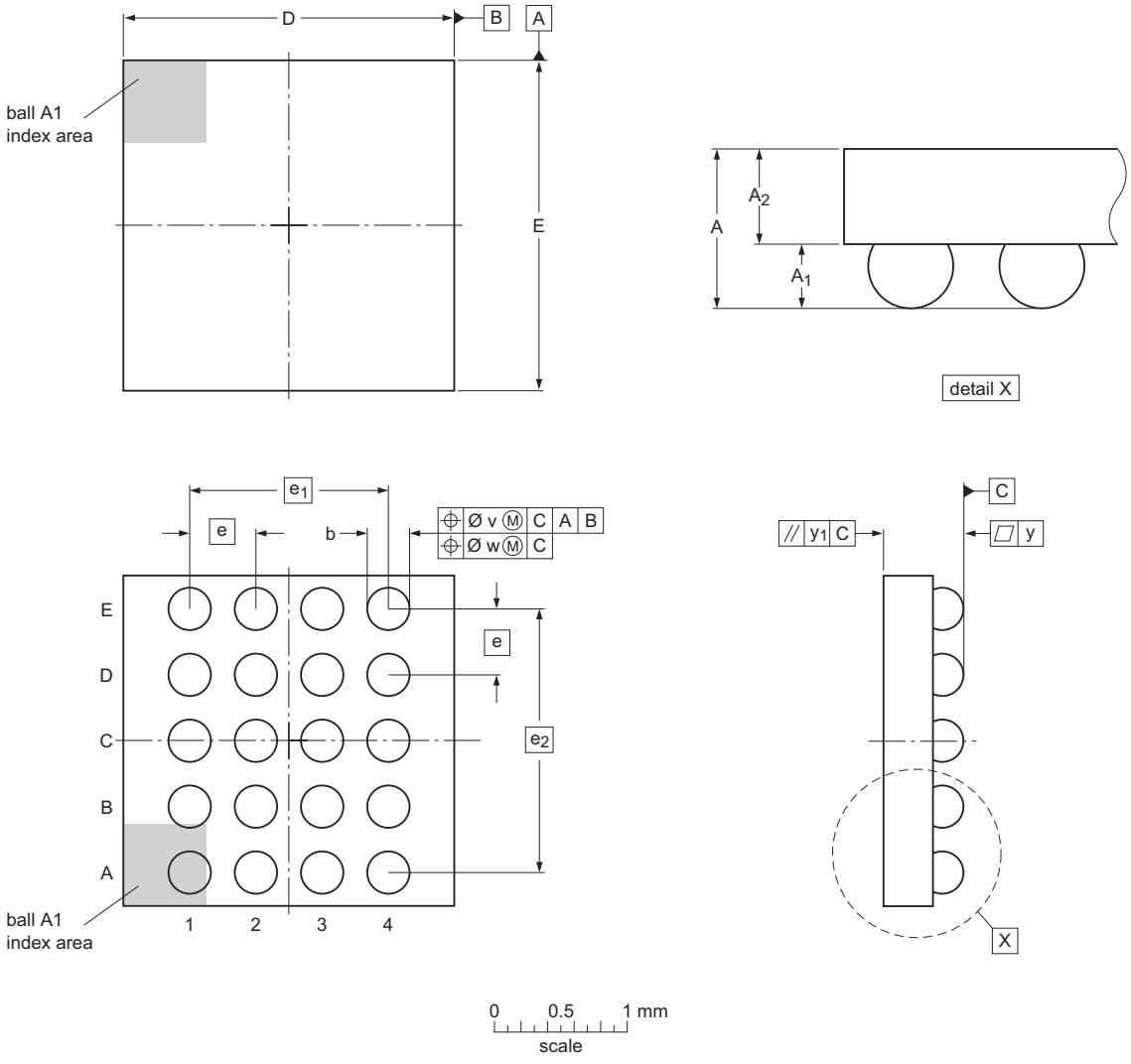
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 34. Package outline LQFP48

WLCSP20: wafer level chip-size package; 20 bumps; 2.5 x 2.5 x 0.6 mm **LPC11AxxUK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.65	0.27	0.38	0.35	2.60	2.60						
mm	nom	0.60	0.24	0.36	0.32	2.55	2.55	0.5	1.5	2.0	0.15	0.05	0.05
	min	0.55	0.21	0.34	0.29	2.50	2.50						

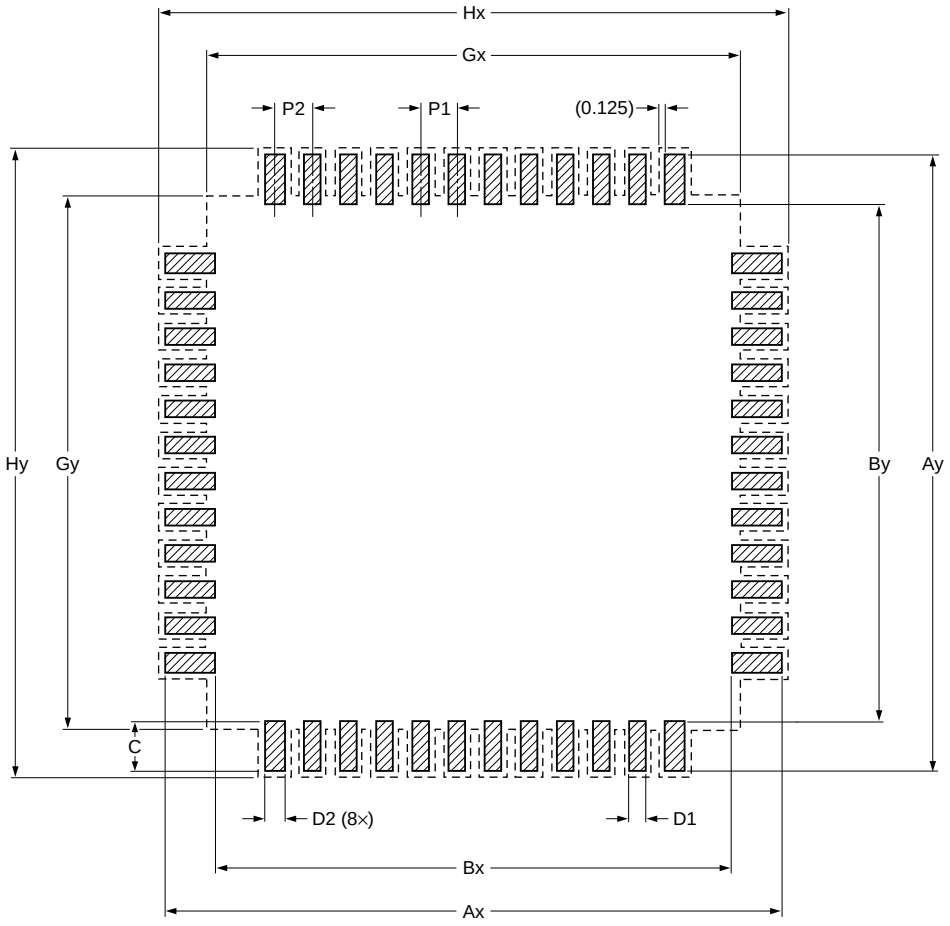
wlcsp20_lpc11axxuk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC11AxxUK						12-03-26

Fig 37. Package outline (WLCSP20)

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 38. Reflow soldering of the LQFP48 package

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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