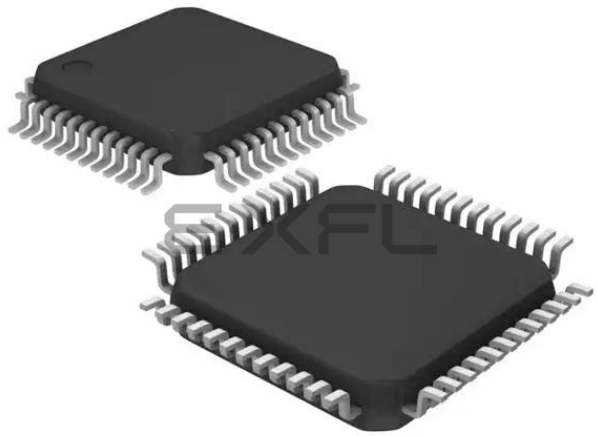

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a12fbd48-101

- Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

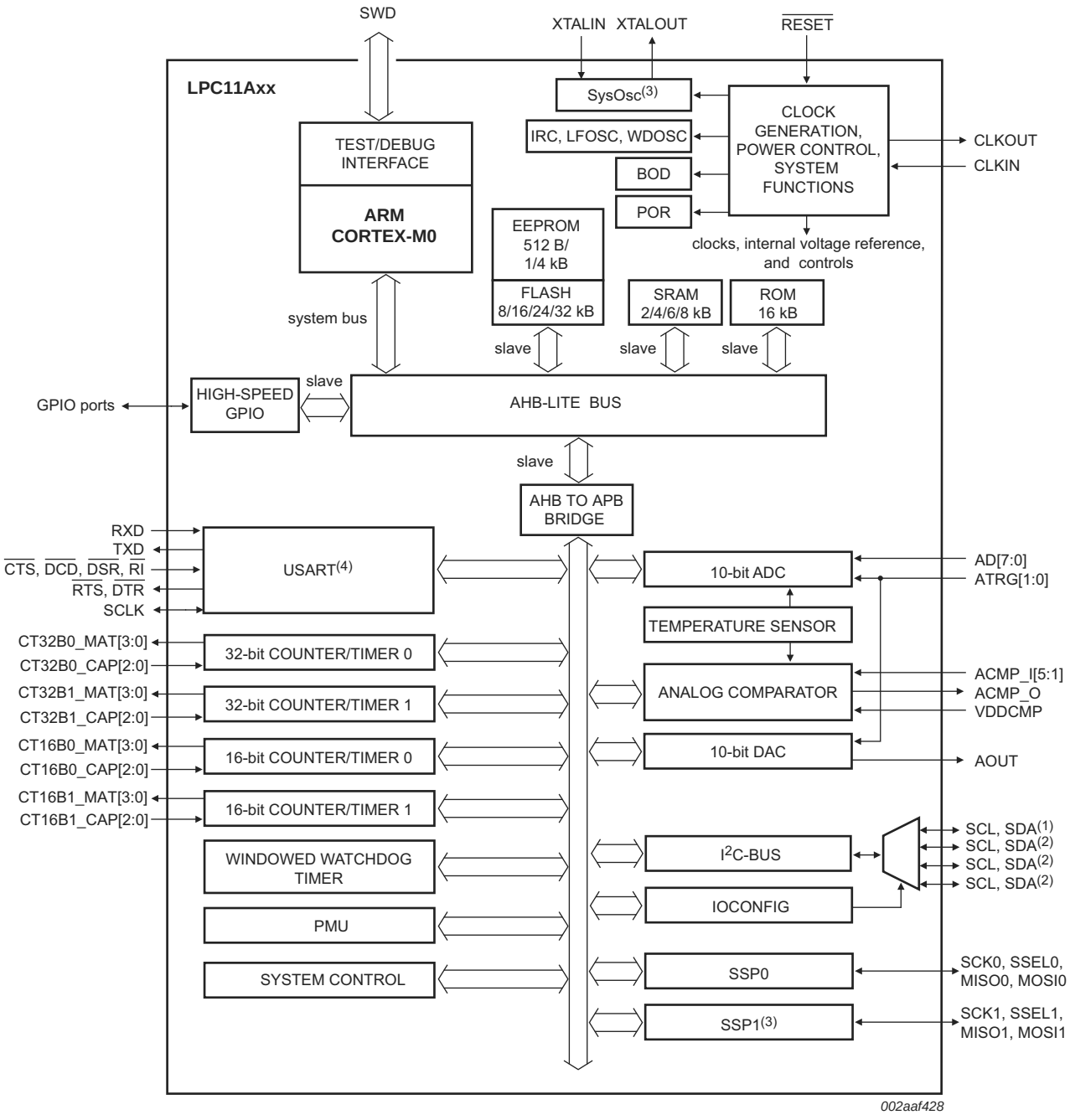
- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC with flexible conversion triggering.
  - Highly flexible analog comparator with a programmable voltage reference.
  - Integrated temperature sensor.
  - Internal voltage reference.
  - UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports one reduced power mode: The ARM Sleep mode.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM	EEPROM	10-bit ADC channels	10-bit DAC	Temperature sensor	Analog comparator	USART	SSP/SPI	I^2C	GPIO	Package
LPC11A02UK	16 kB	4 kB	2 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A04UK	32 kB	8 kB	4 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A11FHN33/001	8 kB	2 kB	512 B	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FHN33/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FBD48/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	42	LQFP48
LPC11A13FHI33/201	24 kB	6 kB	2 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FHN33/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FBD48/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	42	LQFP48

5. Block diagram



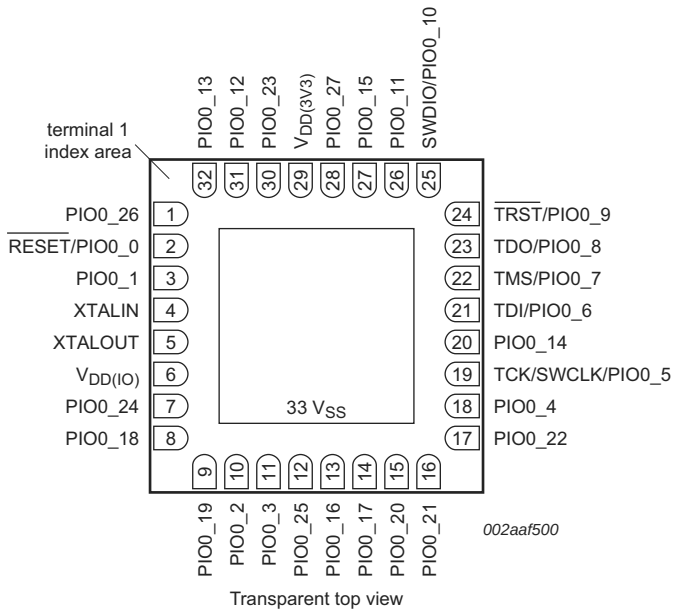
(1) Open-drain pins.

(2) Standard I/O pins.

(3) Not available on WLCSP packages.

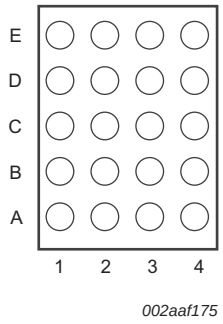
(4) Modem control pins not available on WLCSP packages.

Fig 1. LPC11Axx block diagram



Parts: LPC11A11FHN33/001, LPC11A12FHN33/101, LPC11A13FHI33/201, LPC11A14FHN33/301

Fig 3. Pin configuration HVQFN 33 package



Parts: LPC11A02UK, LPC11A04UK

Fig 4. Pin configuration WLCSP20 package

6.2 Pin description

All functional pins on the LPC11Axx are mapped to GPIO port 0 and port 1 (see Table 4). The port pins are multiplexed to accommodate more than one function (see Table 3).

The pin function is controlled by the pin's IOCON register (see the *LPC11Axx user manual*). The standard I/O pad configuration is illustrated in Figure 31 and a detailed pin description is given in Table 4.

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$\overline{RI}$	I	PIO0_30	no	40	-	-
		PIO0_31	no	24	-	-
		PIO1_3	no	48	-	-
16-bit counter/timer CT16B0						
CT16B0_CAP0	I	PIO0_2	50 ns[2]	15	10	A1
		PIO0_18	no	10	8	-
		PIO0_30	no	40	-	-
CT16B0_CAP1	I	PIO0_16	10 ns[2]	18	13	A2
		PIO1_4	no	19	-	-
CT16B0_CAP2	I	PIO0_17	10 ns[2]	21	14	A3
		PIO1_5	no	20	-	-
CT16B0_MAT0	O	PIO0_7	no	33	22	C4
		PIO0_17	no	21	14	A3
		PIO1_6	no	11	-	-
CT16B0_MAT1	O	PIO0_4	no	28	18	A4
		PIO0_9	no	35	24	D4
		PIO1_0	no	31	-	-
CT16B0_MAT2	O	PIO0_5	no	29	19	B3
		PIO0_10	no	38	25	D3
		PIO1_7	no	25	-	-
16-bit counter/timer CT16B1						
CT16B1_CAP0	I	PIO0_3	50 ns[2]	16	11	B1
		PIO0_24	no	9	7	-
		PIO1_3	no	48	-	-
CT16B1_CAP1	I	PIO0_18	no	10	8	-
		PIO0_26	no	1	1	-
		PIO0_31	no	24	-	-
CT16B1_CAP2	I	PIO0_27	10 ns[2]	43	28	-
		PIO1_7	no	25	-	-
CT16B1_MAT0	O	PIO0_19	no	14	9	-
		PIO0_25	no	17	12	-
		PIO1_1	no	36	-	-
CT16B1_MAT1	O	PIO0_14	no	30	20	B4
		PIO1_2	no	37	-	-
		PIO1_8	no	26	-	-
CT16B1_MAT2	O	PIO0_20	no	22	15	-
		PIO1_2	no	37	-	-
		PIO1_9	no	12	-	-

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
TDI/PIO0_6/AD0/ CT32B0_MAT3/MISO0	32	21	C3	[9]	I	I; PU	**TDI —** Test Data In for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_6 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD0 —** A/D converter input 0.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I/O	-	**MISO0 —** Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
TMS/PIO0_7/AD1/ CT32B1_CAP0/ CT16B0_MAT0	33	22	C4	[9]	I	I; PU	**TMS —** Test Mode Select for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_7 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD1 —** A/D converter input 1.
					I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0 —** Match output 2 for 16-bit timer 0.
TDO/PIO0_8/AD2/ CT32B1_MAT0/SCK1	34	23	C2	[9]	O	I; PU	**TDO —** Test Data Out for JTAG interface.
					I/O	-	**PIO0_8 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD2 —** A/D converter input 2.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I/O	-	**SCK1 —** Serial clock for SSP1. Input glitch filter (10 ns) capable.
$\overline{\text{TRST}}$/PIO0_9/AD3/ CT32B1_MAT1/ CT16B0_MAT1/$\overline{\text{CTS}}$	35	24	D4	[9]	I	I; PU	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_9 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD3 —** A/D converter, input 3.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1/ VDDCMP	30	20	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1	-	-	B4	[9]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO0_15/TXD/AD7/ CT32B0_CAP2/SDA	41	27	E4	[9]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					O	-	**TXD —** Transmitter data output for USART.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
PIO0_16/ ATRG0/ACMP_I3/ CT16B0_CAP1/SCL	18	13	A2	[9]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**ATRG0 —** Conversion trigger 0 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I3 —** Analog comparator input 3.
					I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.

- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight GPIO pins, regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both. The interrupt generating GPIOs can be selected from the GPIO pins with a configurable input glitch filter.

7.8 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Up to 16 pins can be configured with a digital input glitch filter for removing voltage glitches with widths of 10 ns or less (see Table 3 and Table 4), two pins (PIO0_2 and PIO0_3) can be configured with a 50 ns digital input glitch filter.

7.9 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11Axx use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- An entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.9.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 31 and Figure 32 for functional diagrams).

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	−0.5	4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	−0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	−0.5	+5.5	V
		on pins PIO0_2 and PIO0_3	[5]	−0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	−0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[11]	−6.5	+6.5	kV
V_{trig}	trigger voltage	for LVTSCR based ESD pin protection; 1 ns to 10 ns rise time	[12]	8.2	-	V
		> 10 ns rise time		> 8.5	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

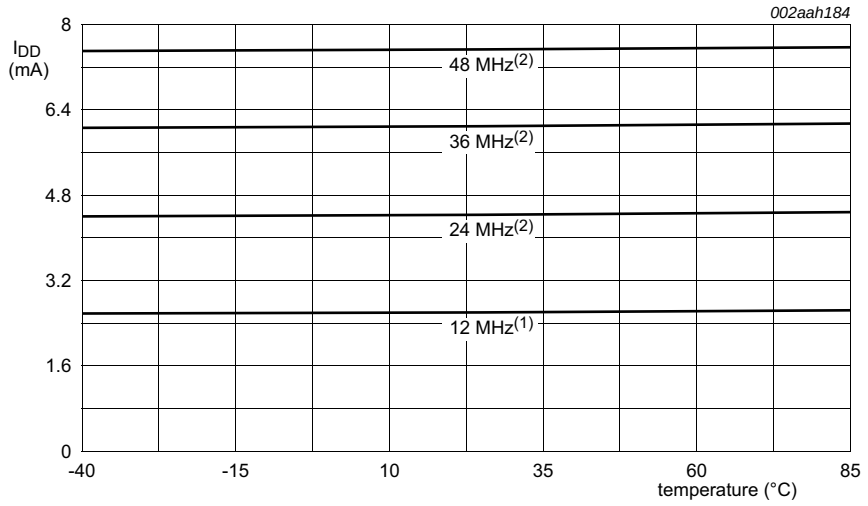
[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_2 and PIO0_3 and except the 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).

9.1 Power consumption

Power measurements in Active and Sleep modes were performed under the following conditions (see *LPC11Axx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIO DIR registers to drive the outputs LOW.

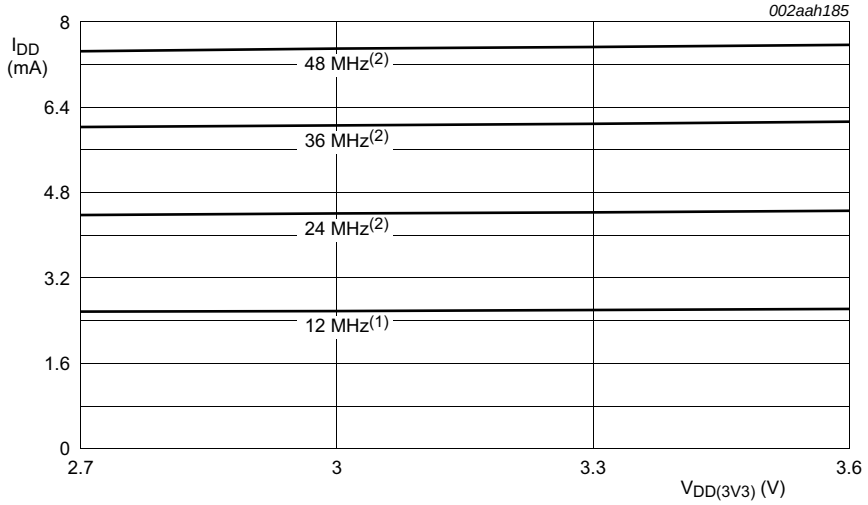


Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 11. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals disabled)

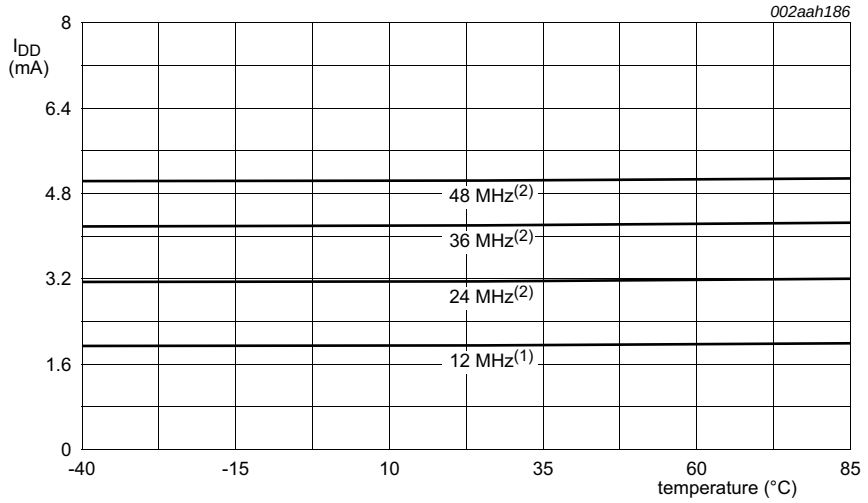


Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 12. Active mode: Typical supply current I_{DD} versus core voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals disabled)



Conditions: $V_{DD(3V3)}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register and PDRUNCFG register; all peripheral clocks disabled; BOD disabled; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 13. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies (all peripherals disabled)

9.2 Peripheral power consumption

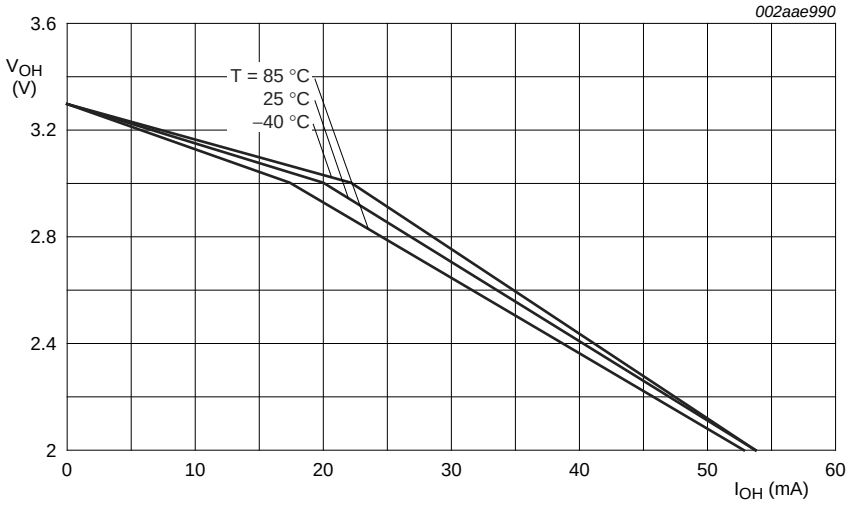
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

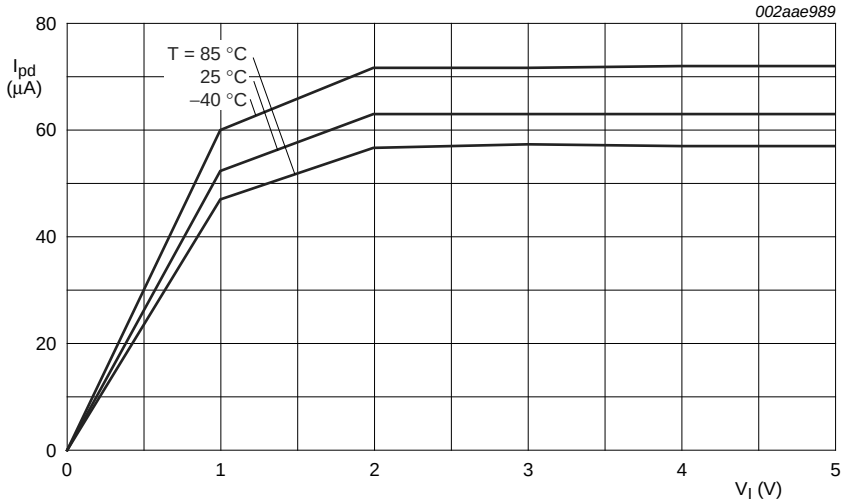
[1] IRC on; PLL off.

9.3 Electrical pin characteristics



Conditions: $V_{DD(IO)}$ = 3.3 V; on pin PIO0_21.

Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 19. Typical pull-down current I_{pd} versus input voltage V_I

Table 24. Comparator characteristics

$V_{DD(3V3)}$= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{DD}	supply current			-	55	-	μA
V_{IC}	common-mode input voltage			0	-	$V_{DD(3V3)}$	V
DV_O	output voltage variation			0	-	$V_{DD(3V3)}$	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	−4 to +4.2	-	mV
		V_{IC} = 1.5 V		-	±2	-	mV
		V_{IC} = 2.8 V		-	±2.5		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	μs
t_{PD}	propagation delay	HIGH to LOW; $V_{DD(3V3)}$ = 3.0 V;		-			
		V_{IC} = 0.1 V; 50 mV overdrive input	[1]		129	140	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	210	250	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	112	130	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	127	160	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	151	170	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	57	70	ns
t_{PD}	propagation delay	LOW to HIGH; $V_{DD(3V3)}$ = 3.0 V;		-			
		V_{IC} = 0.1 V; 50 mV overdrive input	[1]		232	240	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	58	60	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	210	230	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	178	200	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	166	190	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	333	550	ns
V_{hys}	hysteresis voltage	positive hysteresis; $V_{DD(3V3)}$ = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; $V_{DD(3V3)}$ = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

12.4 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.5 Standard I/O pad configuration

Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on 17 pins.
- Analog input

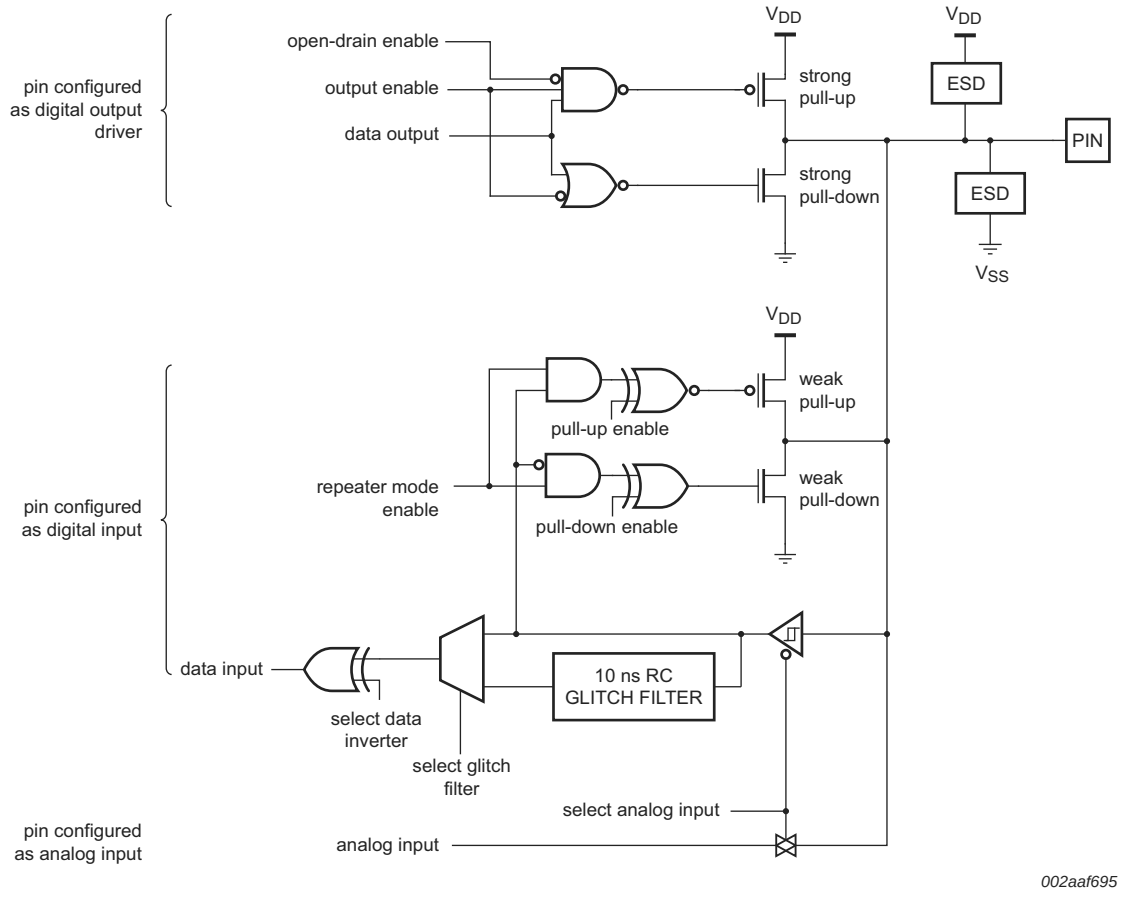
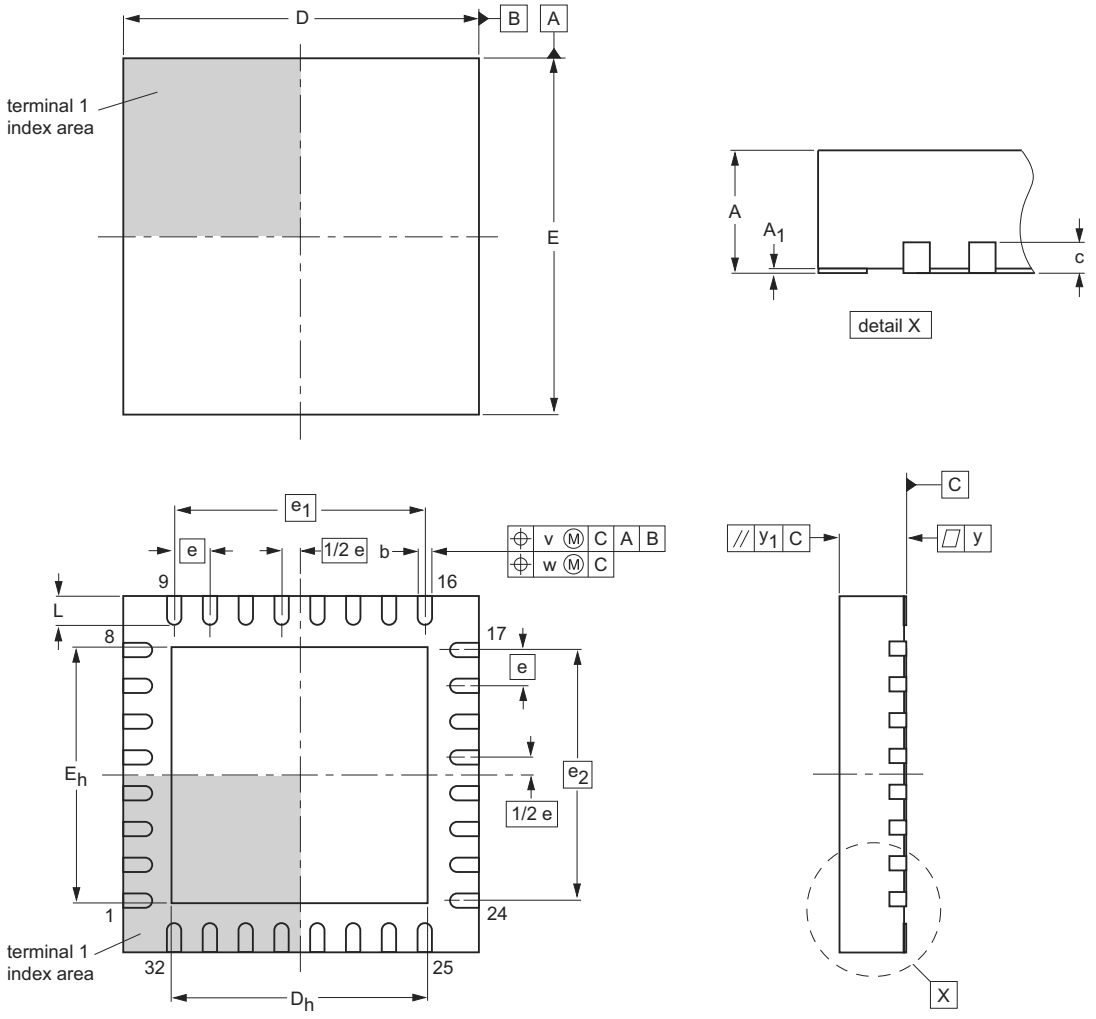


Fig 31. Standard I/O pad configuration

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

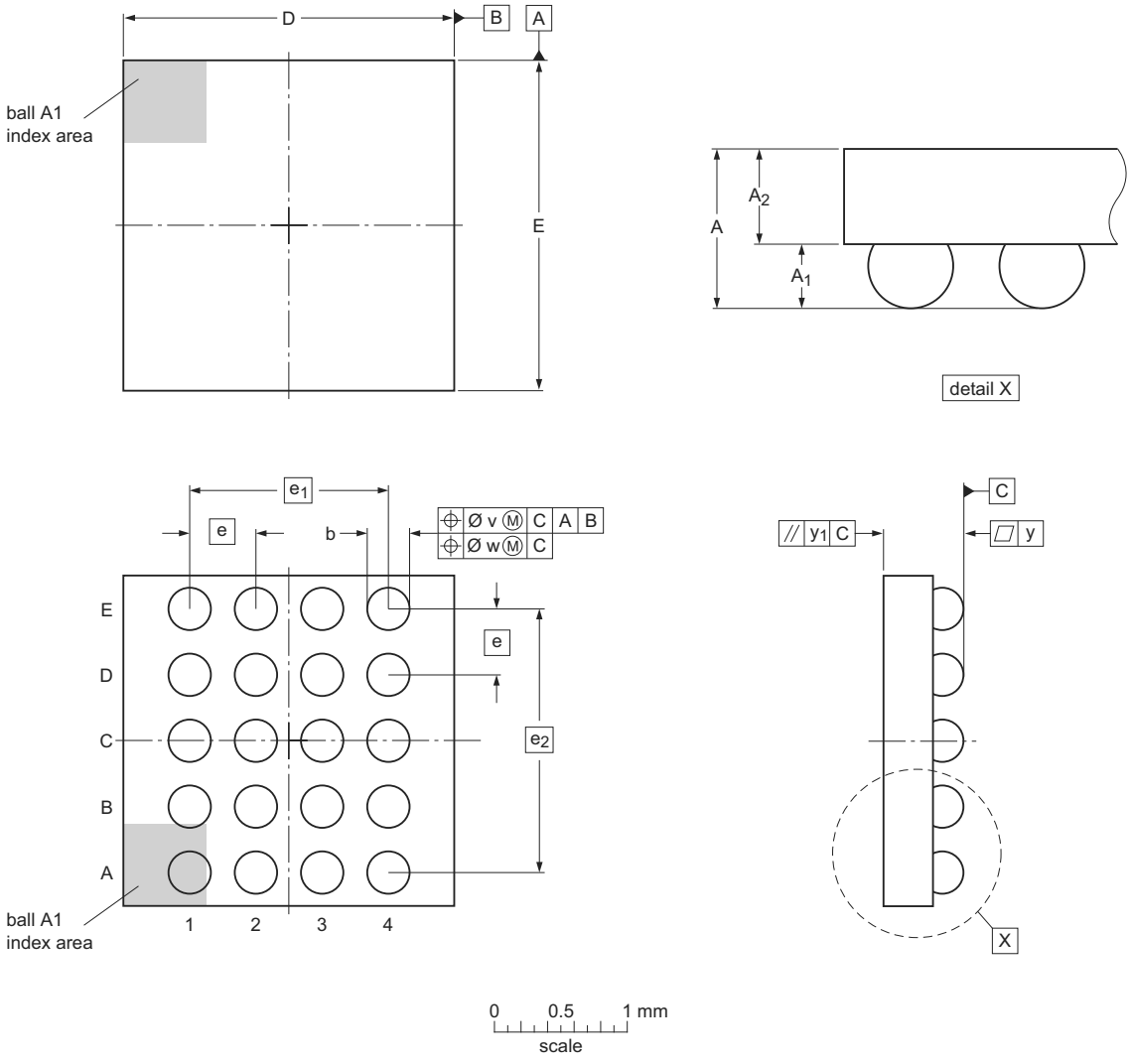
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 36. Package outline HVQFN33 (5x5)

WLCSP20: wafer level chip-size package; 20 bumps; 2.5 x 2.5 x 0.6 mm **LPC11AxxUK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.65	0.27	0.38	0.35	2.60	2.60						
mm	nom	0.60	0.24	0.36	0.32	2.55	2.55	0.5	1.5	2.0	0.15	0.05	0.05
	min	0.55	0.21	0.34	0.29	2.50	2.50						

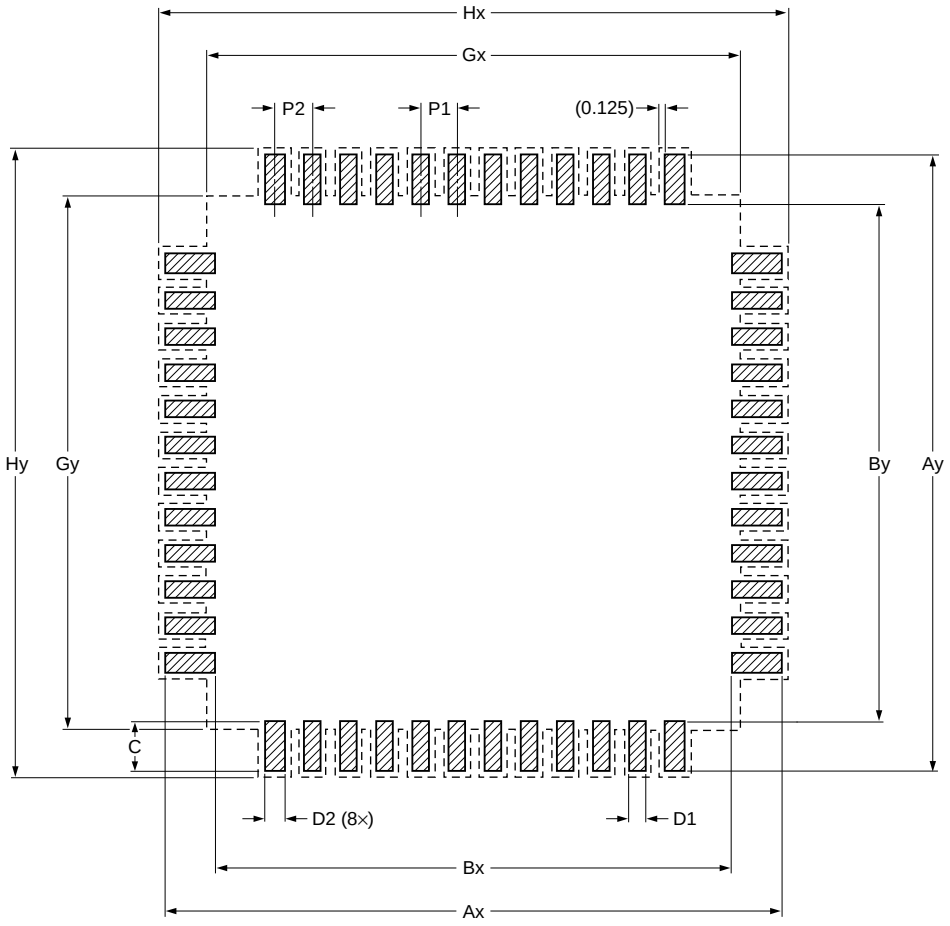
wlcsp20_lpc11axxuk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC11AxxUK						12-03-26

Fig 37. Package outline (WLCSP20)

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 38. Reflow soldering of the LQFP48 package

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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19. Contents

1 General description 1
2 Features and benefits 1
3 Applications 3
4 Ordering information 3
4.1 Ordering options 4
5 Block diagram 5
6 Pinning information 6
6.1 Pinning 6
6.2 Pin description 7
7 Functional description 23
7.1 ARM Cortex-M0 processor 23
7.2 On-chip flash program memory 23
7.3 On-chip EEPROM data memory 23
7.4 On-chip SRAM 23
7.5 On-chip ROM 23
7.6 Memory map 23
7.7 Nested Vectored Interrupt Controller (NVIC) . 24
7.7.1 Features 24
7.7.2 Interrupt sources 25
7.8 IOCON block 25
7.9 Fast general purpose parallel I/O 25
7.9.1 Features 25
7.10 USART 26
7.10.1 Features 26
7.11 SSP serial I/O controller 26
7.11.1 Features 26
7.12 I²C-bus serial I/O controller 26
7.12.1 Features 27
7.13 Configurable analog/mixed-signal subsystems 27
7.14 10-bit ADC 28
7.14.1 Features 29
7.15 Internal voltage reference 29
7.16 Temperature sensor 30
7.17 10-bit DAC 30
7.17.1 Features 31
7.18 Analog comparator 31
7.18.1 Features 32
7.19 General purpose external event counter/timers 33
7.19.1 Features 33
7.20 System tick timer 33
7.21 Windowed WatchDog Timer (WWDT) 33
7.21.1 Features 33
7.22 Clocking and power control 34
7.22.1 Crystal and internal oscillators 34
7.22.1.1 Internal RC Oscillator (IRC) 35
7.22.1.2 Crystal Oscillator (SysOsc) 35
7.22.1.3 Internal Low-Frequency Oscillator (LFOsc) and Watchdog Oscillator (WDOsc) 36
7.22.2 Clock input 36
7.22.3 System PLL 36
7.22.4 Clock output 36
7.22.5 Wake-up process 36
7.22.6 Power control 36
7.22.6.1 Sleep mode 36
7.22.6.2 Power profiles 37
7.23 System control 37
7.23.1 UnderVoltage LockOut (UVLO) protection . . . 37
7.23.2 Reset 37
7.23.3 Brown-out detection 38
7.23.4 Code security (Code Read Protection - CRP) 38
7.23.5 APB interface 38
7.23.6 AHBLite 38
7.23.7 External interrupt inputs 39
7.24 Emulation and debugging 39
8 Limiting values 40
9 Static characteristics 42
9.1 Power consumption 45
9.2 Peripheral power consumption 47
9.3 Electrical pin characteristics 47
10 Dynamic characteristics 51
10.1 Power supply fluctuations 51
10.2 Flash/EEPROM memory 51
10.3 External clock for oscillator in slave mode . . . 52
10.4 Internal oscillators 53
10.5 I/O pins 54
10.6 I²C-bus 54
10.7 SSP interfaces 56
11 Characteristics of analog peripherals 58
12 Application information 66
12.1 ADC usage notes 66
12.2 Use of ADC input trigger signals 66
12.3 XTAL input 66
12.4 XTAL Printed Circuit Board (PCB) layout guidelines 68
12.5 Standard I/O pad configuration 68
12.6 Reset pad configuration 69
12.7 UVLO protection and reset timer circuit 69
12.8 Guidelines for selecting a power supply filter for UVLO protection 69
13 Package outline 71
14 Soldering 75

continued >>