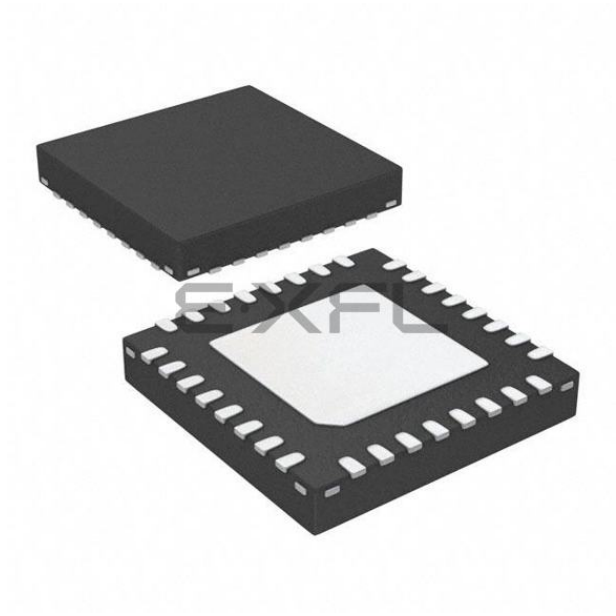

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a12fhn33-101

- Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC with flexible conversion triggering.
  - Highly flexible analog comparator with a programmable voltage reference.
  - Integrated temperature sensor.
  - Internal voltage reference.
  - UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports one reduced power mode: The ARM Sleep mode.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

- Single 3.3 V power supply (2.6 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP48 package, HVQFN33 (7 × 7) and HVQFN33 (5 × 5) packages, and in a very small WLCSP20 package.

3. Applications

- Power management
- Industrial control
- Remote monitoring
- Point-of-sale
- Test and measurement equipment
- Network appliances and services
- Factory automation
- Gaming equipment
- Motion control
- Medical instrumentation
- Fire and security
- Sensors
- Precision instrumentation
- HVAC and building control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11A02UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A04UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A11FHN33/001	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A13FHI33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11A14FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FBD48/101	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11A14FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_3/SDA/ACMP_O/ SWDIO/CT16B1_CAP0	16	11	B1	[4][6]	I/O	I; IA	**PIO0_3 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SDA —** I^2C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I/O	-	**SWDIO —** Serial Wire Debug I/O (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWDIO function by the boot loader after reset.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. Input glitch filter (50 ns) capable.
PIO0_4/R/AOUT/ CT16B0_MAT1/MOSI0	28	18	A4	[7]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**AOUT —** D/A converter output.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ R/CT16B0_MAT2/ SCK0	29	19	-	[9]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ VDDCMP/ CT16B0_MAT2/ SCK0	-	-	B3	[7][8]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and secondary Serial Wire Debug ClocK. Use PIO0_2 for the default TCK/SWCLK function. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I^2C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

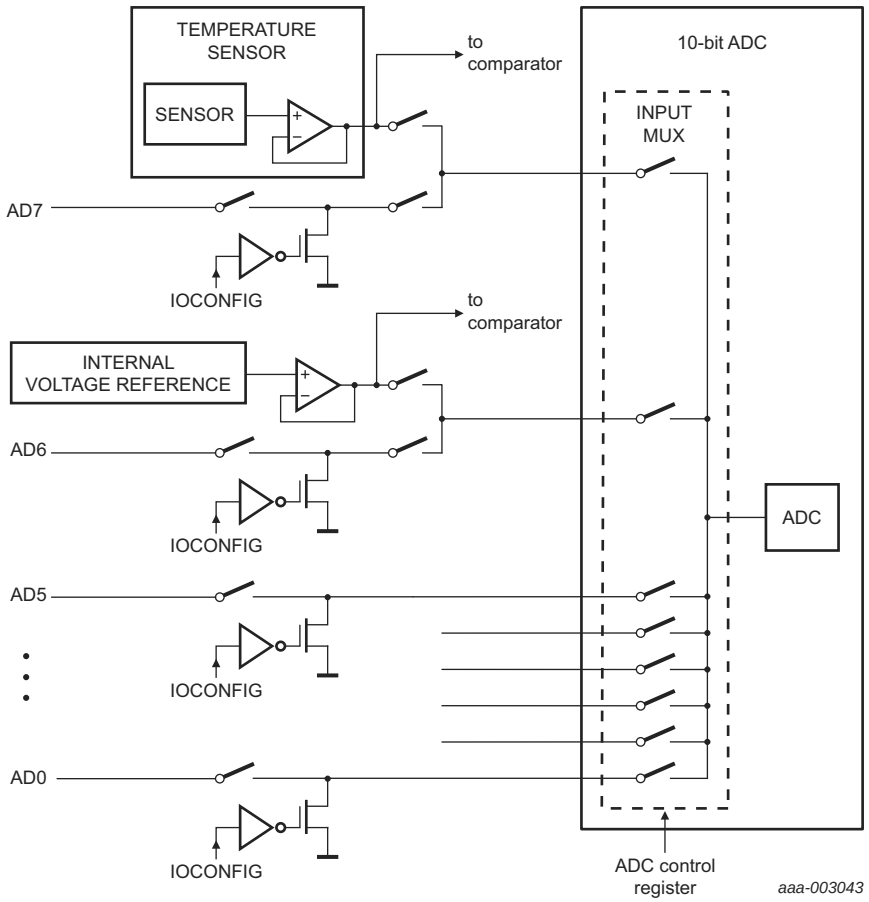


Fig 7. ADC block diagram

7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pins ATRG0 or ATRG1, timer match signal, or comparator output. (Input signals must be held for a minimum of three system clock periods). Also see Section 12.2.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.15 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V and varies typically only ±3 mV over the 0 °C to 85 °C temperature range (see Table 21 and Figure 27). The internal voltage reference can be used in the following applications:

7.19 General purpose external event counter/timers

The LPC11Axx includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt. Up to three capture channels are pinned out. One channel is internally connected to the comparator output ACMP_O.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.20 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.21 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.22.6.2 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11Axx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.23 System control

7.23.1 UnderVoltage LockOut (UVLO) protection

The BOD and POR circuits remain enabled at all times to provide UVLO protection from an unexpected power supply droop below a typical threshold level of 2.4 V (see also the *LPC11Axx user manual*). UVLO protection means that the LPC11Axx is held in reset whenever the supply voltage falls below 2.4 V.

See also Section 10.1 “Power supply fluctuations”, Section 12.7 “UVLO protection and reset timer circuit”, and Section 12.8 “Guidelines for selecting a power supply filter for UVLO protection”.

7.23.2 Reset

Reset has several sources on the LPC11Axx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), the ARM SYSRESETREQ software request, and the Brown-Out Detection (BOD) circuit. After the BOD and the POR resets are released, the internal reset timer counts for 100 µs until the internal reset is removed.

Assertion of chip reset by any source (after the operating voltage attains a usable level) starts the IRC and initializes the flash memory controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

Writing to a special function register allows the software to reset the following peripherals: the I^2C-bus interface, the USART, both SSP controllers, the four counter/timers, the comparator, the ADC, and the DAC.

The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin and uses a special pad. See Figure 32.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	−0.5	4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	−0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	−0.5	+5.5	V
		on pins PIO0_2 and PIO0_3	[5]	−0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	−0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[11]	−6.5	+6.5	kV
V_{trig}	trigger voltage	for LVTSCR based ESD pin protection; 1 ns to 10 ns rise time	[12]	8.2	-	V
		> 10 ns rise time		> 8.5	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

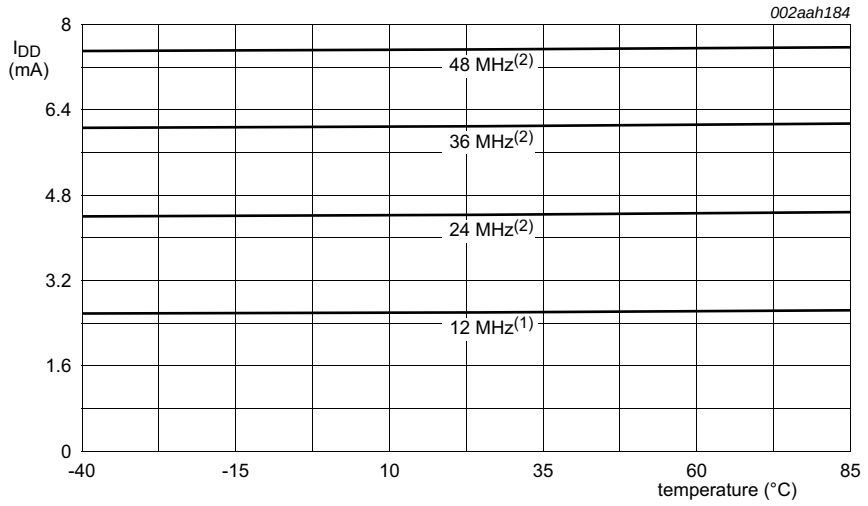
[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_2 and PIO0_3 and except the 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).

9.1 Power consumption

Power measurements in Active and Sleep modes were performed under the following conditions (see *LPC11Axx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIO DIR registers to drive the outputs LOW.



Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 11. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals disabled)

10. Dynamic characteristics

10.1 Power supply fluctuations

If the input voltage ($V_{DD(3V3)}$) to the internal regulator fluctuates, the LPC11Axx is held in reset during a brown-out condition as long as the UVLO circuit is operating. The settling times of the BOD and POR circuits, which constitute the UVLO, determine the minimum time the supply level must remain in the shallow or deep brown-out condition to ensure that the internal reset is asserted properly.

See also Section 7.23.1, Section 12.7, and Section 12.8.

Table 8. UVLO circuits settling characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_s	settling time	power droop:	5	-	-	µs
		from active level to shallow brown-out level ($0.9\ V \le V_{DD(3V3)} \le 2.4\ V$)				
		from active level to deep brown-out level ($0 < V_{DD(3V3)} < 0.9\ V$)	12	-	-	µs

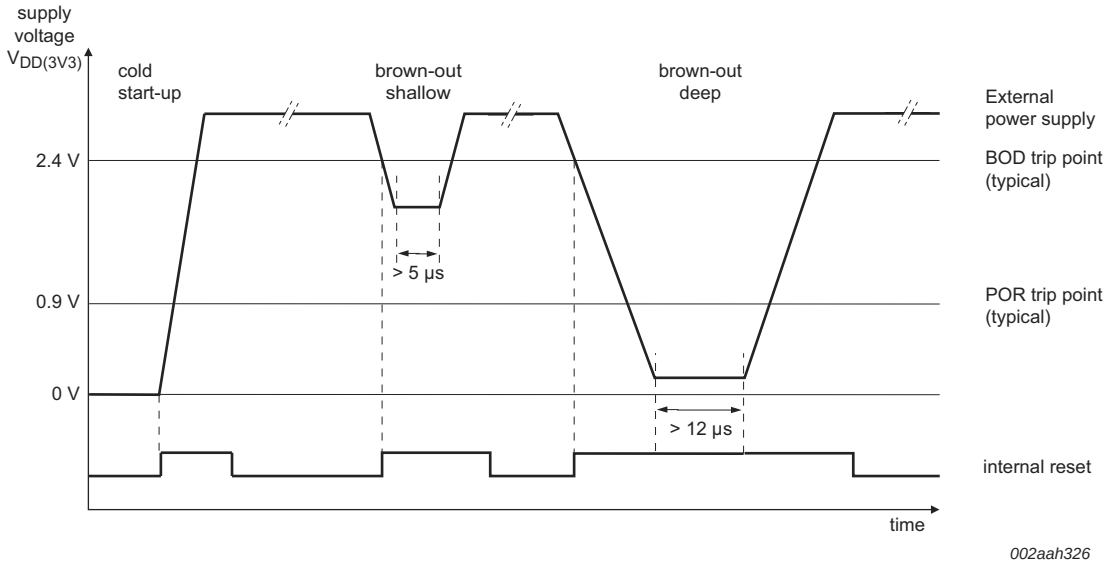


Fig 20. UVLO timing

10.2 Flash/EEPROM memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[2][1]	10000	100000	-	cycles

Table 9. Flash characteristics
T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered	[2]	10	20	-	years
		unpowered	[2]	20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors	[2]	95	100	105	ms
t_{prog}	programming time		[2][3]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[3] Programming times are given for writing 256 bytes to the flash. T_{amb} < +85 °C. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC11Axx user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

Table 10. EEPROM characteristics
T_{amb} = −55 °C to +125 °C; $V_{DD(3V3)}$ = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	100000	1000000	-	cycles
t_{ret}	retention time	powered	[1]	100	200	-	years
		unpowered	[1]	150	300	-	years
t_{prog}	programming time	64 bytes	[2]	-	1.1	-	ms

[1] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[2] T_{amb} < +85 °C.

10.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTALIN pin must be ≤ 1.95 V (see Table 6). For connecting the oscillator to the XTALIN/XTALOUT pins also see Section 12.3.

Table 11. Dynamic characteristic: external clock (XTALIN or CLKIN pin)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ± 40%.

[3] See the LPC11Axx user manual.

10.5 I/O pins

Table 14. Dynamic characteristic: digital I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; load capacitor = 30 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output					
		SSO = 1	[2][3]	2.5	-	5.0	ns
		SSO = 6	[2][3]	2.5	-	4.5	ns
		SSO = 16	[2][4]	3.0	-	5.0	ns
t_f	fall time	pin configured as output	[2][3]				
		SSO = 1		2.0	-	4.5	ns
		SSO = 6	[2][3]	2.0	-	4.5	ns
		SSO = 16	[2][4]	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin. Simulated results.

[2] SSO indicates maximum number of simultaneously switching digital output pins. The pins are optimized for half of the maximum SSO.

[3] Set SLEW bit in the IOCON register to 1.

[4] Set SLEW bit in the IOCON register to 0.

10.6 I²C-bus

Remark: All I²C modes (Standard-mode, Fast-mode, Fast-mode Plus) can be configured for the true open-drain pins PIO0_2 and PIO0_3. If the limited-performance I²C-bus pins are used (I²C-bus functions on standard I/O pins), only Standard-mode with internal pull-up enabled or Fast-mode with external pull-up resistor are supported.

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs

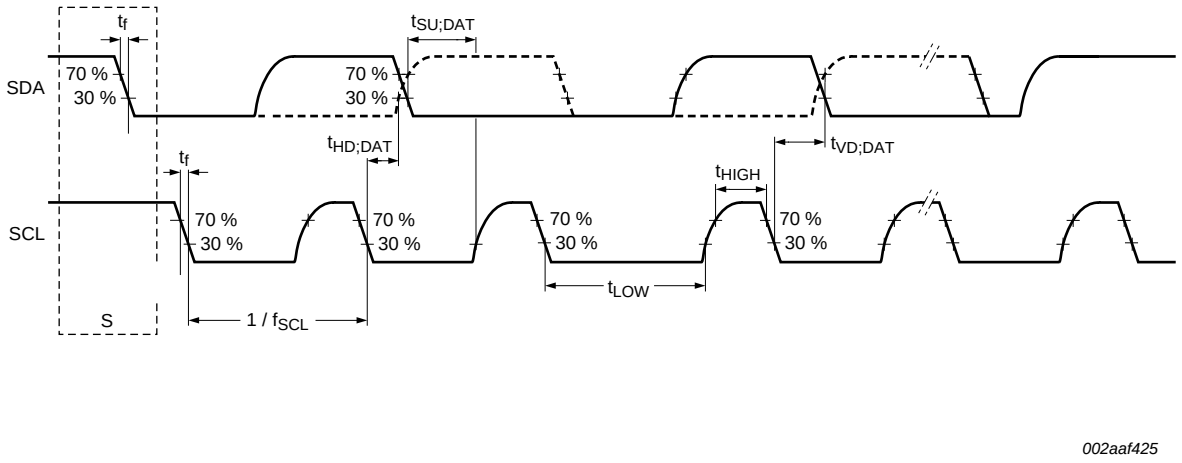


Fig 23. I^2C-bus pins clock timing

10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode
2.6 V <= $V_{DD(3V3)}$ = $V_{DD(IO)}$ <= 3.6 V.

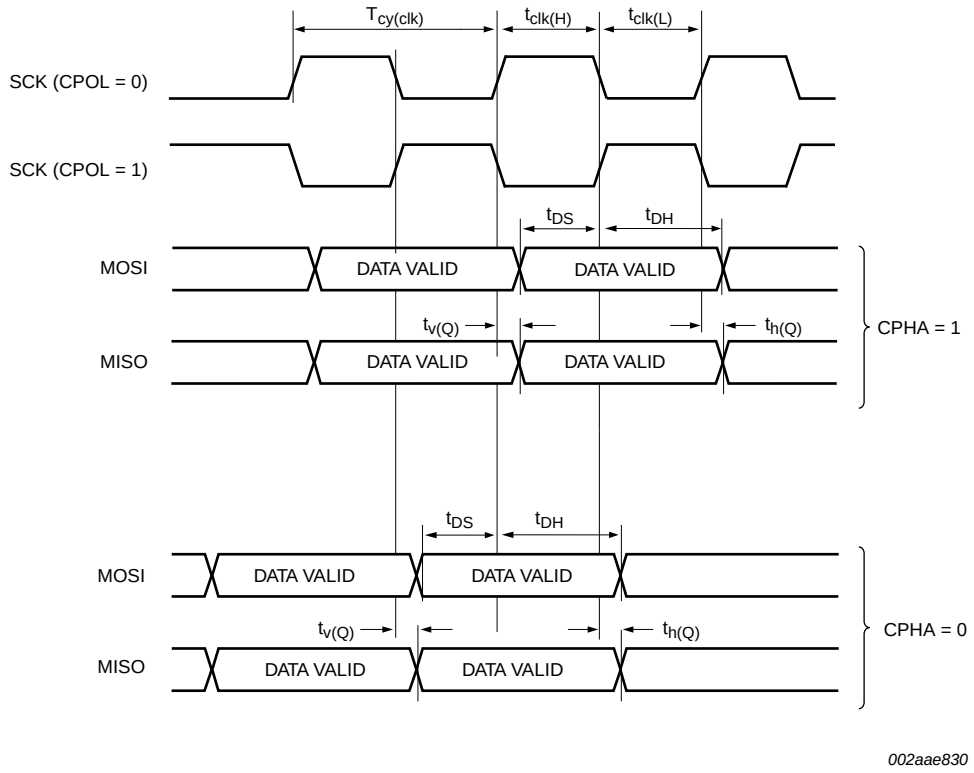
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1][1]	40			ns
t_{DS}	data set-up time	in SPI mode	[1][2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[1][2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[1][2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[1][2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)}$ = 3.3 V.



Pin names SCK, MISO, and MOSI refer to pins for both SSP peripherals, SSP0 and SSP1.

Fig 25. SSP slave timing in SPI mode

11. Characteristics of analog peripherals

Table 17. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage					
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC11Axx user manual*.

Table 25. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation ($V_{DD(3V3)}$ = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

Table 26. Comparator voltage ladder reference static characteristics
$V_{DD(3V3)}$ = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal $V_{DD(3V3)}$ supply					
		decimal code = 00	[2]	-	0	0	%
		decimal code = 08		-	0	±0.4	%
		decimal code = 16		-	–0.2	±0.2	%
		decimal code = 24		-	–0.2	±0.2	%
		decimal code = 30		-	–0.1	±0.1	%
		decimal code = 31		-	–0.1	±0.1	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		-	0	0	%
		decimal code = 08		-	–0.1	±0.5	%
		decimal code = 16		-	–0.2	±0.4	%
		decimal code = 24		-	–0.2	±0.3	%
		decimal code = 30		-	–0.2	±0.2	%
		decimal code = 31		-	–0.1	±0.1	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 µV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC11Axx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

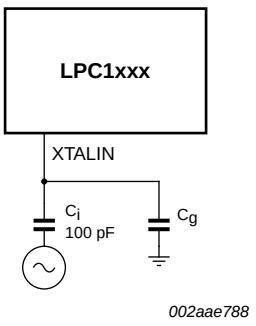


Fig 29. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 30 and in Table 27 and Table 28. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

R_S). Capacitance C_P in Figure 30 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 27).

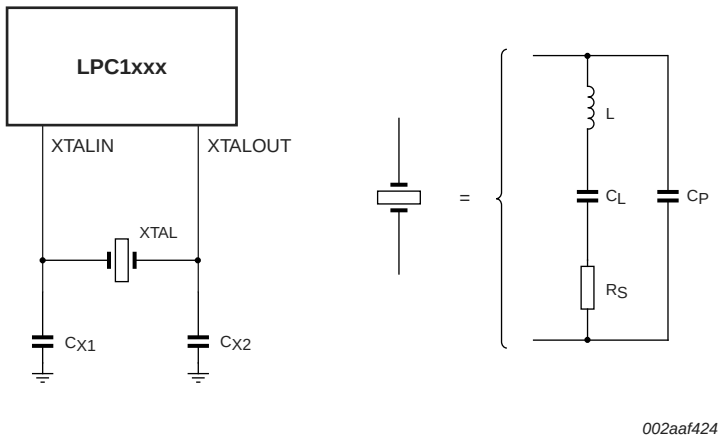


Fig 30. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

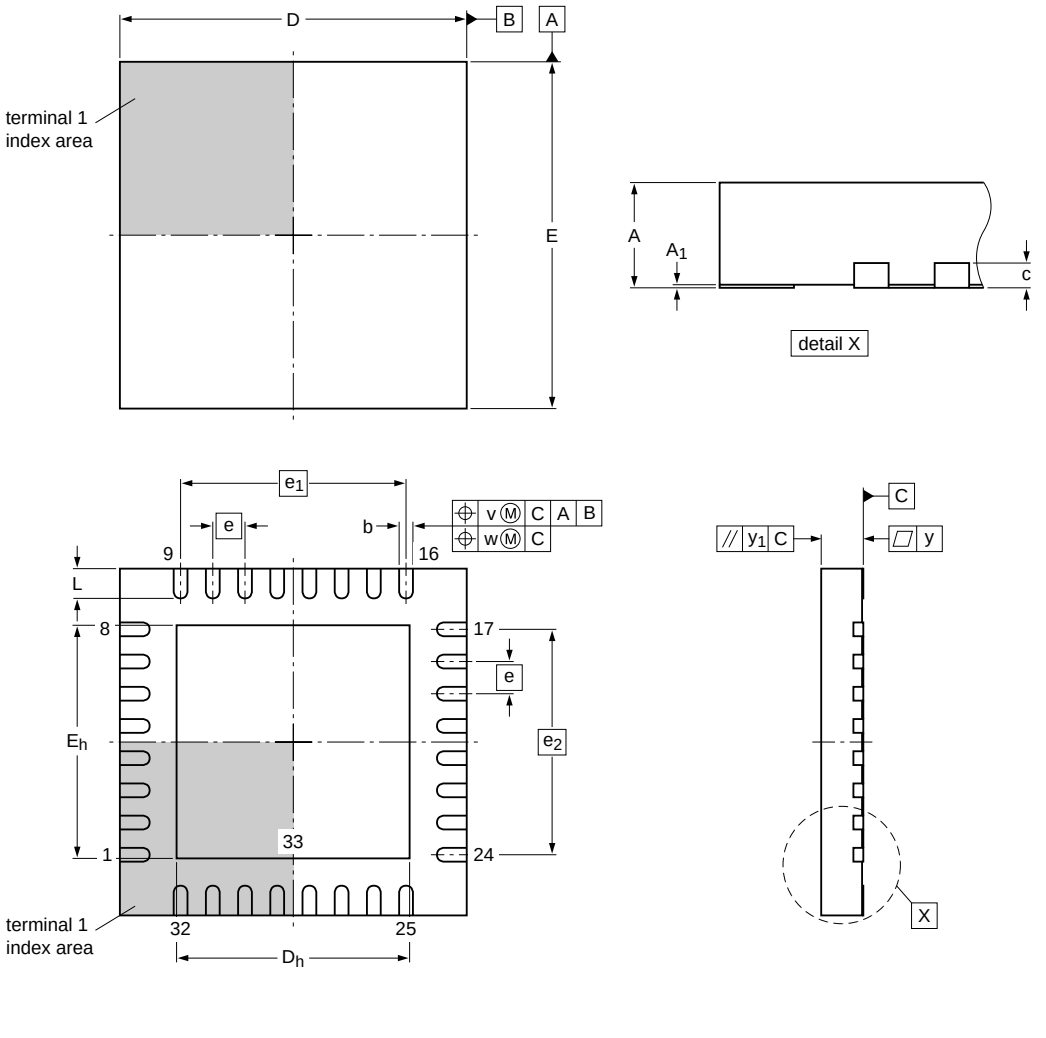
Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 28. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

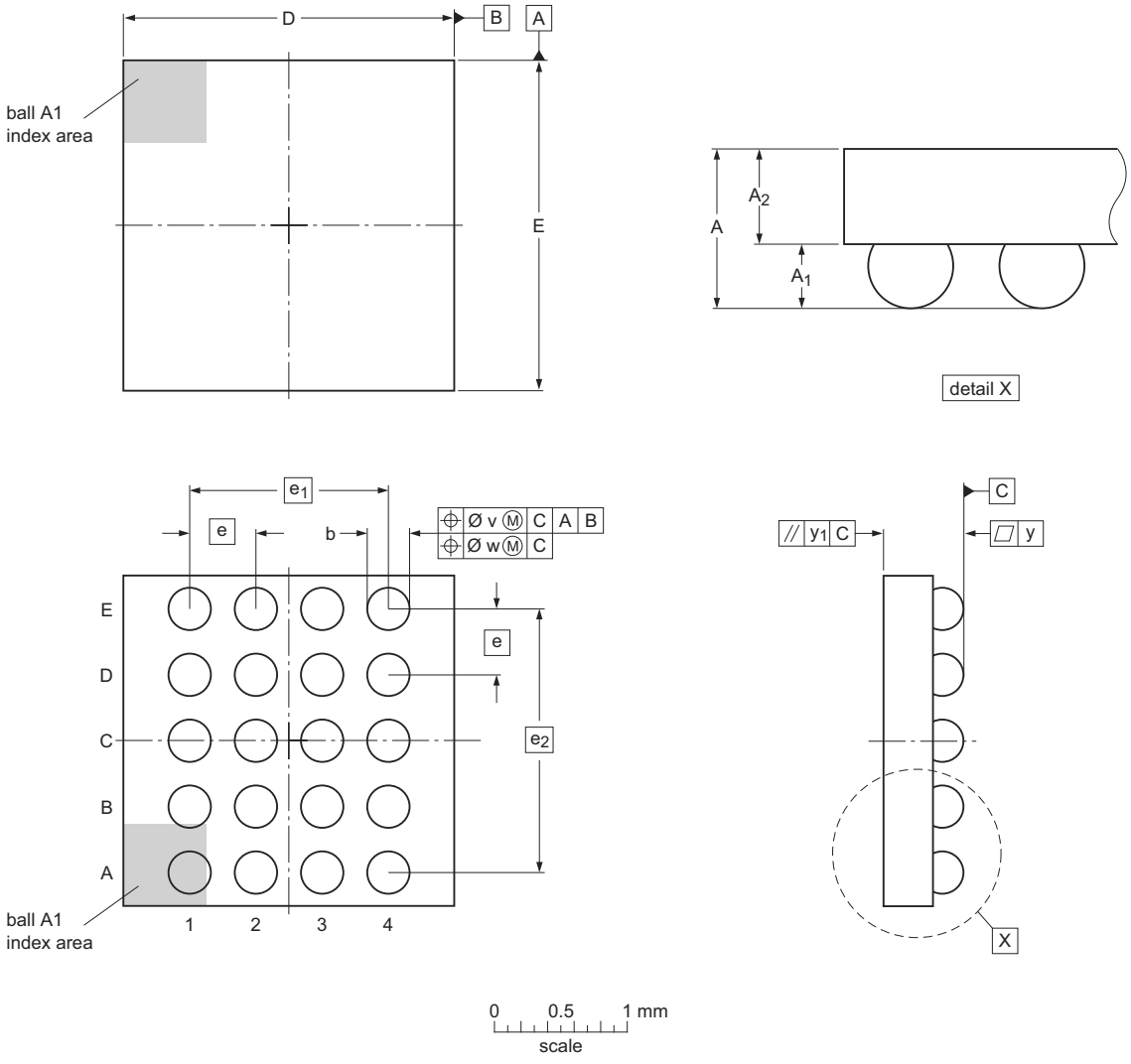
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		- - -				~~09-03-17~~ 09-03-23

Fig 35. Package outline HVQFN33 (7x7)

WLCSP20: wafer level chip-size package; 20 bumps; 2.5 x 2.5 x 0.6 mm **LPC11AxxUK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.65	0.27	0.38	0.35	2.60	2.60						
mm	nom	0.60	0.24	0.36	0.32	2.55	2.55	0.5	1.5	2.0	0.15	0.05	0.05
	min	0.55	0.21	0.34	0.29	2.50	2.50						

wlcsp20_lpc11axxuk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC11AxxUK						12-03-26

Fig 37. Package outline (WLCSP20)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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