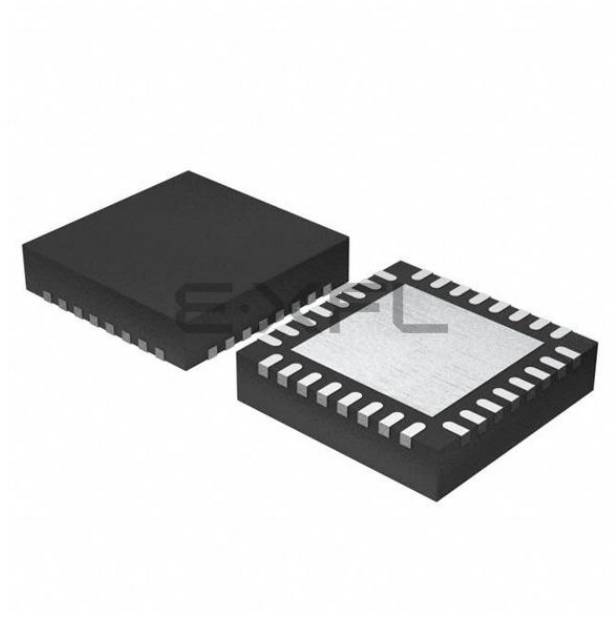

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a13fhi33-201

- Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC with flexible conversion triggering.
  - Highly flexible analog comparator with a programmable voltage reference.
  - Integrated temperature sensor.
  - Internal voltage reference.
  - UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports one reduced power mode: The ARM Sleep mode.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

- Single 3.3 V power supply (2.6 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP48 package, HVQFN33 (7 × 7) and HVQFN33 (5 × 5) packages, and in a very small WLCSP20 package.

3. Applications

- Power management
- Industrial control
- Remote monitoring
- Point-of-sale
- Test and measurement equipment
- Network appliances and services
- Factory automation
- Gaming equipment
- Motion control
- Medical instrumentation
- Fire and security
- Sensors
- Precision instrumentation
- HVAC and building control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11A02UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A04UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A11FHN33/001	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A13FHI33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11A14FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FBD48/101	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11A14FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
SSP1 controller						
MISO1	I/O	PIO0_14	10 ns[2]	30	20	-
		PIO0_26	no	1	1	-
		PIO1_8	no	26	-	-
MOSI1	I/O	PIO0_27	10 ns[2]	43	28	-
		PIO0_31	no	24	-	-
		PIO0_30	no	40	-	-
		PIO1_6	no	11	-	-
SCK1	I/O	PIO0_8	10 ns[2]	34	23	-
		PIO1_5	no	20	-	-
		PIO0_29	no	13	-	-
SSEL1	I/O	PIO0_25	no	17	12	-
		PIO1_4	no	19	-	-
		PIO0_28	no	2	-	-
USART						
RXD	I	PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO1_4	no	19	-	-
		PIO1_8	no	26	-	-
TXD	O	PIO0_13	no	47	32	D1
		PIO0_15	no	41	27	E4
		PIO0_26	no	1	1	-
		PIO1_5	no	20	-	-
SCLK	I/O	PIO0_11	10 ns[2]	39	26	D2
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
$\overline{\text{CTS}}$	I	PIO0_9	10 ns[2]	35	24	D4
		PIO0_21	no	23	16	-
		PIO1_7	no	25	-	-
$\overline{\text{RTS}}$	O	PIO0_10	no	38	25	D3
		PIO0_23	no	45	30	-
		PIO1_6	no	11	-	-
$\overline{\text{DCD}}$	I	PIO1_9	no	12	-	-
		PIO1_0	no	31	-	-
$\overline{\text{DSR}}$	I	PIO0_29	no	13	-	-
		PIO1_2	no	37	-	-
$\overline{\text{DTR}}$	O	PIO0_28	no	2	-	-
		PIO1_1	no	36	-	-

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$\overline{RI}$	I	PIO0_30	no	40	-	-
		PIO0_31	no	24	-	-
		PIO1_3	no	48	-	-
16-bit counter/timer CT16B0						
CT16B0_CAP0	I	PIO0_2	50 ns[2]	15	10	A1
		PIO0_18	no	10	8	-
		PIO0_30	no	40	-	-
CT16B0_CAP1	I	PIO0_16	10 ns[2]	18	13	A2
		PIO1_4	no	19	-	-
CT16B0_CAP2	I	PIO0_17	10 ns[2]	21	14	A3
		PIO1_5	no	20	-	-
CT16B0_MAT0	O	PIO0_7	no	33	22	C4
		PIO0_17	no	21	14	A3
		PIO1_6	no	11	-	-
CT16B0_MAT1	O	PIO0_4	no	28	18	A4
		PIO0_9	no	35	24	D4
		PIO1_0	no	31	-	-
CT16B0_MAT2	O	PIO0_5	no	29	19	B3
		PIO0_10	no	38	25	D3
		PIO1_7	no	25	-	-
16-bit counter/timer CT16B1						
CT16B1_CAP0	I	PIO0_3	50 ns[2]	16	11	B1
		PIO0_24	no	9	7	-
		PIO1_3	no	48	-	-
CT16B1_CAP1	I	PIO0_18	no	10	8	-
		PIO0_26	no	1	1	-
		PIO0_31	no	24	-	-
CT16B1_CAP2	I	PIO0_27	10 ns[2]	43	28	-
		PIO1_7	no	25	-	-
CT16B1_MAT0	O	PIO0_19	no	14	9	-
		PIO0_25	no	17	12	-
		PIO1_1	no	36	-	-
CT16B1_MAT1	O	PIO0_14	no	30	20	B4
		PIO1_2	no	37	-	-
		PIO1_8	no	26	-	-
CT16B1_MAT2	O	PIO0_20	no	22	15	-
		PIO1_2	no	37	-	-
		PIO1_9	no	12	-	-

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
TDI/PIO0_6/AD0/ CT32B0_MAT3/MISO0	32	21	C3	[9]	I	I; PU	**TDI —** Test Data In for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_6 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD0 —** A/D converter input 0.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I/O	-	**MISO0 —** Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
TMS/PIO0_7/AD1/ CT32B1_CAP0/ CT16B0_MAT0	33	22	C4	[9]	I	I; PU	**TMS —** Test Mode Select for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_7 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD1 —** A/D converter input 1.
					I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0 —** Match output 2 for 16-bit timer 0.
TDO/PIO0_8/AD2/ CT32B1_MAT0/SCK1	34	23	C2	[9]	O	I; PU	**TDO —** Test Data Out for JTAG interface.
					I/O	-	**PIO0_8 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD2 —** A/D converter input 2.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I/O	-	**SCK1 —** Serial clock for SSP1. Input glitch filter (10 ns) capable.
$\overline{\text{TRST}}$/PIO0_9/AD3/ CT32B1_MAT1/ CT16B0_MAT1/$\overline{\text{CTS}}$	35	24	D4	[9]	I	I; PU	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_9 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD3 —** A/D converter, input 3.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/$\overline{\text{RTS}}$/ ACMP_O/ CT32B0_CAP0/SCLK	45	30	-	[3]	I/O	I; PU	**PIO0_23 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					I/O	-	**SCLK —** Serial clock for USART.
PIO0_24/SCL/CLKIN/ CT16B1_CAP0	9	7	-	[3]	I/O	I; PU	**PIO0_24 —** General purpose digital input/output pin.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN —** External clock input.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/ CT16B1_MAT0	17	12	-	[3]	I/O	I; PU	**PIO0_25 —** General purpose digital input/output pin.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10].
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/ CT16B1_CAP1/ CT32B0_CAP2	1	1	-	[3]	I/O	I; PU	**PIO0_26 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/ CT32B1_MAT1/ CT16B1_CAP2	43	28	-	[9]	I/O	I; PU	**PIO0_27 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I1 —** Analog comparator input 1.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/$\overline{\text{DTR}}$/SSEL1/ CT32B0_CAP0	2	-	-	[3]	I/O	I; PU	**PIO0_28 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO0_29/$\overline{\text{DSR}}$/SCK1/ CT32B0_CAP1	13	-	-	[3]	I/O	I; PU	**PIO0_29 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
$V_{SS(IO)}$	5	33	E3	[14]	-	-	Ground.
$V_{DD(3V3)}$	44	29	E2	[12] [13]	-	-	3.3 V supply voltage to the analog blocks, internal regulator, and internal clock generator circuits. Also used as the ADC reference voltage.
V_{SS}	42	33	E3	[14]	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up resistor (weak PMOS device) enabled; IA = inactive, no pull-up/down enabled.

[2] See Figure 32 for the reset configuration.

[3] 5 V tolerant pin providing standard digital I/O functions with configurable modes and configurable hysteresis (Figure 31).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] For the SWD function, a pull-up resistor is recommended for the SWCLK pin (WLCSP20 parts only).

[6] For the SWD function, a pull-up resistor is recommended for the SWDIO pin (WLCSP20 parts only).

[7] Not a 5 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, the digital section of the pin is disabled (Figure 31).

[8] If this pin is configured for its VDDCMP function, it cannot be used for SWCLK when the part is on the board. The bypass filter of the power supply filters out the SWCLK clock input signal.

[9] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, digital section of the pin is disabled, and the pin is not 5 V tolerant (Figure 31).

[10] I^2C-bus pins are standard digital I/O pins and have limited performance and electrical characteristics compared to the full I^2C-bus specification. Pins can be configured with an on-chip pull-up resistor (pMOS device) and with open-drain mode. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.

[11] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating. See Section 12.3 if an external clock is connected to the XTALIN pin.

[12] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the power supply pins are filtered for noise with respect to their corresponding grounds V_{SS} and $V_{SS(IO)}$ (LQFP48 package). Using separate filtered supplies reduces the noise to the analog blocks (see also Section 12.1).

[13] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[14] Thermal pad (HVQFN33 pin package). Connect to ground.

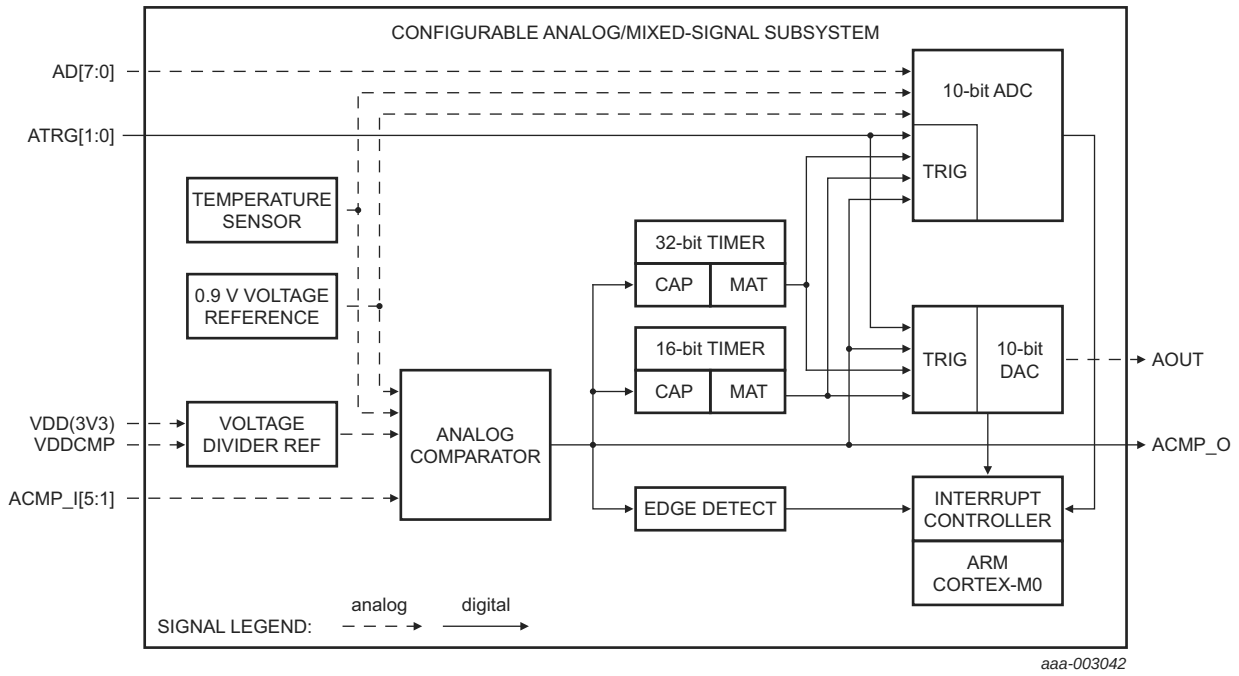


Fig 6. Configurable analog/mixed signal subsystem

7.14 10-bit ADC

The LPC11Axx contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

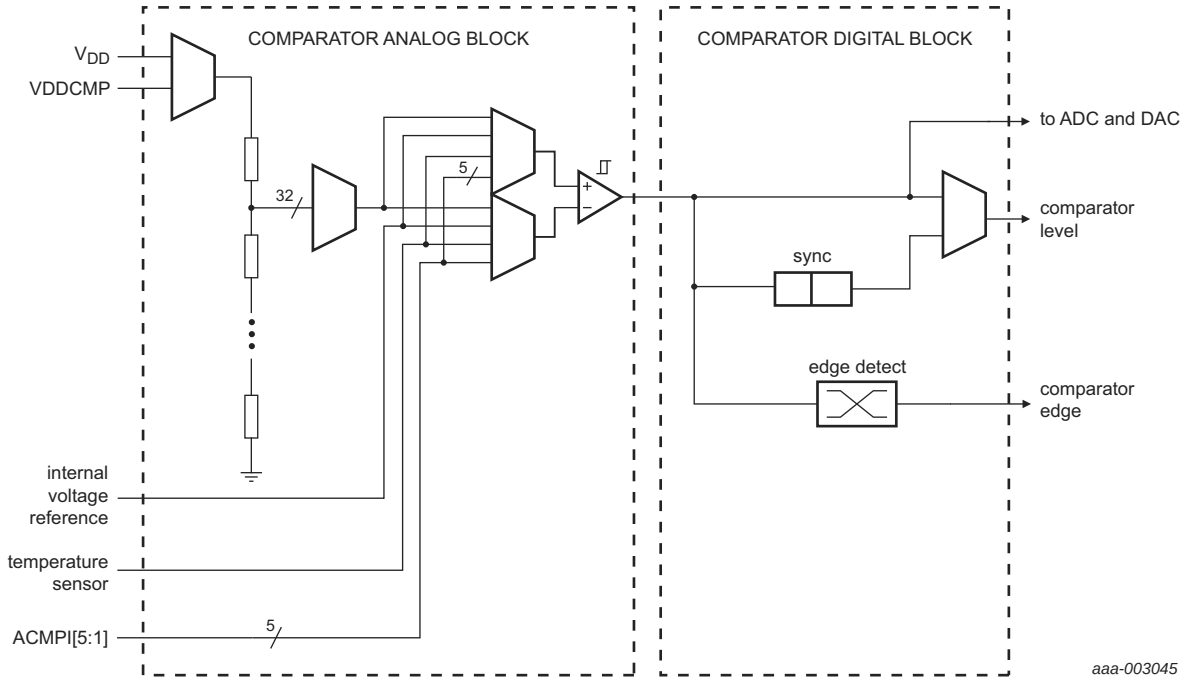


Fig 9. Comparator block diagram

7.18.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Five selectable external voltages; fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap and temperature sensor selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel. See Table 24 to Table 26.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- Comparator output is internally connected to the ADC and DAC and can be used to trigger a conversion.
- The comparator output is also connected internally to capture channel 3 on each of the 32-bit and 16-bit counter/timers.

7.19 General purpose external event counter/timers

The LPC11Axx includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt. Up to three capture channels are pinned out. One channel is internally connected to the comparator output ACMP_O.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.20 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.21 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

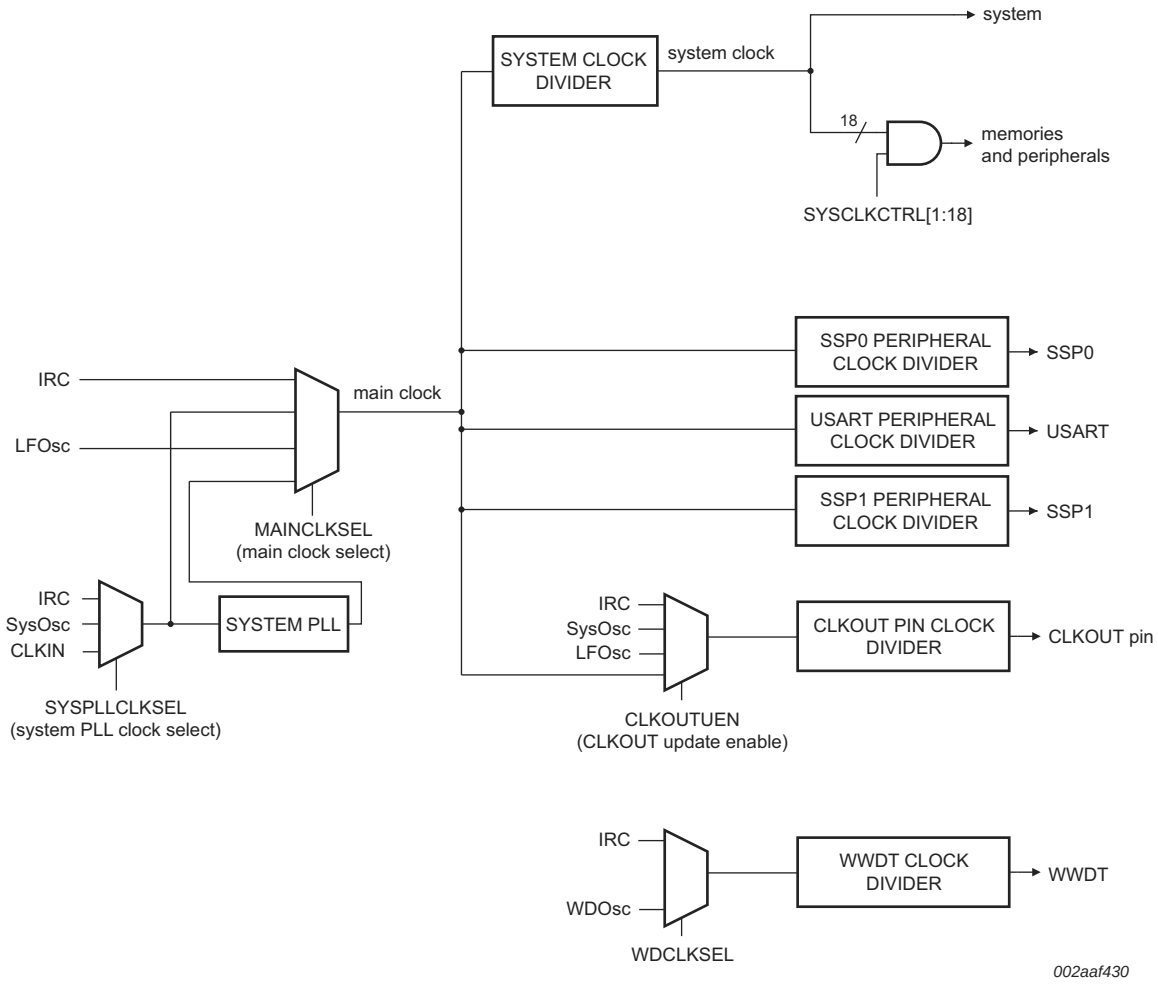


Fig 10. LPC11Axx clock generation block diagram

7.22.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC11Axx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.22.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	−0.5	4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	−0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	−0.5	+5.5	V
		on pins PIO0_2 and PIO0_3	[5]	−0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	−0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[11]	−6.5	+6.5	kV
V_{trig}	trigger voltage	for LVTSCR based ESD pin protection; 1 ns to 10 ns rise time	[12]	8.2	-	V
		> 10 ns rise time		> 8.5	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_2 and PIO0_3 and except the 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] Applies to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

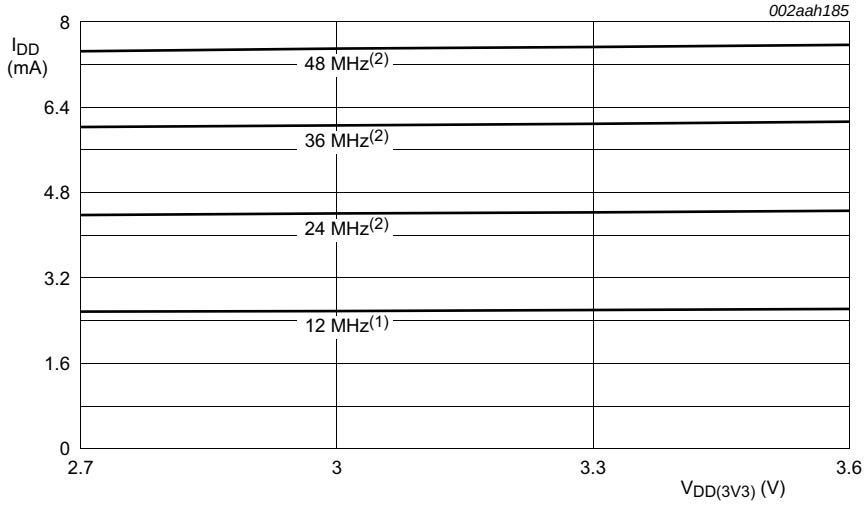
[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Not characterized.

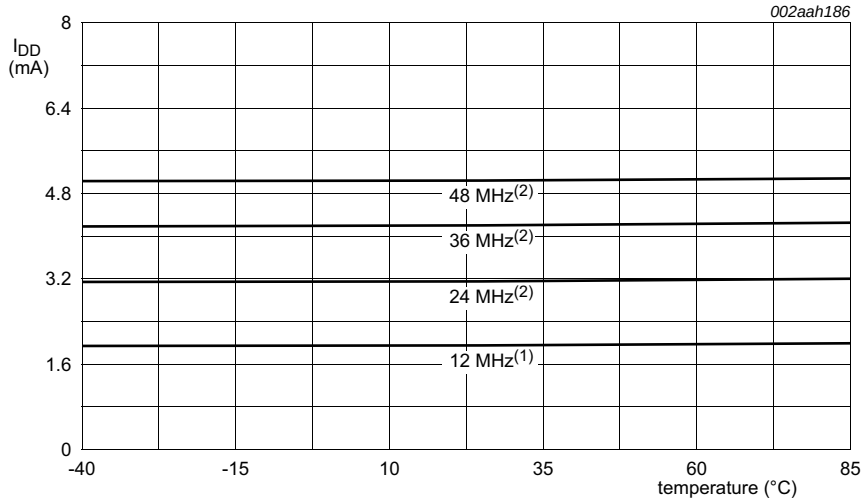


Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 12. Active mode: Typical supply current I_{DD} versus core voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals disabled)



Conditions: $V_{DD(3V3)}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register and PDRUNCFG register; all peripheral clocks disabled; BOD disabled; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

(2) SysOsc and system PLL enabled; IRC disabled.

Fig 13. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies (all peripherals disabled)

9.2 Peripheral power consumption

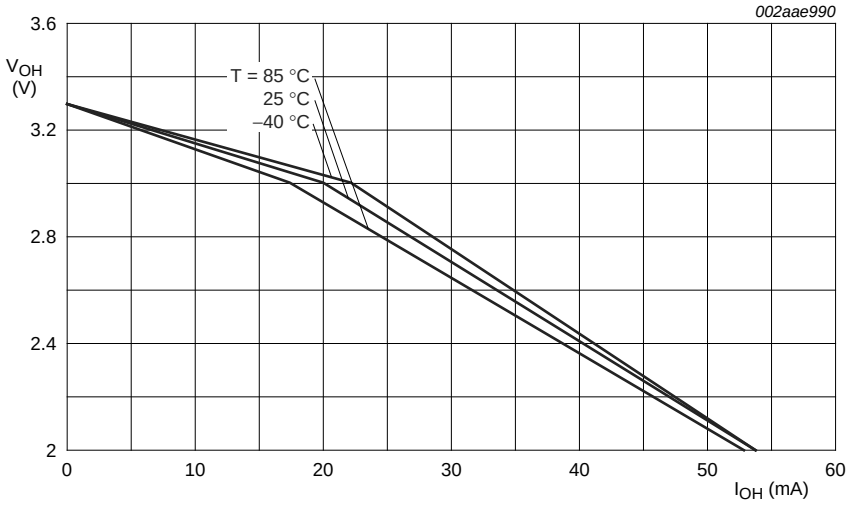
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

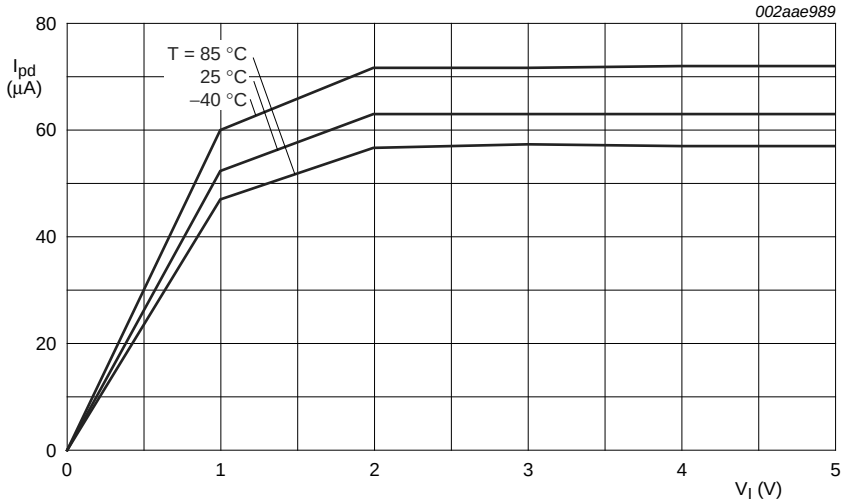
[1] IRC on; PLL off.

9.3 Electrical pin characteristics



Conditions: $V_{DD(IO)}$ = 3.3 V; on pin PIO0_21.

Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 19. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Power supply fluctuations

If the input voltage ($V_{DD(3V3)}$) to the internal regulator fluctuates, the LPC11Axx is held in reset during a brown-out condition as long as the UVLO circuit is operating. The settling times of the BOD and POR circuits, which constitute the UVLO, determine the minimum time the supply level must remain in the shallow or deep brown-out condition to ensure that the internal reset is asserted properly.

See also Section 7.23.1, Section 12.7, and Section 12.8.

Table 8. UVLO circuits settling characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_s	settling time	power droop:	5	-	-	µs
		from active level to shallow brown-out level ($0.9\ V \le V_{DD(3V3)} \le 2.4\ V$)				
		from active level to deep brown-out level ($0 < V_{DD(3V3)} < 0.9\ V$)	12	-	-	µs

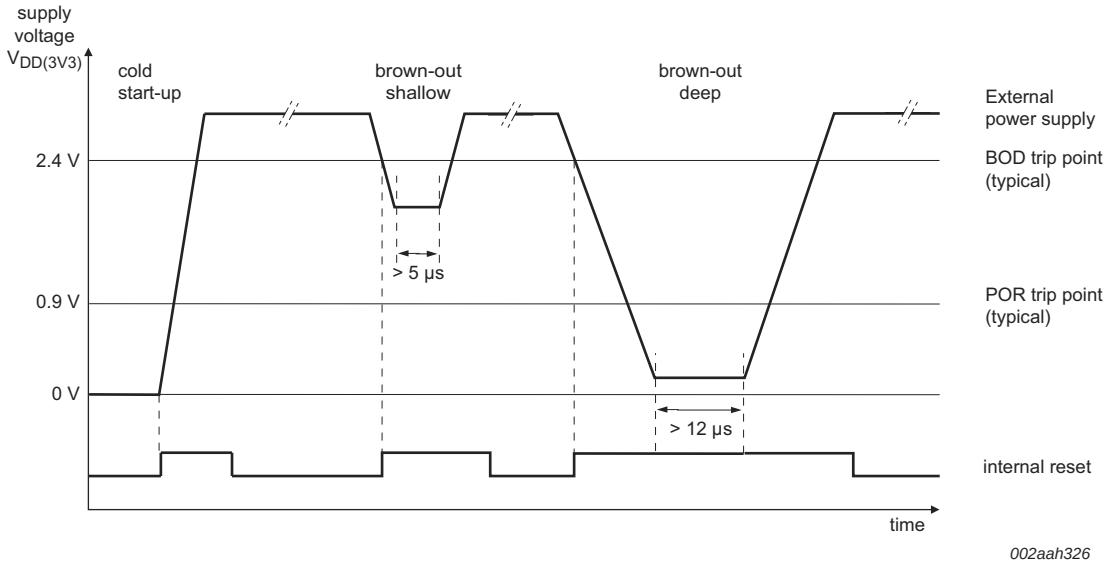


Fig 20. UVLO timing

10.2 Flash/EEPROM memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[2][1]	10000	100000	-	cycles

Table 9. Flash characteristics
T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered	[2]	10	20	-	years
		unpowered	[2]	20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors	[2]	95	100	105	ms
t_{prog}	programming time		[2][3]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[3] Programming times are given for writing 256 bytes to the flash. T_{amb} < +85 °C. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC11Axx user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

Table 10. EEPROM characteristics
T_{amb} = −55 °C to +125 °C; $V_{DD(3V3)}$ = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	100000	1000000	-	cycles
t_{ret}	retention time	powered	[1]	100	200	-	years
		unpowered	[1]	150	300	-	years
t_{prog}	programming time	64 bytes	[2]	-	1.1	-	ms

[1] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[2] T_{amb} < +85 °C.

10.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTALIN pin must be ≤ 1.95 V (see Table 6). For connecting the oscillator to the XTALIN/XTALOUT pins also see Section 12.3.

Table 11. Dynamic characteristic: external clock (XTALIN or CLKIN pin)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

12.6 Reset pad configuration

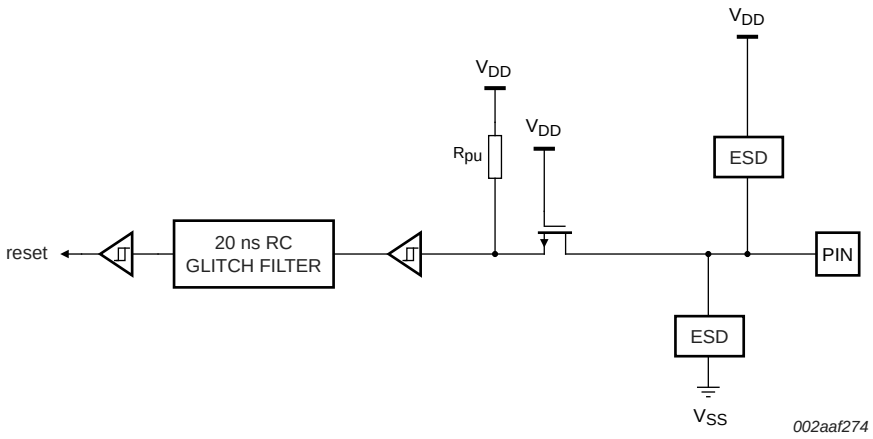


Fig 32. Reset pad configuration

12.7 UVLO protection and reset timer circuit

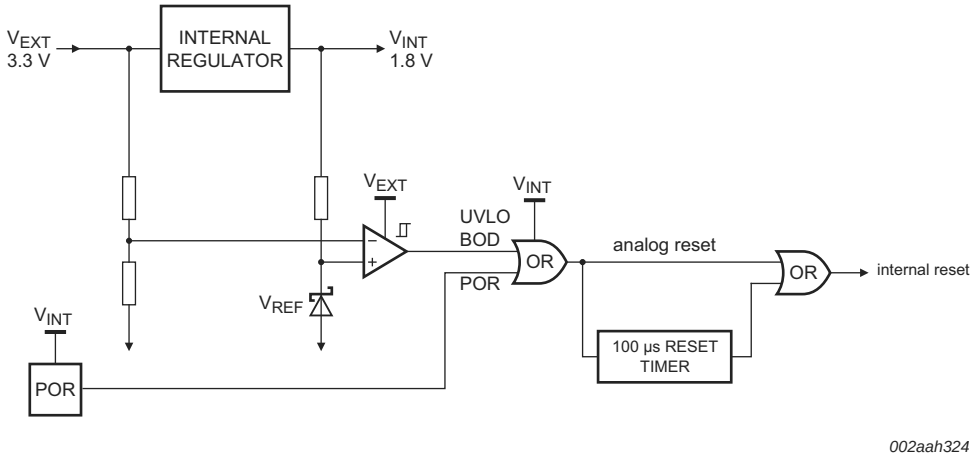


Fig 33. Functional diagram of the UVLO protection and reset timer circuit

12.8 Guidelines for selecting a power supply filter for UVLO protection

For the UVLO circuits to hold the part in reset during shallow and deep brown-out conditions, you must filter the power supply line to allow for the BOD and POR circuits to settle when short voltage drops occur (see Section 10.1 “Power supply fluctuations”).

Select the capacitance of the decoupling/bypass capacitor according to the following guidelines:

$C >> I_{DD} \times t_s/\Delta V_{DD(3V3)}$ with

- $\Delta V_{DD(3V3)} \approx 100$ mV for the voltage drop below the BOD or POR trip points.
- $I_{DD} \approx 3$ mA with the IRC running and PLL/SysOsc off (see Figure 12).

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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