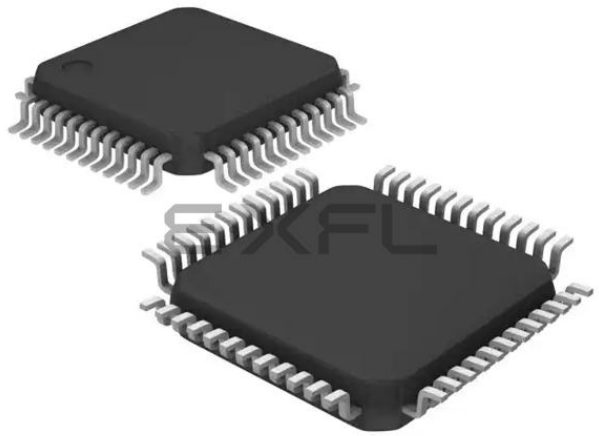

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a14fbd48-301

6. Pinning information

6.1 Pinning

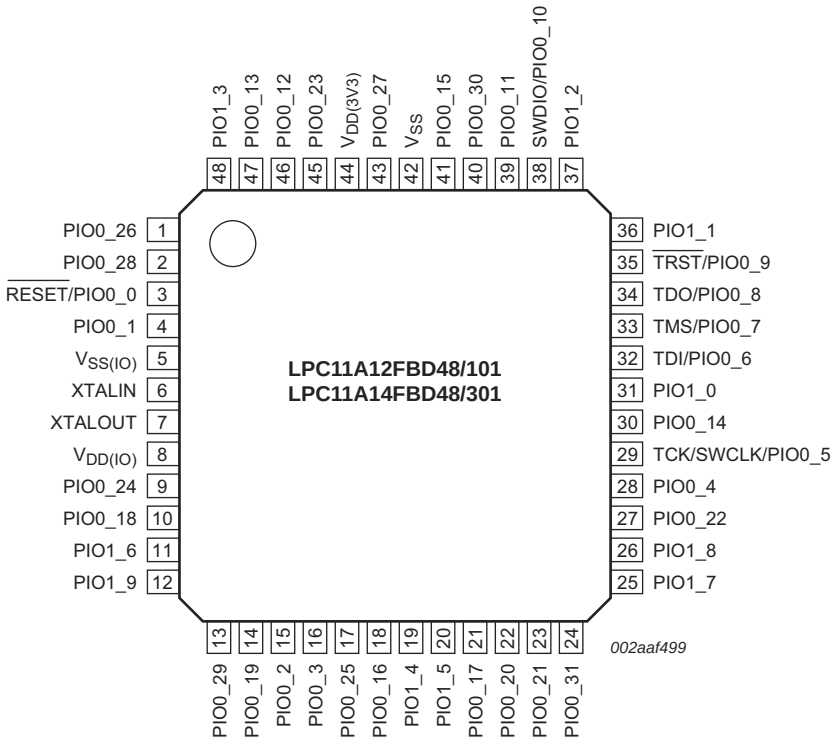


Fig 2. Pin configuration LQFP48 package

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
SSP1 controller						
MISO1	I/O	PIO0_14	10 ns[2]	30	20	-
		PIO0_26	no	1	1	-
		PIO1_8	no	26	-	-
MOSI1	I/O	PIO0_27	10 ns[2]	43	28	-
		PIO0_31	no	24	-	-
		PIO0_30	no	40	-	-
		PIO1_6	no	11	-	-
SCK1	I/O	PIO0_8	10 ns[2]	34	23	-
		PIO1_5	no	20	-	-
		PIO0_29	no	13	-	-
SSEL1	I/O	PIO0_25	no	17	12	-
		PIO1_4	no	19	-	-
		PIO0_28	no	2	-	-
USART						
RXD	I	PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO1_4	no	19	-	-
		PIO1_8	no	26	-	-
TXD	O	PIO0_13	no	47	32	D1
		PIO0_15	no	41	27	E4
		PIO0_26	no	1	1	-
		PIO1_5	no	20	-	-
SCLK	I/O	PIO0_11	10 ns[2]	39	26	D2
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
$\overline{\text{CTS}}$	I	PIO0_9	10 ns[2]	35	24	D4
		PIO0_21	no	23	16	-
		PIO1_7	no	25	-	-
$\overline{\text{RTS}}$	O	PIO0_10	no	38	25	D3
		PIO0_23	no	45	30	-
		PIO1_6	no	11	-	-
$\overline{\text{DCD}}$	I	PIO1_9	no	12	-	-
		PIO1_0	no	31	-	-
$\overline{\text{DSR}}$	I	PIO0_29	no	13	-	-
		PIO1_2	no	37	-	-
$\overline{\text{DTR}}$	O	PIO0_28	no	2	-	-
		PIO1_1	no	36	-	-

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
32-bit counter/timer CT32B0						
CT32B0_CAP0	I	PIO0_11	10 ns[2]	39	26	D2
		PIO0_23	no	45	30	-
		PIO0_28	no	2	-	-
CT32B0_CAP1	I	PIO0_14	10 ns[2]	30	20	B4
		PIO0_29	no	13	-	-
CT32B0_CAP2	I	PIO0_15	10 ns[2]	41	27	E4
		PIO0_26	no	1	1	-
CT32B0_MAT0	O	PIO0_12	no	46	31	E1
		PIO0_30	no	40	-	-
CT32B0_MAT1	O	PIO0_13	no	47	32	D1
		PIO1_4	no	19	-	-
CT32B0_MAT2	O	PIO0_1	no	4	3	B2
		PIO1_5	no	20	-	-
CT32B0_MAT3	O	PIO0_6	no	32	21	C3
		PIO1_6	no	11	-	-
32-bit counter/timer CT32B1						
CT32B1_CAP0	I	PIO0_7	10 ns[2]	33	22	C4
		PIO0_20	no	22	15	-
		PIO1_4	no	19	-	-
CT32B1_CAP1	I	PIO0_21	no	23	16	-
		PIO1_5	no	20	-	-
CT32B1_CAP2	I	PIO0_22	10 ns[2]	27	17	-
		PIO1_6	no	11	-	-
CT32B1_MAT0	O	PIO0_8	no	34	23	C2
		PIO0_31	no	24	-	-
		PIO1_8	no	26	-	-
CT32B1_MAT1	O	PIO0_9	no	35	24	D4
		PIO0_27	no	43	28	-
		PIO1_7	no	25	-	-
CT32B1_MAT2	O	PIO0_10	no	38	25	D3
		PIO0_22	no	27	17	-
		PIO1_9	no	12	-	-
CT32B1_MAT3	O	PIO0_11	no	39	26	D2
		PIO1_1	no	36	-	-
		PIO1_0	no	31	-	-
Supply and ground pins						
$V_{DD(IO)}$	Supply	-	-	8	6	E2

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$V_{DD(3V3)}$	Supply	-	-	44	29	E2
V_{SS}	Ground	-	-	42	33	E3
$V_{SS(IO)}$	Ground	-	-	5	33	E3

[1] Always on.

[2] Programmable on/off. By default, the glitch filter is disabled.

Table 4 shows all pins in order of their port number. The default function after reset is listed first. All port pins PIO0_0 to PIO1_9 have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_2 and PIO0_3.

Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON registers for each of the port pins.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
$\overline{\text{RESET}}$/PIO0_0	3	2	C1	[2]	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with fixed 20 ns glitch filter: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0.
					I/O	-	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/RXD/CLKOUT/ CT32B0_MAT2/SSEL0/ CLKIN	4	3	B2	[3]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	-	**RXD —** Receiver data input for USART.
					O	-	**CLKOUT —** Clock output.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I/O	-	**SSEL0 —** Slave Select for SSP0.
					I	-	**CLKIN —** External clock input.
PIO0_2/SCL/ACMP_O/ TCK/SWCLK/ CT16B0_CAP0	15	10	A1	[4][5]	I/O	I; IA	**PIO0_2 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**TCK/SWCLK —** Serial Wire Debug Clock (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWCLK function by the boot loader after reset.
					I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0. Input glitch filter (50 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/$\overline{\text{RTS}}$/ ACMP_O/ CT32B0_CAP0/SCLK	45	30	-	[3]	I/O	I; PU	**PIO0_23 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					I/O	-	**SCLK —** Serial clock for USART.
PIO0_24/SCL/CLKIN/ CT16B1_CAP0	9	7	-	[3]	I/O	I; PU	**PIO0_24 —** General purpose digital input/output pin.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN —** External clock input.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/ CT16B1_MAT0	17	12	-	[3]	I/O	I; PU	**PIO0_25 —** General purpose digital input/output pin.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10].
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/ CT16B1_CAP1/ CT32B0_CAP2	1	1	-	[3]	I/O	I; PU	**PIO0_26 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/ CT32B1_MAT1/ CT16B1_CAP2	43	28	-	[9]	I/O	I; PU	**PIO0_27 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I1 —** Analog comparator input 1.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/$\overline{\text{DTR}}$/SSEL1/ CT32B0_CAP0	2	-	-	[3]	I/O	I; PU	**PIO0_28 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					I/O	-	**SSEL1 —** Slave Select for SSP1.
					I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO0_29/$\overline{\text{DSR}}$/SCK1/ CT32B0_CAP1	13	-	-	[3]	I/O	I; PU	**PIO0_29 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO1_5/TXD/SCK1/ CT32B0_MAT2/ CT32B1_CAP1/ CT16B0_CAP2	20	-	-	[3]	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					I	-	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_6/$\overline{\text{RTS}}$/MOSI1/ CT32B0_MAT3/ CT32B1_CAP2/ CT16B0_MAT0	11	-	-	[3]	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I	-	**CT32B1_CAP2 —** Capture input 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_7/$\overline{\text{CTS}}$/MOSI0/ CT32B1_MAT1/ CT16B0_MAT2/ CT16B1_CAP2	25	-	-	[3]	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1.
PIO1_8/RXD / MISO1/ CT32B1_MAT0/ CT16B1_MAT1	26	-	-	[3]	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
					I	-	**RXD —** Receiver data input for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_9/$\overline{\text{DCD}}$/R/ CT32B1_MAT2 / CT16B1_MAT2	12	-	-	[3]	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	-	**R —** Reserved.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					O	-	**CT16B1_MAT2 —** Match output 2 for 16-bit timer 1.
XTALIN	6	4	-	[11]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	5	-	[11]	-	-	Output from the oscillator amplifier.
$V_{DD(IO)}$	8	6	E2	[12] [13]	-	-	3.3 V input/output supply voltage.

- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.10 USART

The LPC11Axx contains one USART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 MBit/s.
- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Supports a full modem control handshake interface.
- Support for synchronous mode.

7.11 SSP serial I/O controller

The LPC11Axx contain two SSP controllers.

The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SPI mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC11Axx contains one I^2C-bus controller.

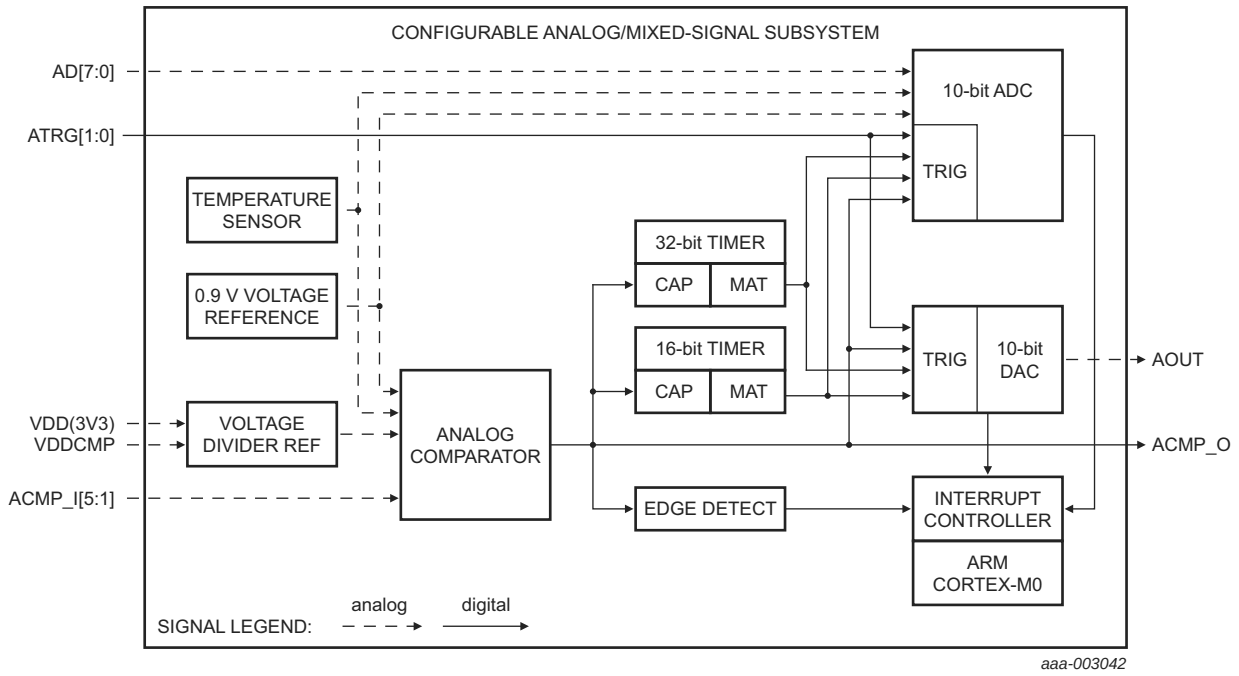


Fig 6. Configurable analog/mixed signal subsystem

7.14 10-bit ADC

The LPC11Axx contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

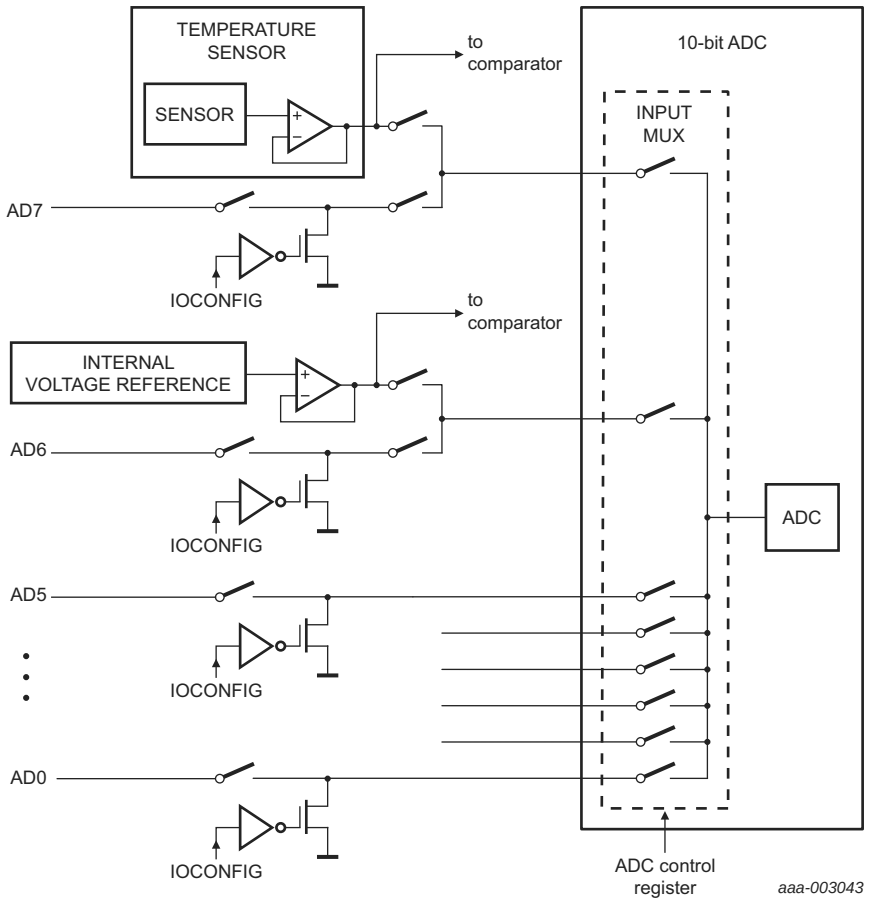


Fig 7. ADC block diagram

7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pins ATRG0 or ATRG1, timer match signal, or comparator output. (Input signals must be held for a minimum of three system clock periods). Also see Section 12.2.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.15 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V and varies typically only ±3 mV over the 0 °C to 85 °C temperature range (see Table 21 and Figure 27). The internal voltage reference can be used in the following applications:

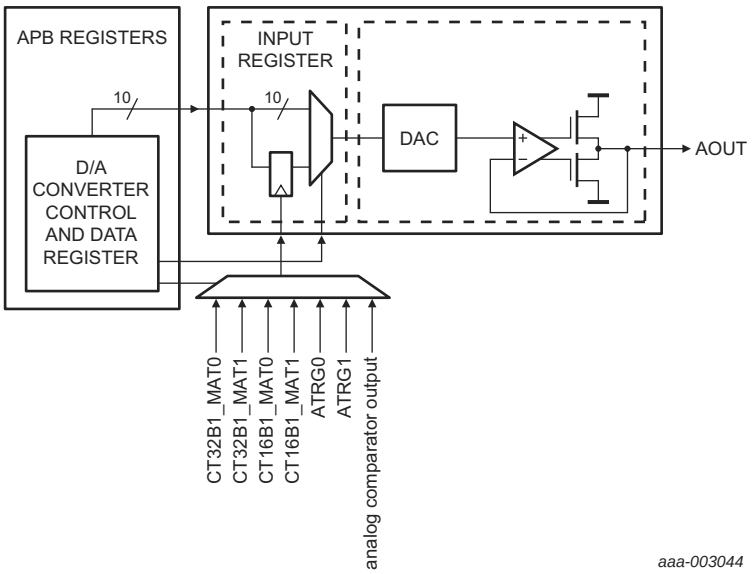


Fig 8. DAC block diagram

7.17.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
  - write operations to the DAC register.
  - a transition of pins ATRG0 or ATRG1. Input signals must be held for a minimum of three system clock periods.
  - a timer match signal.
  - a comparator output signal held for a minimum of two system clock periods.
- Holds output value during Sleep mode if the DAC is not powered down.

7.18 Analog comparator

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages. See Table 24.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

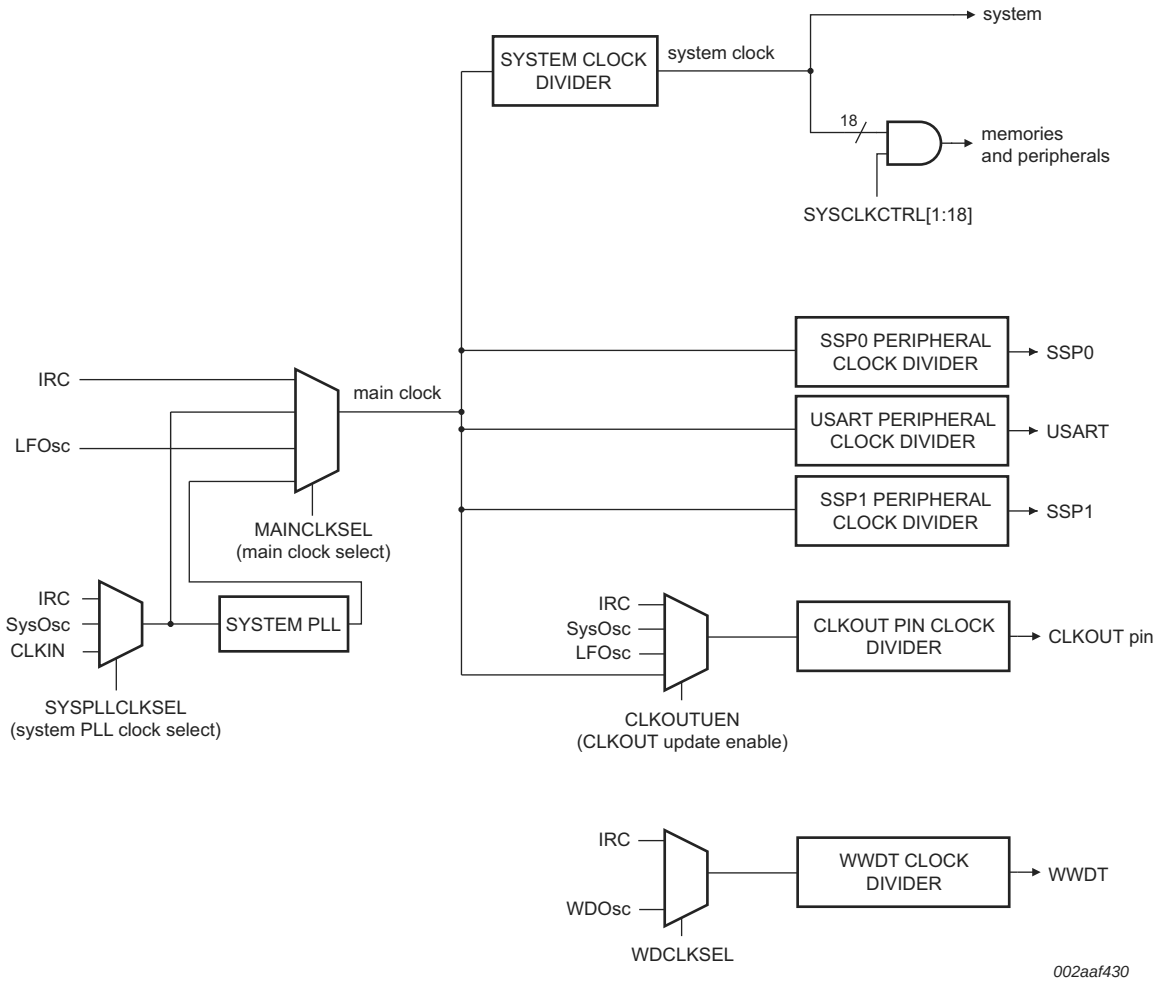


Fig 10. LPC11Axx clock generation block diagram

7.22.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC11Axx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.22.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

9.2 Peripheral power consumption

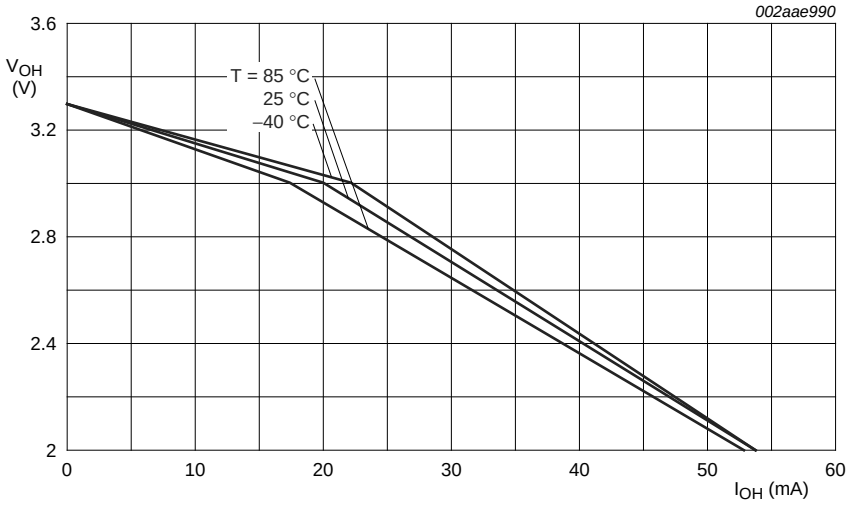
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

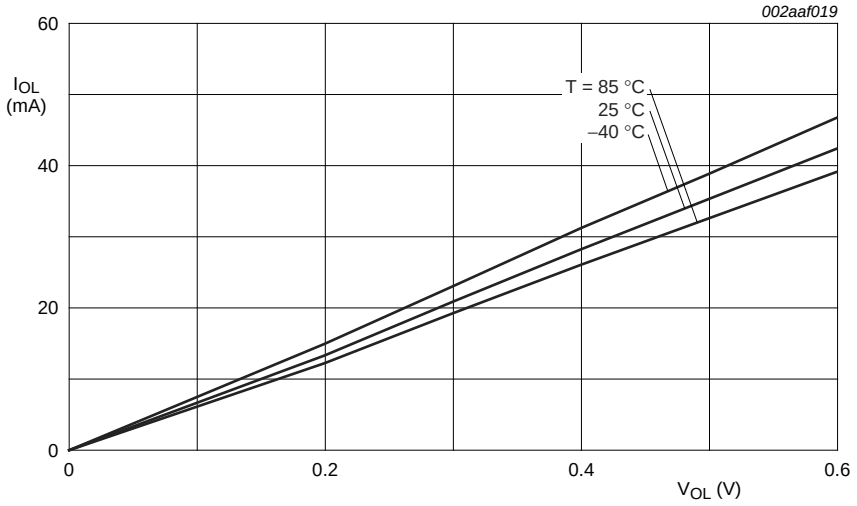
[1] IRC on; PLL off.

9.3 Electrical pin characteristics



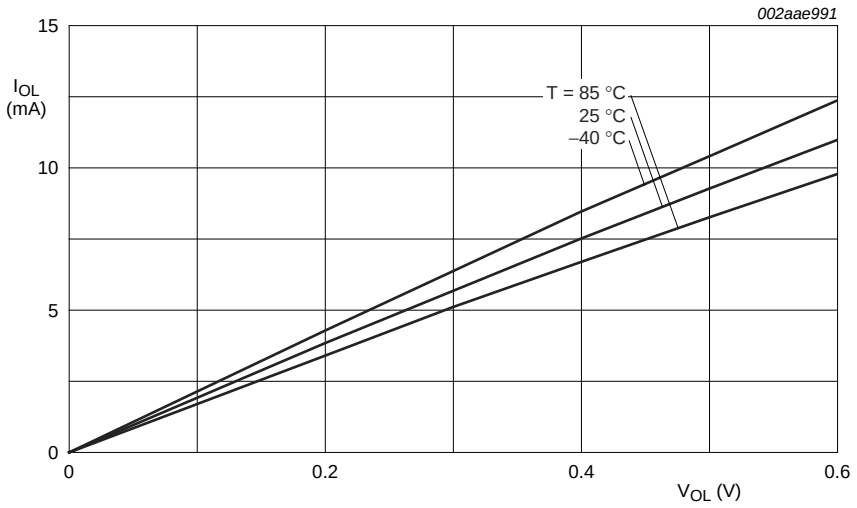
Conditions: $V_{DD(IO)}$ = 3.3 V; on pin PIO0_21.

Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



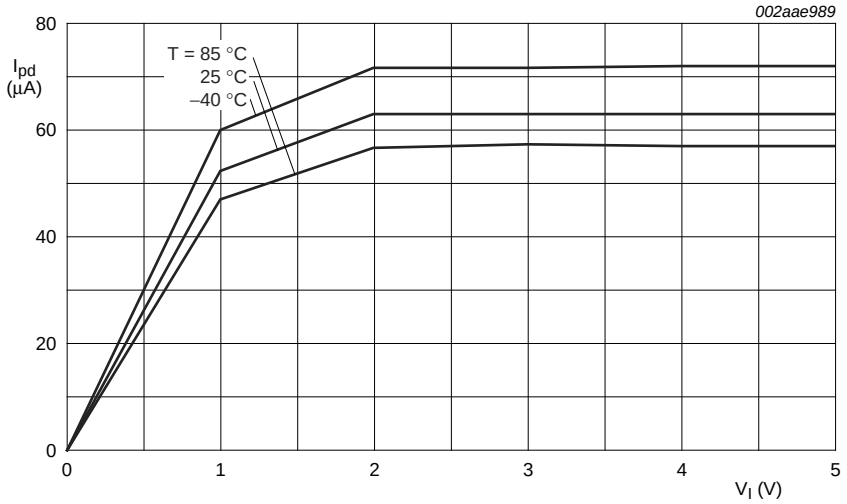
Conditions: $V_{DD(IO)}$ = 3.3 V; on pins PIO0_2 and PIO0_3.

Fig 15. High-current sink pins: Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins and PIO0_21.

Fig 16. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 19. Typical pull-down current I_{pd} versus input voltage V_I

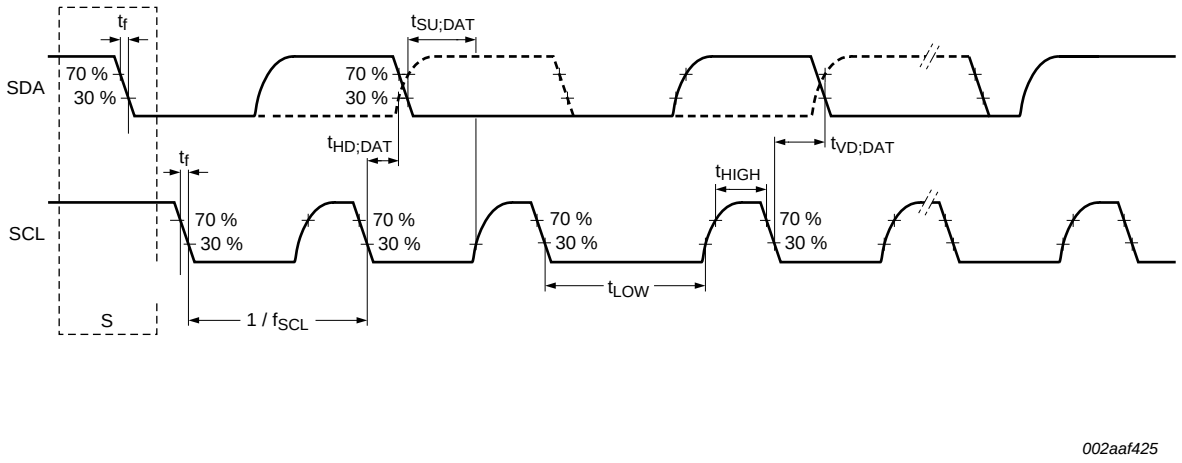


Fig 23. I^2C-bus pins clock timing

10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode
2.6 V <= $V_{DD(3V3)}$ = $V_{DD(IO)}$ <= 3.6 V.

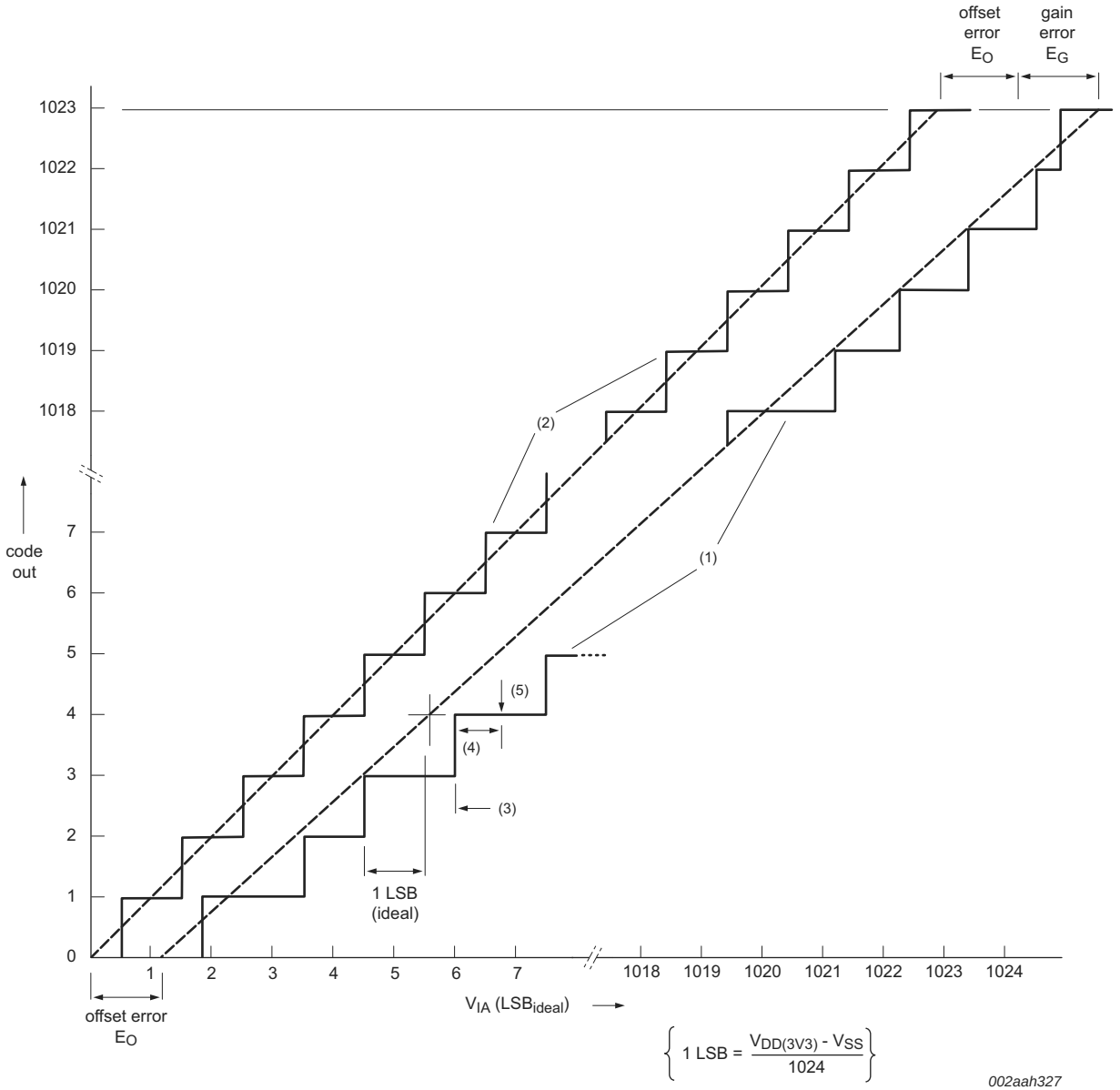
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1][1]	40			ns
t_{DS}	data set-up time	in SPI mode	[1][2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[1][2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[1][2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[1][2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)}$ = 3.3 V.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 26. ADC characteristics

12.6 Reset pad configuration

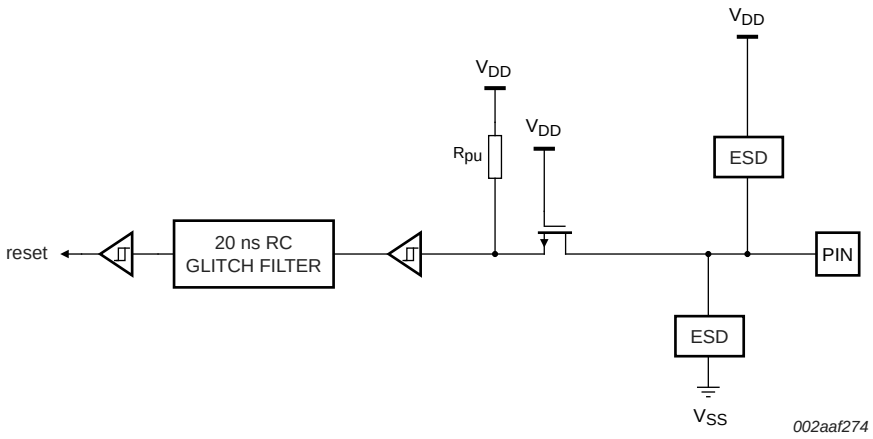


Fig 32. Reset pad configuration

12.7 UVLO protection and reset timer circuit

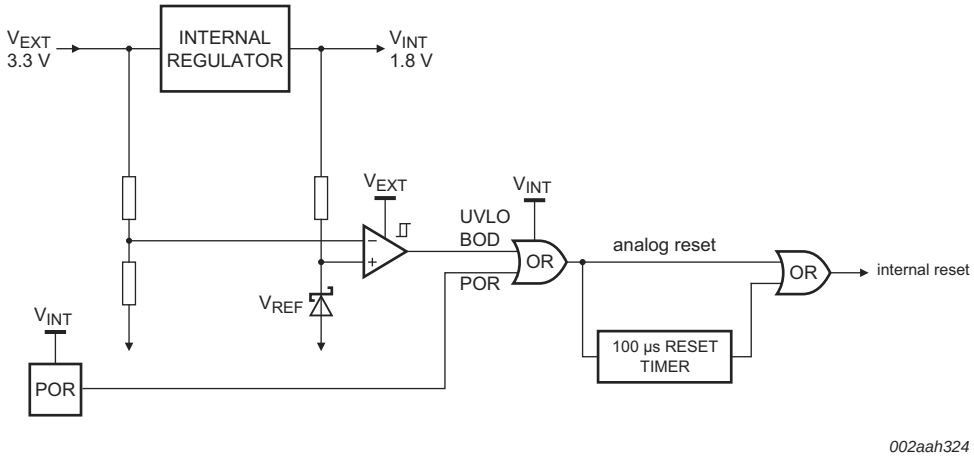


Fig 33. Functional diagram of the UVLO protection and reset timer circuit

12.8 Guidelines for selecting a power supply filter for UVLO protection

For the UVLO circuits to hold the part in reset during shallow and deep brown-out conditions, you must filter the power supply line to allow for the BOD and POR circuits to settle when short voltage drops occur (see Section 10.1 “Power supply fluctuations”).

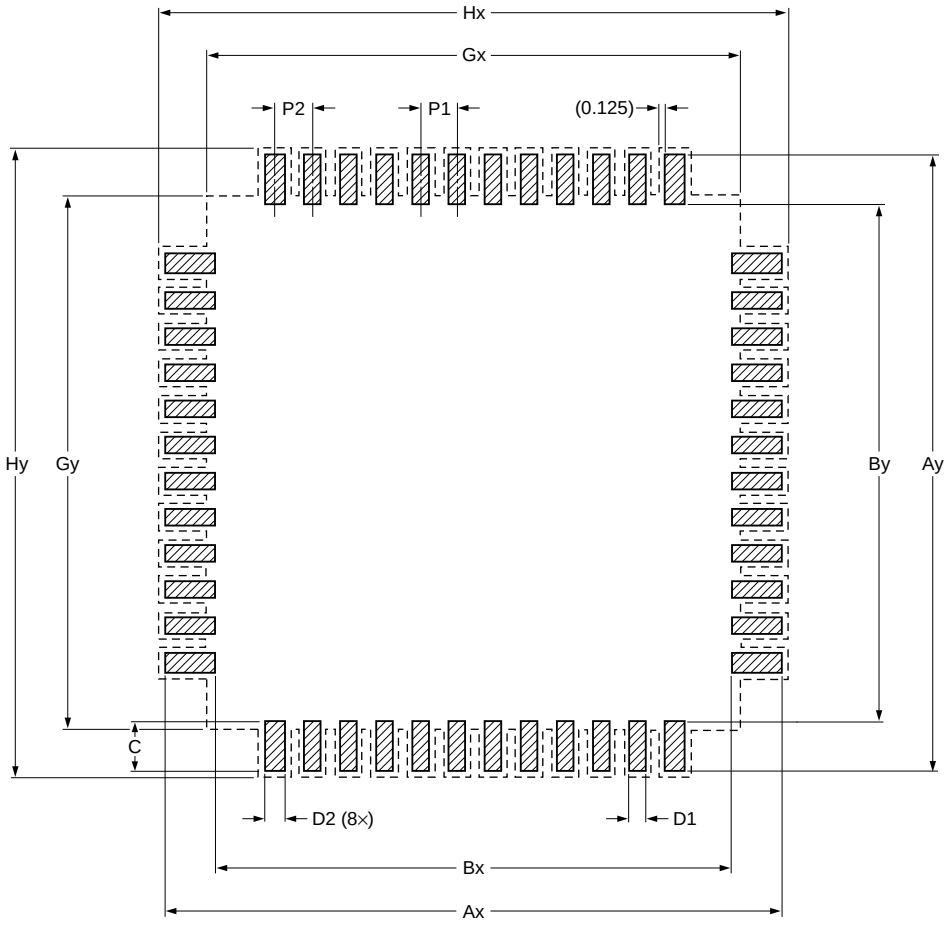
Select the capacitance of the decoupling/bypass capacitor according to the following guidelines:

$C >> I_{DD} \times t_s/\Delta V_{DD(3V3)}$ with

- $\Delta V_{DD(3V3)} \approx 100$ mV for the voltage drop below the BOD or POR trip points.
- $I_{DD} \approx 3$ mA with the IRC running and PLL/SysOsc off (see Figure 12).

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 38. Reflow soldering of the LQFP48 package

15. Abbreviations

Table 29. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detection
GPIO	General Purpose Input/Output
I2C	Inter Integrated Circuit
JEDEC	Joint Electron Devices Engineering Council
LVTSCR	Low-Voltage Triggered Silicon-Controlled Rectifier
NVM	Non-Volatile Memory
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
UVLO	Under-Voltage LockOut

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