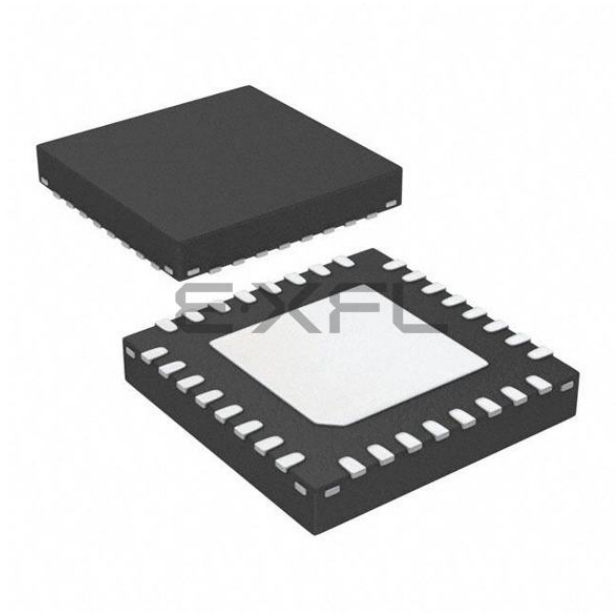

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.6V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11a14fhn33-301

- Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC with flexible conversion triggering.
  - Highly flexible analog comparator with a programmable voltage reference.
  - Integrated temperature sensor.
  - Internal voltage reference.
  - UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports one reduced power mode: The ARM Sleep mode.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_17/ ATRG1/ACMP_I4/ CT16B0_CAP2/ CT16B0_MAT0	21	14	A3	[9]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**ATRG1 —** Conversion trigger 1 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I4 —** Analog comparator input 4.
					I	-	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_18/R/SSEL0/ CT16B0_CAP0/ CT16B1_CAP1	10	8	-	[3]	I/O	I; PU	**PIO0_18 —** General purpose digital input/output pin.
					-	-	**R —** Reserved.
					I/O	-	**SSEL0 —** Slave Select for SSP0.
					I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
PIO0_19/CLKIN/ CLKOUT/ MOSI0/CT16B1_MAT0	14	9	-	[3]	I/O	I; PU	**PIO0_19 —** General purpose digital input/output pin.
					I	-	**CLKIN —** External clock input.
					O	-	**CLKOUT —** Clock output.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
					O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO0_20/R/SCK0/ CT32B1_CAP0/ CT16B1_MAT2	22	15	-	[3]	I/O	I; PU	**PIO0_20 —** General purpose digital input/output pin.
					-	-	**R —** Reserved.
					I/O	-	**SCK0 —** Serial clock for SSP0.
					I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT2 —** Match output 2 for 16-bit timer 1.
PIO0_21/$\overline{\text{CTS}}$/ ACMP_O/ CT32B1_CAP1/SCLK	23	16	-	[3]	I/O	I; PU	**PIO0_21 —** General purpose digital input/output pin. If configured as output, this pin is a high-current source output driver (20 mA).
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					I/O	-	**SCLK —** Serial clock for USART.
PIO0_22/MISO0/ ACMP_I5/ CT32B1_MAT2/ CT32B1_CAP2	27	17	-	[9]	I/O	I; PU	**PIO0_22 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO0 —** Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I5 —** Analog comparator input 5.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					I	-	**CT32B1_CAP2 —** Capture input 2 for 32-bit timer 1. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO1_5/TXD/SCK1/ CT32B0_MAT2/ CT32B1_CAP1/ CT16B0_CAP2	20	-	-	[3]	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					I	-	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_6/$\overline{\text{RTS}}$/MOSI1/ CT32B0_MAT3/ CT32B1_CAP2/ CT16B0_MAT0	11	-	-	[3]	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I	-	**CT32B1_CAP2 —** Capture input 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_7/$\overline{\text{CTS}}$/MOSI0/ CT32B1_MAT1/ CT16B0_MAT2/ CT16B1_CAP2	25	-	-	[3]	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1.
PIO1_8/RXD / MISO1/ CT32B1_MAT0/ CT16B1_MAT1	26	-	-	[3]	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
					I	-	**RXD —** Receiver data input for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_9/$\overline{\text{DCD}}$/R/ CT32B1_MAT2 / CT16B1_MAT2	12	-	-	[3]	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	-	**R —** Reserved.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					O	-	**CT16B1_MAT2 —** Match output 2 for 16-bit timer 1.
XTALIN	6	4	-	[11]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	5	-	[11]	-	-	Output from the oscillator amplifier.
$V_{DD(IO)}$	8	6	E2	[12] [13]	-	-	3.3 V input/output supply voltage.

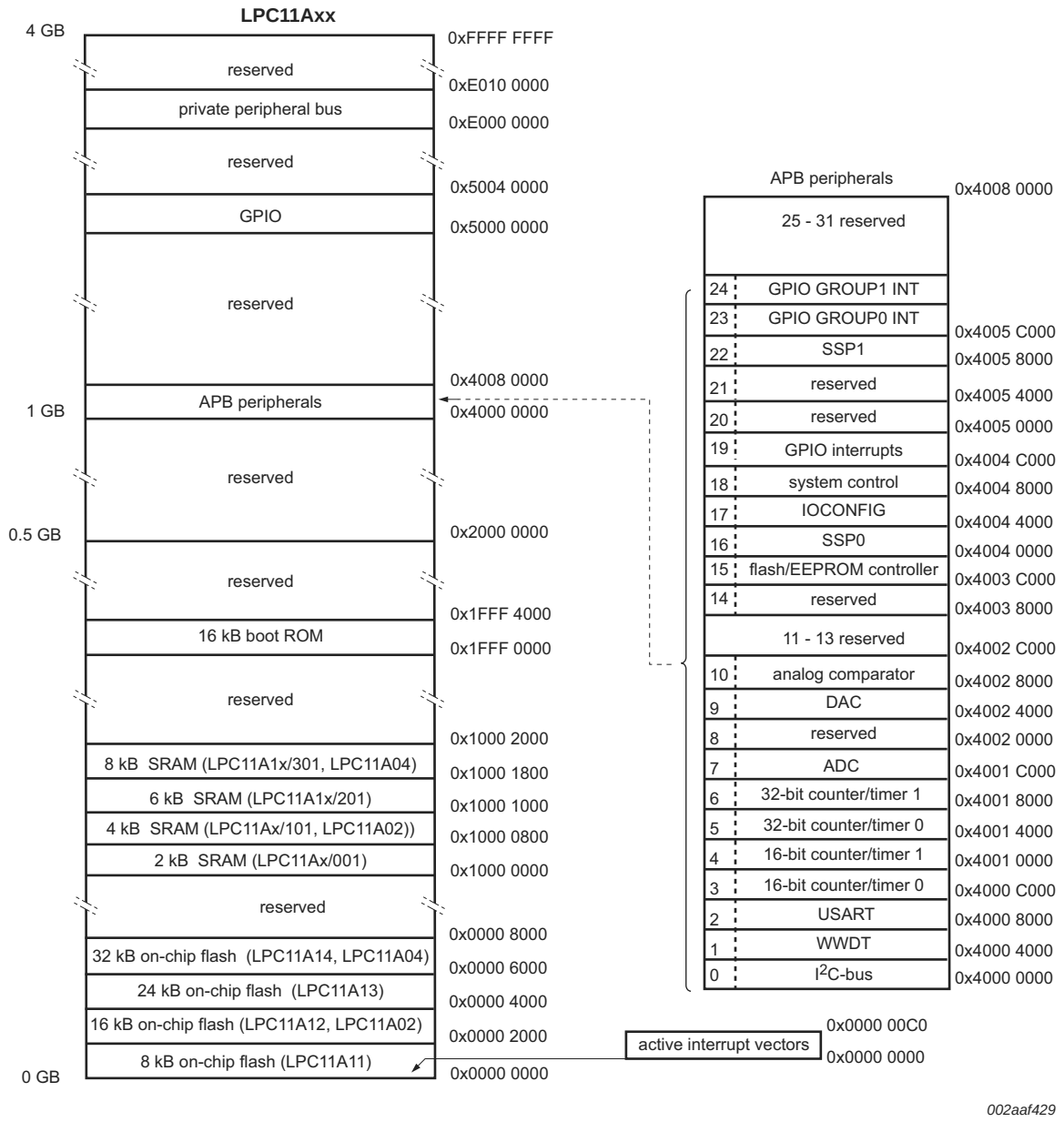


Fig 5. LPC11Axx memory map

7.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11Axx, the NVIC supports 32 vectored interrupts including up to 8 inputs to the start logic from the individual GPIO pins.

- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.10 USART

The LPC11Axx contains one USART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 MBit/s.
- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Supports a full modem control handshake interface.
- Support for synchronous mode.

7.11 SSP serial I/O controller

The LPC11Axx contain two SSP controllers.

The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SPI mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC11Axx contains one I^2C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

Remark: On the WLCSP package, the bootloader configures the open-drain pins (PIO0_2 and PIO0_3) for the Serial Wire Debug (SWD) function.

7.12.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins (PIO0_2 and PIO0_3). The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s. For the I²C-bus specification, see *UM10204*.
- The true open-drain pins PIO0_2 and PIO0_3 can be configured with a 50 ns digital input glitch filter.
- If the true open-drain pins are used for other purposes, a limited-performance I²C-bus interface can be configured from a choice of six GPIO pins configured in open-drain mode and with a pull-up resistor. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.
- Fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C-bus are floating and do not disturb the bus.
- Easy to configure as master, slave, or master/slave.
- ROM-based I²C-bus driver routines to easily create applications.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 Configurable analog/mixed-signal subsystems

Multiple analog/mixed-signal subsystems can be configured by software from interconnected digital and analog peripherals. See Figure 6.

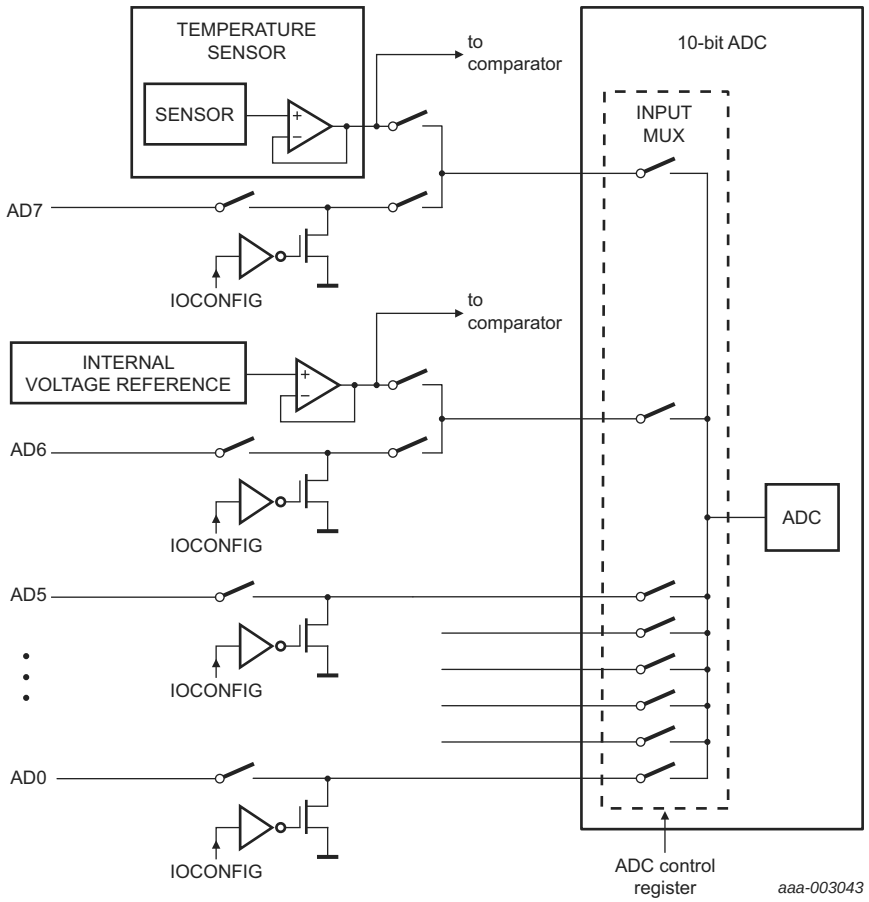


Fig 7. ADC block diagram

7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pins ATRG0 or ATRG1, timer match signal, or comparator output. (Input signals must be held for a minimum of three system clock periods). Also see Section 12.2.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.15 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V and varies typically only ±3 mV over the 0 °C to 85 °C temperature range (see Table 21 and Figure 27). The internal voltage reference can be used in the following applications:

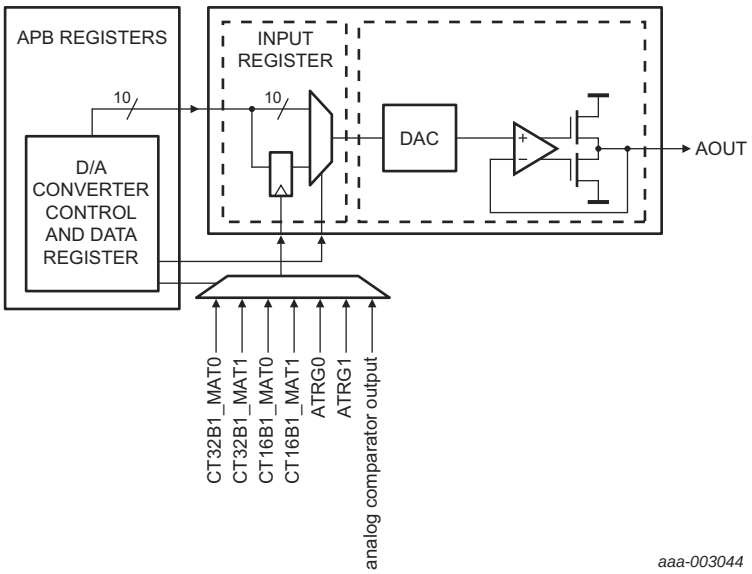


Fig 8. DAC block diagram

7.17.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
  - write operations to the DAC register.
  - a transition of pins ATRG0 or ATRG1. Input signals must be held for a minimum of three system clock periods.
  - a timer match signal.
  - a comparator output signal held for a minimum of two system clock periods.
- Holds output value during Sleep mode if the DAC is not powered down.

7.18 Analog comparator

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages. See Table 24.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

7.19 General purpose external event counter/timers

The LPC11Axx includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt. Up to three capture channels are pinned out. One channel is internally connected to the comparator output ACMP_O.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.20 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.21 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			2.6	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			2.6	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash; $V_{DD(3V3)} = V_{DD(IO)} = 3.3$ V; low-current mode (see Section 7.22.6.2)					
		system clock = 12 MHz; all peripherals disabled	[2][4][5]	-	3	-	mA
		system clock = 48 MHz; all peripherals disabled	[2][6][5]	-	8	-	mA
		Sleep mode; system clock = 12 MHz; $V_{DD(3V3)} = V_{DD(IO)} = 3.3$ V; low-current mode (see Section 7.22.6.2)					
		all peripherals disabled; 12 MHz	[2][4][5]	-	2	-	mA
		all peripherals disabled; 48 MHz	[2][4][5]	-	5	-	mA
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	$V_I = 0$ V; on-chip pull-up resistor disabled		-	0.5	1000	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	0.5	1000	nA
I_{OZ}	OFF-state output current	$V_O = 0$ V; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	0.5	1000	nA
V_I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
		5 V tolerant pins					
		3 V tolerant pins: PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package)	[7][8]			$V_{DD(IO)}$	
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	$3.0\text{ V} \leq V_{DD(IO)} \leq 3.6\text{ V}$		0.4	-	-	V

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−160	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−15	−50	−85	μA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_2 and PIO0_3)							
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3$V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.05$V_{DD(IO)}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as high-current sink pins 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[11]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; SysOsc disabled; system PLL disabled.

[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

[6] IRC disabled; SysOsc enabled; system PLL enabled.

[7] Including voltage on outputs in 3-state mode.

[8] All supply voltages must be present.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

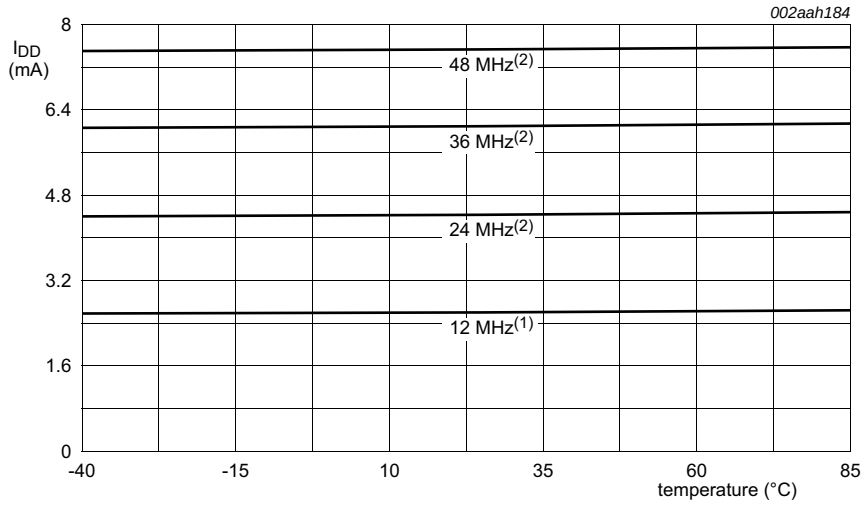
[10] Does not apply to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package).

[11] To V_{SS}.

9.1 Power consumption

Power measurements in Active and Sleep modes were performed under the following conditions (see *LPC11Axx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIO DIR registers to drive the outputs LOW.

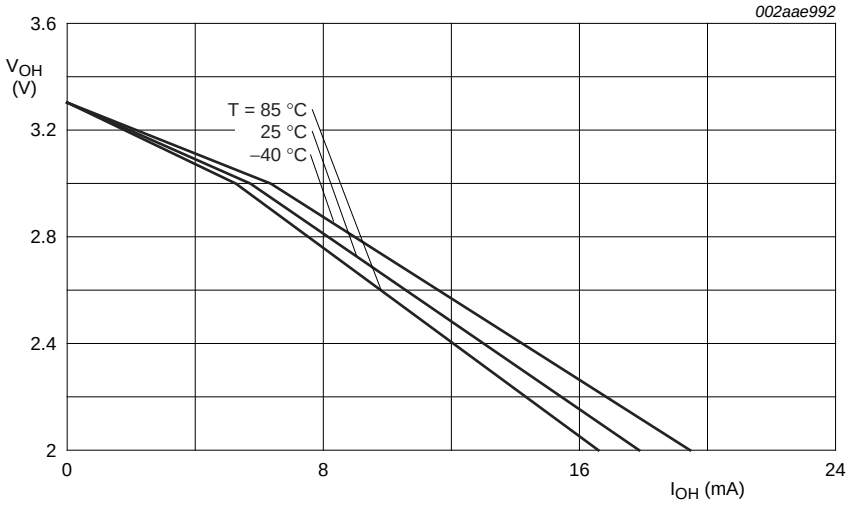


Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

(1) SysOsc and system PLL disabled; IRC enabled.

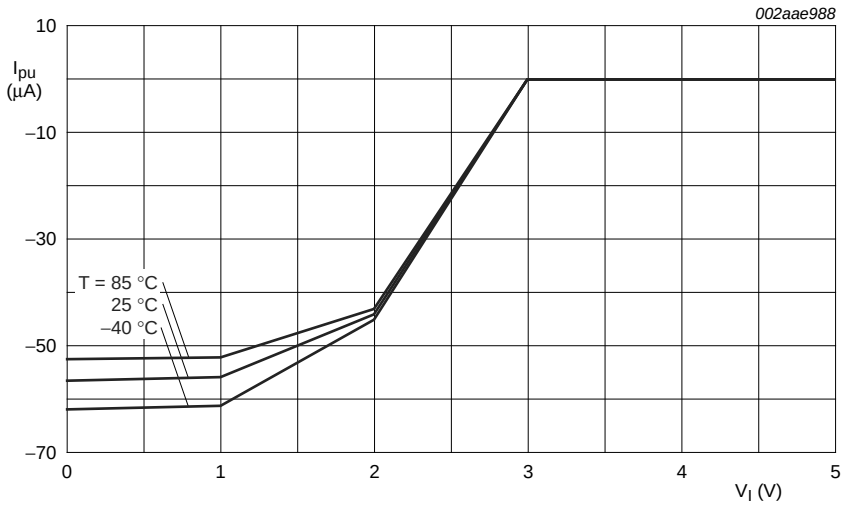
(2) SysOsc and system PLL enabled; IRC disabled.

Fig 11. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals disabled)



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 17. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 18. Typical pull-up current I_{pu} versus input voltage V_I

Table 9. Flash characteristics
T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered	[2]	10	20	-	years
		unpowered	[2]	20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors	[2]	95	100	105	ms
t_{prog}	programming time		[2][3]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[3] Programming times are given for writing 256 bytes to the flash. T_{amb} < +85 °C. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC11Axx user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

Table 10. EEPROM characteristics
T_{amb} = −55 °C to +125 °C; $V_{DD(3V3)}$ = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	100000	1000000	-	cycles
t_{ret}	retention time	powered	[1]	100	200	-	years
		unpowered	[1]	150	300	-	years
t_{prog}	programming time	64 bytes	[2]	-	1.1	-	ms

[1] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[2] T_{amb} < +85 °C.

10.3 External clock for oscillator in slave mode

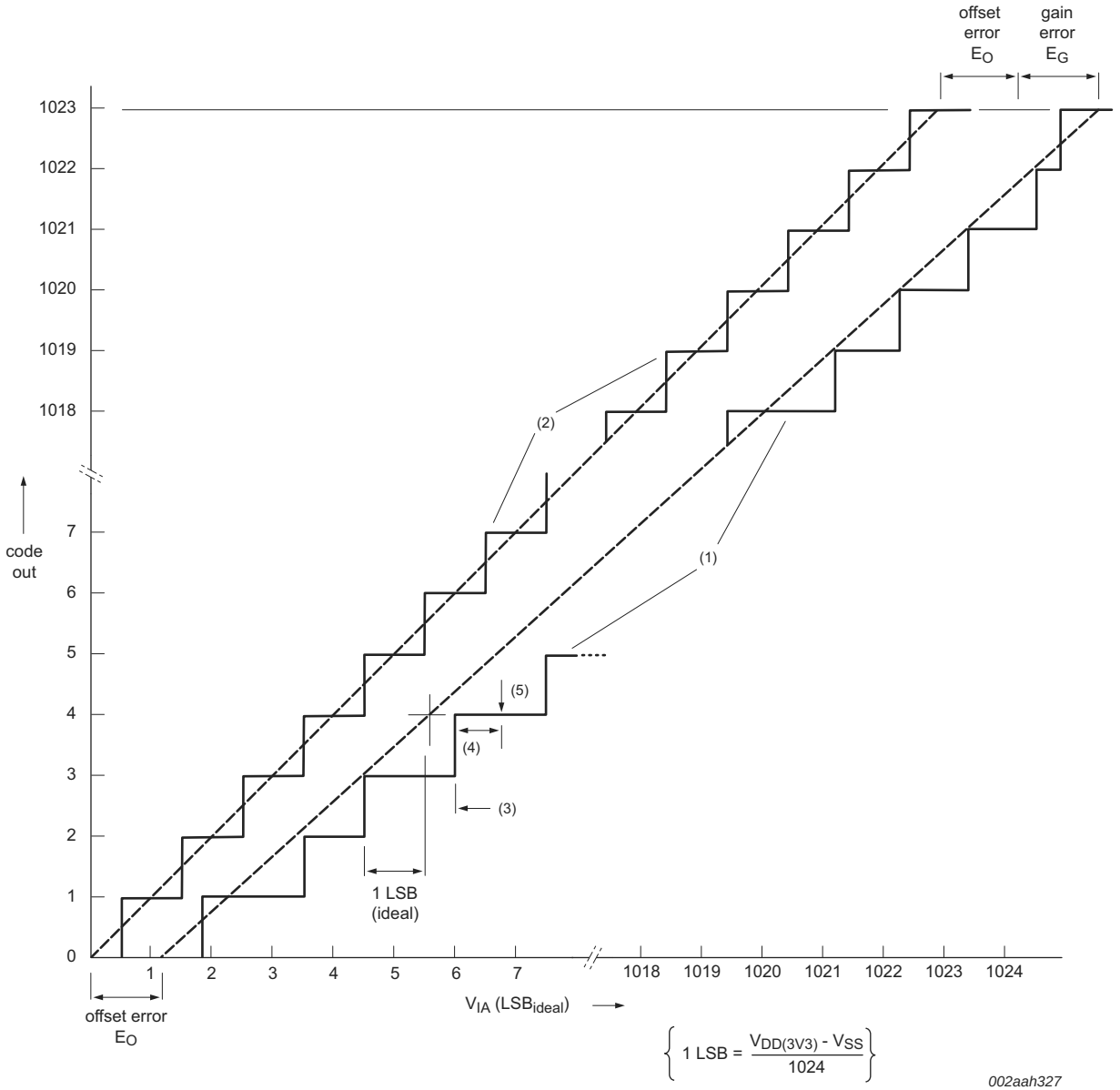
Remark: The input voltage on the XTALIN pin must be ≤ 1.95 V (see Table 6). For connecting the oscillator to the XTALIN/XTALOUT pins also see Section 12.3.

Table 11. Dynamic characteristic: external clock (XTALIN or CLKIN pin)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 26. ADC characteristics

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC11Axx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

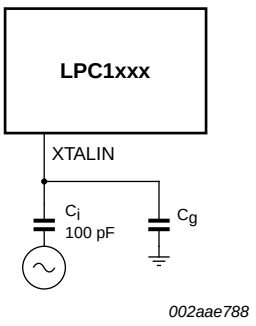


Fig 29. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 30 and in Table 27 and Table 28. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

16. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11AXX v.4	20121030	Product data sheet	-	LPC11AXX v.3
	• Parameter t_{PD} corrected in Table 25. • Editorial updates. • Maximum and minimum values for V_{DD} and $V_{DD(IO)}$ updated in Table 5 “Limiting values”. • Limiting values for parameter V_I added for open-drain pins PIO0_2 and PIO0_3 in Table 5 “Limiting values”. • Table 26 “Comparator voltage ladder reference static characteristics” updated. • Parameters $t_{s(pu)}$ and $t_{s(sw)}$ added to Table 21 “Internal voltage reference static and dynamic characteristics”. • Parameters V_{IA} and V_{trig} and $V_{i(xtal)}$ added to Table 5.			
LPC11AXX v.3	20120907	Product data sheet	-	LPC11AXX v.2.1
	• Section 10.1 abbreviated for clarity. • UVLO description including description of cold start-up behavior moved to the *LPC11Axx user manual*. • Table “Slew rate for the internal regulator power-up from ground” removed. This specification is included in the cold start-up description in the *LPC11Axx user manual*. • Details regarding boundary scan added to Section 7.24 “Emulation and debugging”. • Figure 33 “Functional diagram of the UVLO protection and reset timer circuit” updated to include the reset timer circuit. • Section 12.8 “Guidelines for selecting a power supply filter for UVLO protection” added. • Section 7.23.2 updated to include internal reset timer. • Parameter t_{PD} corrected in Table 24. • Parameter $E_{V(O)}$ corrected in Table 26.			
LPC11AXX v.2.1	20120704	Product data sheet	-	LPC11AXX v.2
	• Data sheet status changed to Product. • Changed Table note [2] in Table 24. • Changed Table note [1] in Table 8. • Added Table note [1] in Table 9. • Moved DT_{sen} and E_L values from typ to max in Table 22. • Corrected V_{esd} in Table 5. • Added Table note [5] and Table note [6] to Table 4.			

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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