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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MPU Core
Core Processor	ARM® Cortex®-A8, AM3359
Co-Processor	PowerVR SGX530
Speed	720MHz
Flash Size	1GB (NAND), 32MB (NOR)
RAM Size	512MB
Connector Type	SO-DIMM-204
Size / Dimension	-
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/dave-embedded-systems/ddf59100i

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Abbreviation	Definition
RTC	Real time clock
SOC	System-on-chip
SO-DIMM	Small Outline Dual In-line Memory Module
SOM	System-on-module
WDT	Watchdog

Tab. 2: Abbreviations and acronyms used in this manual

Feature	Specifications	Options
	timers (PWM function available) PWMSS (Pulse width modulation subsystem) with 3x eHRPWM, 3x eCap, 3x eQEP	
RTC	On board, external battery powered	
Debug	JTAG IEEE 1149.1 Test Access Port ETM Port ETB Port	
Miscellaneous	Up to 8x 12-bit ADC channels	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	[3.6 - 5.5] V, voltage regulation on board	
Active power consumption	Please refer to Power consumption section	
Dimensions	67.5 mm x 38.3 mm	
Weight	<tbd>	
MTBF	<tbd>	
Operation temperature	0..70 °C -40..+85 °C	
Shock	<tbd>	
Vibration	<tbd>	
Connectors	204-pin SO-DIMM	
Connectors insertion/removal	<tbd>	

Tab. 5: Electrical, Mechanical and Environmental Specifications

- Board width: 67.6 mm
- Height of all components is < 2.8 mm.
- PCB thickness is 1 mm.

The following figure highlights the maximum components' heights on DIVA module:

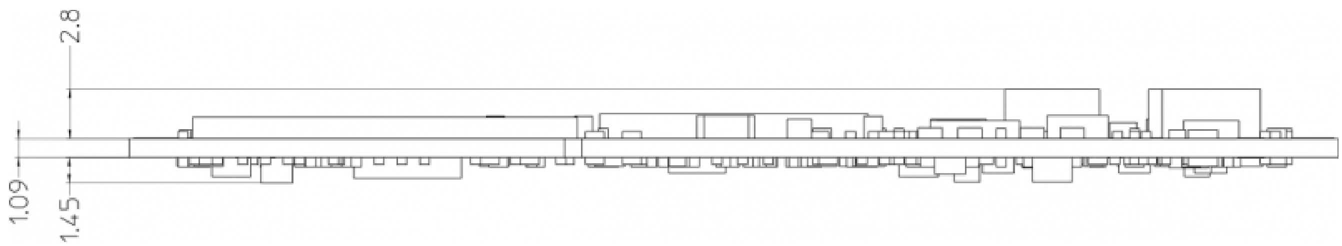

Fig. 5: DIVA module - Side view

4.2 Connectors

The following figure shows the DIVA SODIMM connector layout:

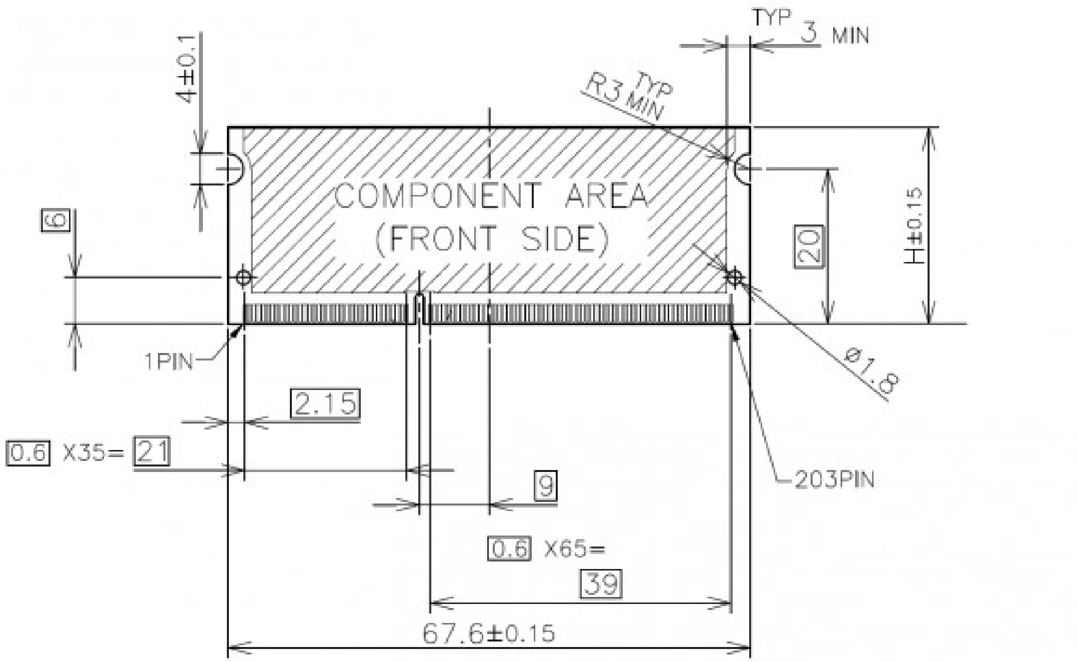

Fig. 6: Connectors layout

The following table reports the connectors specifications:

Part number	Standard SO-DIMM 204-pin (DDR3)
Mating connectors	DDR3 SO-DIMM SOCKET Part number : TE Connectivity 2013289-1 (used on DIVAEVB-Lite)

5 Power, reset and control

5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for AM335x processors family is not a trivial task because several power rails are involved. DIVA SOM simplifies this task and embeds all the needed circuitry. The following picture shows a

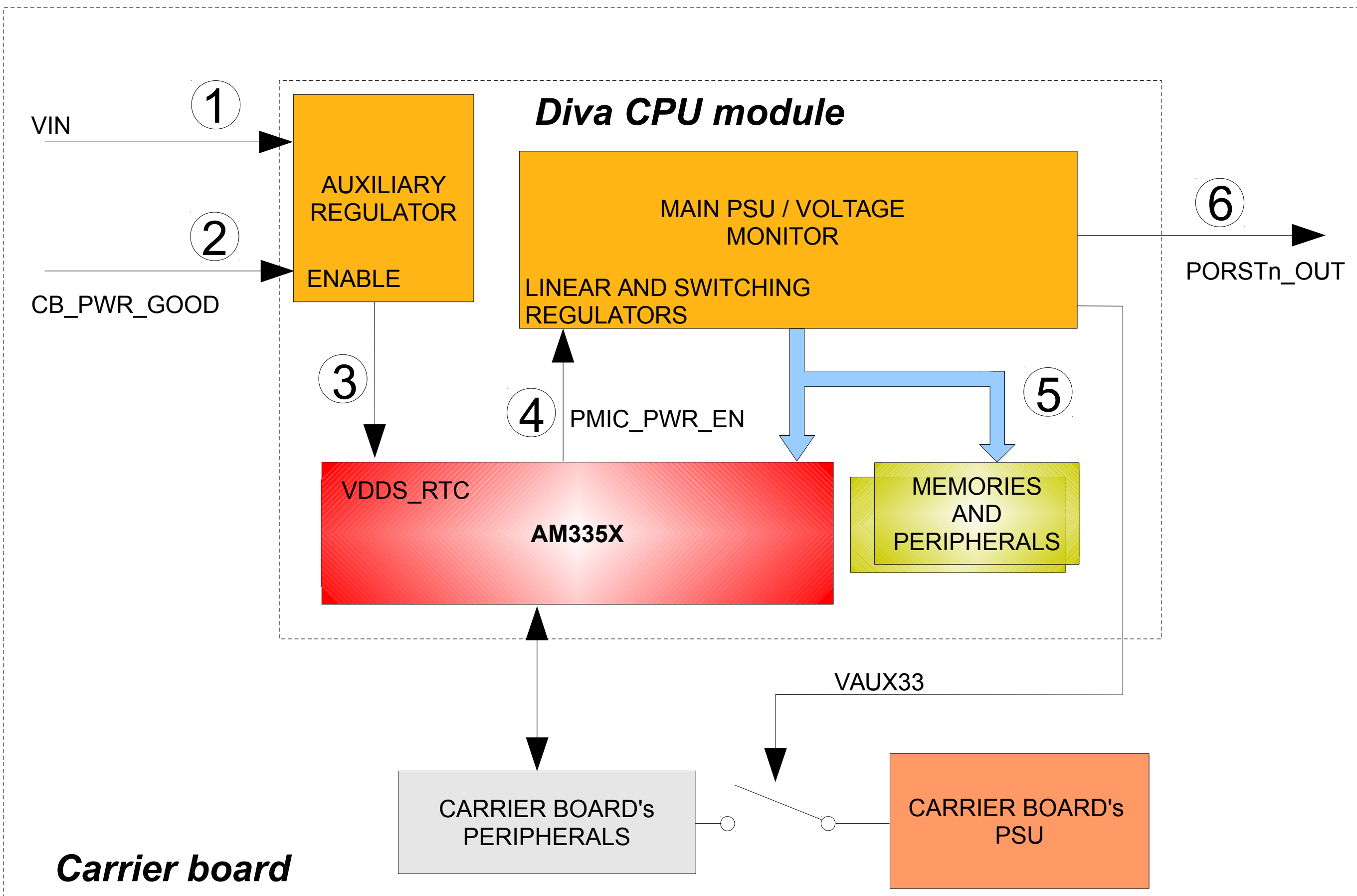

Fig. 7: DIVA power-up sequence

simplified block diagram of PSU/voltage monitoring circuitry:

is running, reprogramming the flash memory is straightforward.

*The UART boot uses **UART0** interface.*

5.6.3 SD/MMC Recovery

MMC recovery is a valuable option that requires no special hardware at all, apart a properly formatted MMC. The boot sequence must include the SD/MMC option and a way to enable it. When SD/MMC boot option is selected, bootrom looks for a valid boot sector on SD/MMC0. Once the board is running after booting from SD, reprogramming the flash memory is straightforward.

5.7 Multiplexing

AM335x pins can have up to eight alternate function modes. The I/O pins can be internally routed to/from one of several peripheral modules within the device: this routing is referred to as Pin Multiplexing. Pin Multiplexing allows software to choose the subset of internal signals which will be mapped to balls of the device for a given application. Pin multiplexing selects which one of several peripheral pin functions controls the pin's I/O buffer output data values.

Please note that pin mux configuration is a very critical step. Wrong configuration may lead to system instability, side effects or even damage the hardware permanently

Pin multiplexing configuration is quite complex in DIVA but a tool from TI, the Pin Mux Utility, can help to perform this operation. Software installation and generic usage documentation is available on this page of the TI Embedded Processors Wiki:
http://processors.wiki.ti.com/index.php/Pin_Mux_Utility_for_ARM_MPU_Processors

6.1 Carrier board mating connector J1

Pin	Pin Name	Internal Connections	Ball/ pin #	Supply Group	Type	Voltage	Note
1	DGND	DGND	-				
2	AM335X_GPMC_WPn	CPU.[GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MII1_TXEN/UART4_TXD/GPIO0_31]	U17				
3	AM335X_I2C0_SCL	CPU.[I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6]	C16				Internally connected to a 10K pull-up resistor
4	AM335X_GPMC_CS0n	CPU.[GPMC_CSN0///////GPIO1_29]	V6				Internally connected to the NAND flash (if present)
5	AM335X_I2C0_SDA	CPU.[I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT////GPIO3_5]	C17				Internally connected to a 10K pull-up resistor
6	AM335X_GPMC_CS1n	CPU.[GPMC_CSN1/GPMC_CLK/MMC1_CLK/PR1_EDIO_DATA_IN6/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30]	U9				
7	WD_SET0	WDT.SET0	4				
8	AM335X_GPMC_CS2n	CPU.[GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31]	V9				
9	WD_SET1	WDT.SET1	5				
10	AM335X_GPMC_CS3n	CPU.[GPMC_CSN3///MMC2_CMD/PR1_MII0_CRS/PR1_MDIO_DATA/EMU4/GPIO2_0]	T13				
11	WD_SET2	WDT.SET2	6				
12	DGND	DGND	-				
13	EEPROM_WP	EEPROM.WP	7				

		EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12]					
115	AM335X_MMC_D1	CPU. [MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28]	G15				
116	AM335X_LCD_DATA7	CPU. [LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13]	T4				
117	AM335X_MMC_D0	CPU. [MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29]	G16				
118	AM335X_LCD_DATA8	CPU. [LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14]	U1				
119	AM335X_MMC_CMD	CPU. [MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31]	G18				
120	AM335X_LCD_DATA9	CPU. [LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15]	U2				
121	DGND	DGND	-				
122	AM335X_LCD_DATA10	CPU. [LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16]	U3				
123	AM335X_MMC_CLK	CPU. [MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30]	G17				
124	AM335X_LCD_DATA11	CPU. [LCD_DATA11/GPMC_A15/EHRPWM1B/MCAS	U4				

141	DGND	DGND	-				
142	AM335X_MCASP0_AXR0	CPU. [MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16]	D12				
143	ETH_CTRD						
144	AM335X_MCASP0_AHCLKR	CPU. [MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17]	C12				
145	ETH_TX-	ETHPHY.TXN	28				
146	AM335X_MCASP0_ACLKR	CPU. [MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18]	B12				
147	ETH_TX+	ETHPHY.TXP	29				
148	AM335X_MCASP0_AHCLKX	CPU. [MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21]	A14				
149	ETH_RX-	ETHPHY.RXN	30				
150	AM335X_MCASP0_ACLKX	CPU. [MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14]	A13				
151	ETH_RX+	ETHPHY.RXP	31				
152	DGND	DGND	-				
153	EMAC0_PHY_LED_SPEED	ETHPHY.LED2/nINTSEL	2				10kOhm pull-down
154	NC/OUT_PMIC_VRTC//OUT_VDD3_SMPS//OUT_VDIG1						By default this pin must not be connected. Optionally it can route power voltages generated by DIVA PSU. This option is meant to allow monitoring of such voltages by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
155	EMAC0_PHY_LED_LINK/ACT	ETHPHY.LED1/nREGOFF	3				

7.5.1 MMC/SD/SDIO0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
MMC0_CLK	J1.123	MMC/SD/SDIO Clock	
MMC0_CMD	J1.119	MMC/SD/SDIO Command	
MMC0_DAT0	J1.117	MMC/SD/SDIO Data bus	
MMC0_DAT1	J1.115	MMC/SD/SDIO Data bus	
MMC0_DAT2	J1.113	MMC/SD/SDIO Data bus	
MMC0_DAT3	J1.111	MMC/SD/SDIO Data bus	
MMC0_DAT4	J1.173	MMC/SD/SDIO Data bus	
MMC0_DAT5	J1.171	MMC/SD/SDIO Data bus	
MMC0_DAT6	J1.175	MMC/SD/SDIO Data bus	
MMC0_DAT7	J1.177	MMC/SD/SDIO Data bus	
MMC0_POW	J1.51 J1.23	MMC/SD Power switch control	
MMC0_SDCD	J1.51 J1.150 J1.167	MMC/SD Card Detect	
MMC0_SDWP	J1.109 J1.146 J1.165	MMC/SD Write Protect	

7.5.2 MMC/SD/SDIO 1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
MMC1_CLK	J1.6	MMC/SD/SDIO	

Pin name	Conn. Pin	Function	Notes
AIN0	J1.87	Analog Input/Output	
AIN1	J1.89	Analog Input/Output	
AIN2	J1.91	Analog Input/Output	
AIN3	J1.95	Analog Input/Output	
AIN4	J1.97	Analog Input	
AIN5	J1.99	Analog Input	
AIN6	J1.103	Analog Input	
AIN7	J1.105	Analog Input	
AGND_TSC	J1.93 J1.101 J1.107	Analog TSC ground	

7.8 LCD controller

The AM335x integrates an LCD Controller which provides support for up to 24-bit data output (RGB, 8 bits-per-pixel) and up to WXGA (1366x768) resolution. It can drive Character, STN, TFT and OLED panels. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LCD_AC_BIAS_EN	J1.98	LCD AC bias enable chip select	
LCD_DATA0	J1.100	LCD Data bus	
LCD_DATA1	J1.102	LCD Data bus	
LCD_DATA2	J1.104	LCD Data bus	
LCD_DATA3	J1.106	LCD Data bus	
LCD_DATA4	J1.108	LCD Data bus	
LCD_DATA5	J1.110	LCD Data bus	
LCD_DATA6	J1.114	LCD Data bus	
LCD_DATA7	J1.116	LCD Data bus	

Pin name	Conn. Pin	Function	Notes
SPI0_CS0	J1.49	SPI0 Chip Select #0	
SPI0_CS1	J1.51	SPI0 Chip Select #1	
SPI0_D0	J1.45	SPI0 data	
SPI0_D1	J1.47	SPI0 data	
SPI0_SCLK	J1.43	SPI0 clock	

7.9.2 SPI channel 1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SPI1_CS0	J1.27 J1.29 J1.39 J1.144	SPI1 Chip Select #0	
SPI1_CS1	J1.25 J1.37 J1.69 J1.109	SPI1 Chip Select #1	
SPI1_D0	J1.31 J1.140	SPI1 data	
SPI1_D1	J1.29 J1.142	SPI1 data	
SPI1_SCLK	J1.109 J1.150 J1.169	SPI1 clock	

7.10 I2C buses

Up to three I2C channels are available on DIVA to provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module. The I2C ports support standard (up to 100 Kbps) and fast (up to 400 Kbps) modes; the controller supports the multi-master mode that allows more than one device capable of controlling the bus to be connected to it.

7.10.1 I2C channel 0

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C0_SCL	J1.3	I2C0 clock	Internally connected to a 10K pull-up resistor
I2C0_SDA	J1.5	I2C0 data	Internally connected to a 10K pull-up resistor

7.10.2 I2C channel 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C1_SCL	J1.29 J1.33 J1.49	I2C1 clock	No pull-up/pull-down
I2C1_SDA	J1.31 J1.35 J1.47	I2C1 data	No pull-up/pull-down

7.10.3 I2C channel 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C2_SCL	J1.25 J1.37 J1.45	I2C2 clock	No pull-up/pull-down
I2C2_SDA	J1.27 J1.39 J1.43	I2C2 data	No pull-up/pull-down

Pin name	Conn. Pin	Function	Notes
		14	
GPMC_A15	J1.124	GPMC Address bit 15	
GPMC_A16	J1.28 J1.126	GPMC Address bit 16	
GPMC_A17	J1.30 J1.128	GPMC Address bit 17	
GPMC_A18	J1.34 J1.130	GPMC Address bit 18	
GPMC_A19	J1.36 J1.134	GPMC Address bit 19	
GPMC_A20	J1.38 J1.111	GPMC Address bit 20	
GPMC_A21	J1.40 J1.113	GPMC Address bit 21	
GPMC_A22	J1.42 J1.115	GPMC Address bit 22	
GPMC_A23	J1.44 J1.117	GPMC Address bit 23	
GPMC_A24	J1.46 J1.123	GPMC Address bit 24	
GPMC_A25	J1.48 J1.119	GPMC Address bit 25	
GPMC_A26	J1.50	GPMC Address bit 26	
GPMC_A27	J1.54	GPMC Address bit 27	
GPMC_AD0	J1.56	GPMC Address and Data bit 0	
GPMC_AD1	J1.58	GPMC Address and Data bit 1	
GPMC_AD2	J1.60	GPMC Address and Data bit 2	
GPMC_AD3	J1.62	GPMC Address and Data bit 3	
GPMC_AD4	J1.64	GPMC Address and Data bit 4	

Connector Pin	Pin name	Function	Notes
EHRPWM0B	J1.45 J1.140	eHRPWM0 B output.	
EHRPWM0_SYNCI	J1.49 J1.144	Sync input to eHRPWM0 module from an external pin	
EHRPWM0_SYNCO	J1.106	Sync Output from eHRPWM0 module to an external pin	
EHRPWM0_TRIPZONE_INPUT	J1.47 J1.142	eHRPWM0 trip zone input	

7.15.2 eHRPWM 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EHRPWM1A	J1.34 J1.122	eHRPWM1 A output.	
EHRPWM1B	J1.36 J1.124	eHRPWM1 B output.	
EHRPWM1_TRIPZONE_INPUT	J1.28 J1.118	eHRPWM1 trip zone input	

7.15.3 eHRPWM 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EHRPWM2A	J1.74 J1.100	eHRPWM2 A output.	
EHRPWM2B	J1.76 J1.102	eHRPWM2 B output.	
EHRPWM2_TRIPZONE_INPUT	J1.78 J1.104	eHRPWM2 trip zone input	

7.15.4 eCAP

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
ECAP0_IN_PWM0_OUT	J1.109	Enhanced Capture 0 input or Auxiliary PWM0 output	
ECAP1_IN_PWM1_OUT	J1.3 J1.25 J1.51	Enhanced Capture 1 input or Auxiliary PWM1 output	
ECAP2_IN_PWM2_OUT	J1.5 J1.27 J1.144	Enhanced Capture 2 input or Auxiliary PWM2 output	

7.15.5 eQEP 0

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP0A_IN	J1.146	eQEP0A quadrature input	
EQEP0B_IN	J1.136	eQEP0B quadrature input	
EQEP0_INDEX	J1.138	eQEP0 index	
EQEP0_STROBE	J1.148	eQEP0 strobe	

7.15.6 eQEP 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP1A_IN	J1.38 J1.126	eQEP1A quadrature input	
EQEP1B_IN	J1.40 J1.128	eQEP1B quadrature input	
EQEP1_INDEX	J1.42 J1.130	eQEP1 index	
EQEP1_STROBE	J1.44 J1.134	eQEP1 strobe	

7.15.7 eQEP 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP2A_IN	J1.82 J1.108	eQEP2A quadrature input	
EQEP2B_IN	J1.84 J1.110	eQEP2B quadrature input	
EQEP2_INDEX	J1.86 J1.114	eQEP2 index	
EQEP2_STROBE	J1.88 J1.116	eQEP2 strobe	

The test bench runs the following software:

- burnCortexA8 in continuous loop
- MEMTest: memtester 6M 1 with logddrXXX.txt
- USB:
  - mount
  - head -c 10485760 /dev/urandom
  - md5sum
  - copy
  - md5sum
  - diff md5
  - remount
  - md5sum
  - diff md5
  - umount
- NAND: mtd13 mtd14
  - flash_erase
  - nandbadcount /dev/mtd
- slide_show with fbi

8.3.1.1 Results

With this test bench, the **CPU load is always 100%** and many components are active at the same time, so this is a non-realistic worst case scenario. The average measured power consumption is **2,6 W**.

8.4 Heat Dissipation

This section will be completed in a future version of this manual.