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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	65536
Number of I/O	260
Number of Gates	322970
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/5962-9957201nna

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, max	V, min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	(2)	(2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	(2)	(2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	-8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.65	V_{REF} + 0.65	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	(2)	(2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

IOB Input Switching Characteristics Standard Adjustments

Symbol	Description	Standard	Speed Grade	Units
			-4	
Data Input Delay Adjustments				
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0.0	ns
$T_{ILVCMOS2}$		LVCMOS2	–0.05	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	–0.14	ns
T_{IPCI33_5}		PCI, 33 MHz, 5.0V	0.33	ns
T_{IGTL}		GTL	0.26	ns
T_{IGTLP}		GTL+	0.14	ns
T_{IHSTL}		HSTL	0.04	ns
T_{ISSTL2}		SSTL2	–0.10	ns
T_{ISSTL3}		SSTL3	–0.06	ns
T_{ICTT}		CTT	0.02	ns
T_{IAGP}		AGP	–0.08	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.

Symbol	Description	Speed Grade		Units
		-4		
		Min	Max	
Propagation Delays				
T_{IOOP}	O input to pad	-	3.5	ns
T_{IOOLP}	O input to pad via transparent latch	-	4.0	ns
3-State Delays				
T_{IOTHZ}	T input to pad high-impedance(1)	-	2.4	ns
T_{IOTON}	T input to valid data on pad	-	3.7	ns
$T_{IOTLPHZ}$	T input to pad high-impedance via transparent latch(1)	-	3.0	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	-	4.2	ns
T_{GTS}	GTS to pad high-impedance(1)	-	6.3	ns
Sequential Delays				
T_{IOCKP}	Clock CLK to pad	-	3.5	ns
T_{IOCKHZ}	Clock CLK to pad high-impedance (synchronous)(1)	-	2.9	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	4.1	ns
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time(2)**		
T_{IOOCK}/T_{IOCKO}	O input	1.3 / 0	-	ns
$T_{IOOCECK}/T_{IOCKOCE}$	OCE input	1.0 / 0	-	ns
$T_{IOSRCKO}/T_{IOCKOSR}$	SR input (OFF)	1.4 / 0	-	ns
T_{IOTCK}/T_{IOCKT}	3-state setup times, T input	0.9 / 0	-	ns
$T_{IOTCECK}/T_{IOCKTCE}$	3-state setup times, TCE input	1.1 / 0	-	ns
$T_{IOSRCKT}/T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.3 / 0	-	ns
Set/Reset Delays				
T_{IOSRP}	SR input to pad (asynchronous)	4.6	-	ns
T_{IOSRHZ}	SR input to pad high-impedance (asynchronous)(1)	3.9	-	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	5.1	-	ns

Notes:
1. High-impedance turn-off delays should not be adjusted.
2. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Symbol	Description	Standard		Speed Grade -4	Units
Output Delay Adjustments					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{sl})	LVTTL, slow	2 mA	17.0	ns
T_{OLVTTL_S4}			4 mA	8.6	ns
T_{OLVTTL_S6}			6 mA	5.6	ns
T_{OLVTTL_S8}			8 mA	3.5	ns
T_{OLVTTL_S12}			12 mA	2.2	ns
T_{OLVTTL_S16}			16 mA	2.0	ns
T_{OLVTTL_S24}			24 mA	1.6	ns
T_{OLVTTL_F2}		LVTTL, fast	2 mA	15.1	ns
T_{OLVTTL_F4}			4 mA	6.1	ns
T_{OLVTTL_F6}			6 mA	3.6	ns
T_{OLVTTL_F8}			8 mA	1.2	ns
T_{OLVTTL_F12}			12 mA	0.0	ns
T_{OLVTTL_F16}			16 mA	–0.05	ns
T_{OLVTTL_F24}			24 mA	–0.23	ns
$T_{OLVCMOS2}$		LVCMOS2		0.12	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V		2.7	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V		3.3	ns
T_{OGTL}		GTL		0.6	ns
T_{OGTLP}		GTL+		1.0	ns
T_{OHSTL_I}		HSTL I		–0.5	ns
T_{OHSTL_III}		HSTL III		–1.0	ns
T_{OHSTL_IV}		HSTL IV		–1.1	ns
T_{OSSTL2_I}		SSTL2 I		–0.5	ns
T_{OSSTL2_II}		SSTL2 II		–1.0	ns
T_{OSSTL3_I}		SSTL3 I		–0.5	ns
T_{OSSTL3_II}		SSTL3 II		–1.1	ns
T_{OCTT}		CTT		–0.6	ns
T_{OAGP}		AGP		–1.0	ns

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-4		
		Min	Max	
Combinatorial Delays				
T_{ILO}	4-input function: F/G inputs to X/Y outputs	-	0.8	ns
T_{IF5}	5-input function: F/G inputs to F5 output	-	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	-	1.0	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	-	1.2	ns
T_{F5INY}	6-input function: F5IN input to Y output	-	0.5	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.8	ns
T_{BYYB}	BY input to YB output	-	0.7	ns
Sequential Delays				
T_{CKO}	FF clock CLK to XQ/YQ outputs	-	1.4	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	-	1.6	ns
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time**		
T_{ICK}/T_{CKI}	4-input function: F/G Inputs	1.5 / 0	-	ns
T_{IF5CK}/T_{CKIF5}	5-input function: F/G inputs	1.7 / 0	-	ns
T_{F5INCK}/T_{CKF5IN}	6-input function: F5IN input	1.2 / 0	-	ns
T_{IF6CK}/T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.9 / 0	-	ns
T_{DICK}/T_{CKDI}	BX/BY inputs	0.8 / 0	-	ns
T_{CECK}/T_{CKCE}	CE input	1.0 / 0	-	ns
$T_{RCK}T_{CKR}$	SR/BY inputs (synchronous)	0.9 / 0	-	ns
Clock CLK				
T_{CH}	Minimum pulse width, High	2.0	-	ns
T_{CL}	Minimum pulse width, Low	2.0	-	ns
Set/Reset				
T_{RPW}	Minimum pulse width, SR/BY inputs	3.3	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	-	1.4	ns
T_{IOGSRQ}	Delay from GSR to XQ/YQ outputs	-	12.5	ns

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-4		
		Min	Max	
Combinatorial Delays				
T_{OPX}	F operand inputs to X via XOR	-	1.0	ns
T_{OPXB}	F operand input to XB output	-	1.4	ns
T_{OPY}	F operand input to Y via XOR	-	2.0	ns
T_{OPYB}	F operand input to YB output	-	2.0	ns
T_{OPCYF}	F operand input to COUT output	-	1.5	ns
T_{OPGY}	G operand inputs to Y via XOR	-	1.2	ns
T_{OPGYB}	G operand input to YB output	-	2.1	ns
T_{OPCYG}	G operand input to COUT output	-	1.6	ns
T_{BXCY}	BX initialization input to COUT	-	1.1	ns
T_{CINX}	CIN input to X output via XOR	-	0.6	ns
T_{CINXB}	CIN input to XB	-	0.1	ns
T_{CINY}	CIN input to Y via XOR	-	0.6	ns
T_{CINYB}	CIN input to YB	-	0.6	ns
T_{BYP}	CIN input to COUT output	-	0.2	ns
Multiplier Operation				
T_{FANDXB}	F1/2 operand inputs to XB output via AND	-	0.5	ns
T_{FANDYB}	F1/2 operand inputs to YB output via AND	-	1.1	ns
T_{FANDCY}	F1/2 operand inputs to COUT output via AND	-	0.6	ns
T_{GANDYB}	G1/2 operand inputs to YB output via AND	-	0.7	ns
T_{GANDCY}	G1/2 operand inputs to COUT output via AND	-	0.2	ns
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time**		
T_{CCKX}/T_{CKCX}	CIN input to FFX	1.3 / 0	-	ns
T_{CCKY}/T_{CKCY}	CIN input to FFY	1.4 / 0	-	ns

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB SelectRAM Switching Characteristics

Symbol	Description	Speed Grade -4 Min	Speed Grade -4 Max	Units
Sequential Delays				
T_{SHCKO}	Clock CLK to X/Y outputs (WE active)	-	3.0	ns
Shift-Register Mode				
T_{SHCKO}	Clock CLK to X/Y outputs	-	3.0	ns
Setup Times before Clock CLK		**Setup Time / Hold Time**		
T_{AS}/T_{AH}	F/G address inputs	0.7 / 0	-	ns
T_{DS}/T_{DH}	BX/BY data inputs (DIN)	0.9 / 0	-	ns
T_{WS}/T_{WH}	CE input (WE)	1.0 / 0	-	ns
Shift-Register Mode				
T_{SHDICK}	BX/BY data inputs (DIN)	0.9	-	ns
T_{SHCECK}	CE input (WS)	1.0	-	ns
Clock CLK				
T_{WPH}	Minimum pulse width, High	3.1	-	ns
T_{WPL}	Minimum pulse width, Low	3.1	-	ns
T_{WC}	Minimum clock period to meet address write cycle time	6.2	-	ns
Shift-Register Mode				
T_{SRPH}	Minimum pulse width, High	3.1	-	ns
T_{SRPL}	Minimum pulse width, Low	3.1	-	ns

BLOCKRAM Switching Characteristics

Symbol	Description	Speed Grade -4 Min	Speed Grade -4 Max	Units
Sequential Delays				
T_{BCKO}	Clock CLK to DOUT output	-	4.1	ns
Setup Times Before Clock Clk				
T_{BACK}/T_{BCKA}	ADDR inputs	1.5 / 0	-	ns
T_{BDCK}/T_{BCKD}	DIN inputs	1.5 / 0	-	ns
T_{BECK}/T_{BCKE}	EN input	3.4 / 0	-	ns
T_{BRCK}/T_{BCKR}	RST input	3.2 / 0	-	ns
T_{BWCK}/T_{BCKW}	WEN input	3.0 / 0	-	ns
Clock CLK				
T_{BPWH}	Minimum pulse width, High	2.0	-	ns
T_{BPWL}	Minimum pulse width, Low	2.0	-	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	4.0	-	ns

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade -4 Min	Speed Grade -4 Max	Units
Combinatorial Delays				
T_{IO}	IN input to OUT output	-	0.0	ns
T_{OFF}	TRI input to OUT output high-impedance	-	0.2	ns
T_{ON}	Tri input to valid data on OUT output	-	0.2	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade -4 Min	Speed Grade -4 Max	Units
T_{TAPTCK}	TMS and TDI setup times before TCK	4.0	-	ns
T_{TCKTAP}	TMS and TDI hold times after TCK	2.0	-	ns
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	ns
F_{TCK}	Maximum TCK clock frequency	-	33	MHz

Virtex Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -4 Max	Units
	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	XQV100	-	3.6	ns
		XQV300	-	3.6	ns
		XQV600	-	3.6	ns
		XQV1000	-	3.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 2.
3. DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -4 Max	Units
	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	XQV100	-	5.7	ns
		XQV300	-	5.9	ns
		XQV600	-	6.0	ns
		XQV1000	-	6.3	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column,and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 2.

Minimum Clock to Out for Virtex Devices

I/O Standard	With DLL	Without DLL				
	All Devices	V100	V300	V600	V1000	Units
LVTTL_S2(1)	5.2	6.0	6.1	6.1	6.1	ns
LVTTL_S4(1)	3.5	4.3	4.4	4.4	4.4	ns
LVTTL_S6(1)	2.8	3.6	3.7	3.7	3.7	ns
LVTTL_S8(1)	2.2	3.1	3.1	3.2	3.2	ns
LVTTL_S12(1)	2.0	2.9	2.9	3.0	3.0	ns
LVTTL_S16(1)	1.9	2.8	2.8	2.9	2.9	ns
LVTTL_S24(1)	1.8	2.6	2.7	2.7	2.8	ns
LVTTL_F2(1)	2.9	3.8	3.8	3.9	3.9	ns
LVTTL_F4(1)	1.7	2.6	2.6	2.7	2.7	ns
LVTTL_F6(1)	1.2	2.0	2.1	2.1	2.2	ns
LVTTL_F8(1)	1.1	1.9	2.0	2.0	2.0	ns
LVTTL_F12(1)	1.0	1.8	1.9	1.9	1.9	ns
LVTTL_F16(1)	0.9	1.8	1.8	1.8	1.9	ns
LVTTL_F24(1)	0.9	1.7	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.5	2.5	ns
PCI33_5	1.4	2.2	2.3	2.3	2.4	ns
GTL	1.6	2.5	2.5	2.6	2.6	ns
GTL+	1.7	2.5	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.7	1.7	1.7	1.8	ns
SSTL3 II	0.7	1.5	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.9	1.9	2.0	ns

Notes:
1. S = Slow Slew Rate, F = Fast Slew Rate
2. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column. and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
3. Output timing is measured at 50% V_{CC} threshold with 8 pF external capacitive load.

Virtex Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Setup and Hold for LVTTL Standard, *with* DLL

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -4 Max	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.					
T_{PSDLL}/T_{PHDLL}	**No Delay** Global clock and IFF, with DLL	XQV100	2.1 / –0.4	-	ns
		XQV300	2.1 / –0.4	-	ns
		XQV600	2.1 / –0.4	-	ns
		XQV1000	2.1 / –0.4	-	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -4 Max	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.					
T_{PSFD}/T_{PHFD}	**Full Delay** Global clock and IFF, without DLL	XQV100	3.0 / 0.0	-	ns
		XQV300	3.1 / 0.0	-	ns
		XQV600	3.3 / 0.0	-	ns
		XQV1000	3.6 / 0.0	-	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

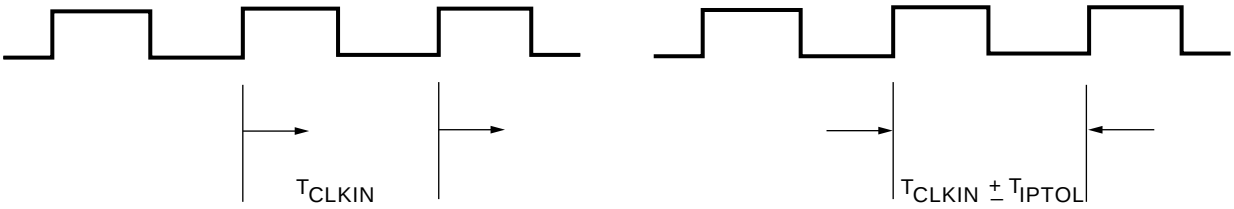
Symbol	Description	Speed Grade -4		Units
		Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	180	MHz
$F_{CLKINLF}$	Inputclock frequency (CLKDLL)	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	3.0	-	ns

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to +100°C).

Symbol	Description		CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter cycle to cycle		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire Lock						
	F_{CLKIN}	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{SKEW}	DLL output skew (between any DLL output)		-	±150	-	±150	ps
T_{OPHASE}	DLL output long term phase differential		-	±100	-	±100	ps
T_{OJITCC}	DLL output ditter cycle to cycle		-	±60	-	±60	ps

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to +100°C).

Period Tolerance: the allowed input clock period change in nanoseconds.



Clock Jitter: the difference between an ideal reference clock edgfe and the actual design.

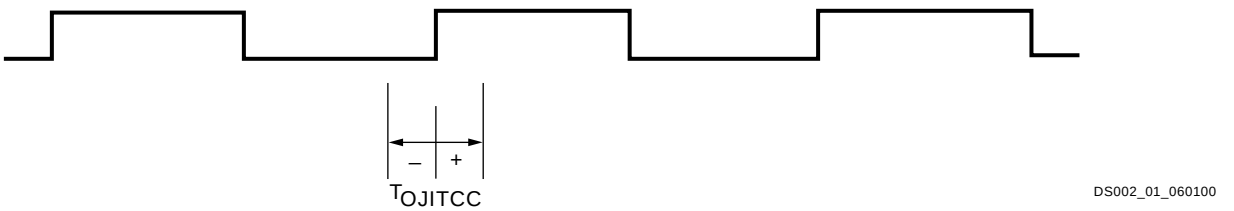


Figure 1: **Frequency Tolerance and Clock Jitter**

QPro Virtex Pinouts

Pinout Tables

See the Xilinx WebLINX web site (http://www.xilinx.com/partinfo/databook.htm) for updates or additional pinout information. For convenience, Table 3, Table 4 and Table 5 list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

Table 3: **Virtex QFP Package Pinout Information**

Pin Name	Device	PQ/HQ240
GCK0	All	92
GCK1	All	89
GCK2	All	210
GCK3	All	213
M0	All	60
M1	All	58
M2	All	62
CCLK	All	179
PROGRAM	All	122
DONE	All	120
INIT	All	123
BUSY/DOUT	All	178
D0/DIN	All	177
D1	All	167
D2	All	163
D3	All	156
D4	All	145
D5	All	138
D6	All	134
D7	All	124
WRITE	All	185
CS	All	184
TDI	All	183
TDO	All	181
TMS	All	2
TCK	All	239
V_{CCINT}	All	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225
V_{CCO} (The V_{CCO} for the PQ/HQ240 package is common to all eight I/O banks. Different output standards per I/O bank that require different V_{CCO} values cannot be supported.)	All	15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
DXP	All	V4	AE24	AK29	AJ28
V_{CCINT} (V_{CCINT} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XQV100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	-	-	-
	XQV300	-	A20, B16, C14, D10, D12, J24, K4, L1, L25, P2, P25, R23, T1, V24, W2, AC10, AE14, AE19, AF11, AF16,	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22	-
	XQV600	-	-	... + B26, C7, F1, F30, AE29, AF1, AH8, AH24	-
	XQV1000	-	-	-	A21, B12, B14, B18, B28, C22, C24, E9, E12, F2, H30, J1, K32, M3, N1, N29, N33, U5, U30, Y2, Y31, AB2, AB32, AD2, AD32, AG3, AG31, AJ13, AK8, AK11, AK17, AK20, AL14, AL22, AL27, AN25
V_{CCO}, Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V_{CCO}, Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32
V_{CCO}, Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17. E4, E17, J4, J17, K4, K17, L4, L17, M4, M9, M10, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9, AL14, AL18, AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
GND(1)	All	J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11,M12	-	-	-
No Connect	-	-	-	-	C31, AC2, AK4, AL3

Notes:
1. 16 extra balls (grounded) at package center.

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO_VREF_5	79
IO	80
IO	81
IO	82
VCCINT	83
GCK1	84
VCCO	85
GND	86
GCKO	87
IO	88
IO	89
IO	90
IO	91
IO_VREF_4	92
IO	93
IO	94
VCCO	95
IO	96
IO	97
IO	98
VCCINT	99
GND	100
IO	101
IO_VREF_4	102
IO	103
IO	104
IO_VREF_4	105
GND	106
IO	107
IO	108
IO_VREF_4	109
IO	110
IO	111
IO	112
GND	113
DONE	114
VCCO	115
PROGRAM	116
IO_INIT	117
IO_D7	118

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO	119
IO_VREF_3	120
IO	121
IO	122
GND	123
IO_VREF_3	124
IO	125
IO	126
IO_VREF_3	127
IO_D6	128
GND	129
VCCINT	130
IO_D5	131
IO	132
VCCO	133
IO	134
IO	135
IO_VREF_3	136
IO_D4	137
IO	138
IO	139
VCCINT	140
IO_TRDY	141
VCCO	142
GND	143
IO_IRDY	144
IO	145
IO	146
IO	147
IO_D3	148
IO_VREF_2	149
IO	150
IO	151
VCCO	152
IO	153
IO	154
IO_D2	155
VCCINT	156
GND	157
IO_D1	158

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO_VREF_2	159
IO	160
IO	161
IO_VREF_2	162
GND	163
IO	164
IO	165
IO_VREF_2	166
IO	167
IO_DIN_D0	168
IO_DOUT_BUSY	169
CCLK	170
VCCO	171
TDO	172
GND	173
TDI	174
IO_CS	175
IO_WRITE	176
IO	177
IO_VREF_1	178
IO	179
GND	180
IO_VREF_1	181
IO	182
IO	183
IO_VREF_1	184
IO	185
GND	186
VCCINT	187
IO	188
IO	189
IO	190
VCCO	191
IO	192
IO	193
IO_VREF_1	194
IO	195
IO	196
IO	197
IO	198

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
GCK2	199
GND	200
VCCO	201
GCK3	202
VCCINT	203
IO	204
IO	205
IO	206
IO_VREF_0	207
IO	208
IO	209
VCCO	210
IO	211
IO	212
IO	213
VCCINT	214
GND	215
IO	216
IO_VREF_0	217
IO	218
IO	219
IO_VREF_0	220
GND	221
IO	222
IO	223
IO_VREF_0	224
IO	225
IO	226
TCK	227
VCCO	228
GND	1, 8, 14, 27, 42, 48, 56, 66, 72, 86, 100, 106, 113, 123, 129, 143, 157, 163, 173, 180, 186, 200, 215, 221
VCCINT	15, 30, 41, 73, 83, 99, 130, 140, 156, 187, 203, 214
VCCO	18, 28, 37, 58, 76, 85, 95, 115, 133, 142, 152, 171, 191, 201, 210, 228

Pinout Diagrams

The following diagrams illustrate the locations of special-purpose pins on Virtex FPGAs. Table 6 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

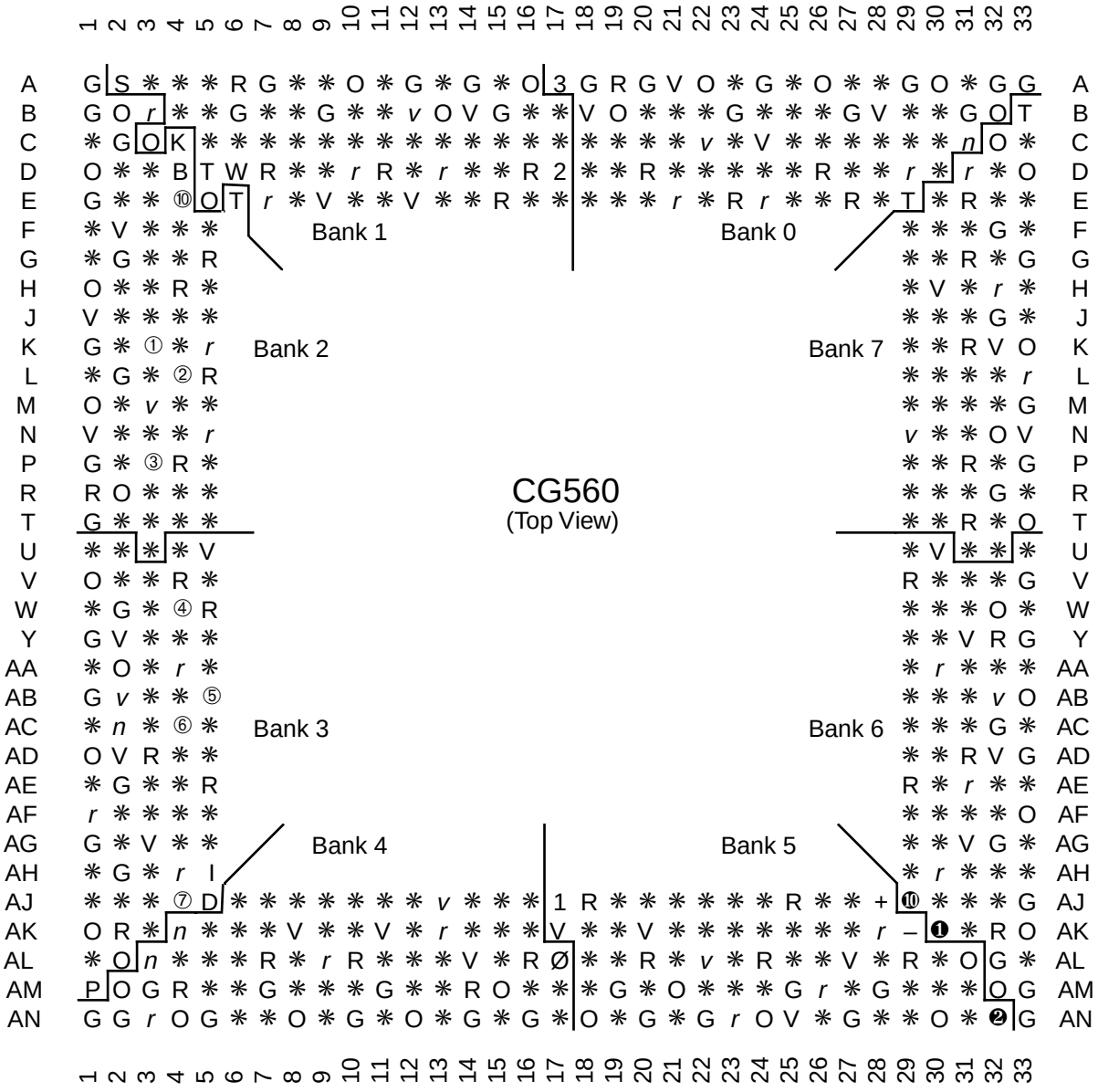
Table 6: **Pinout Diagram Symbols**

Symbol	Pin Function
S	General I/O
d	Device-dependent general I/O, n/c on smaller devices
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks

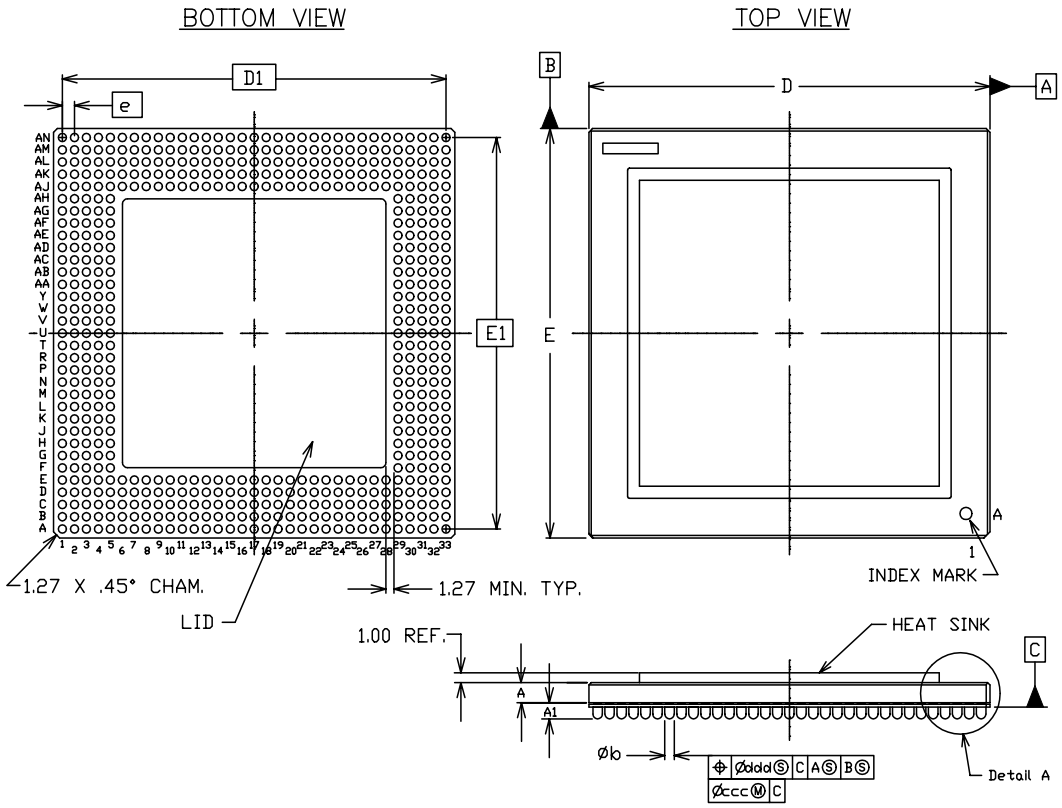
Table 6: **Pinout Diagram Symbols**

Symbol	Pin Function
⓾, ❶, ❷	M0, M1, M2
⓾, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan test aAccess port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

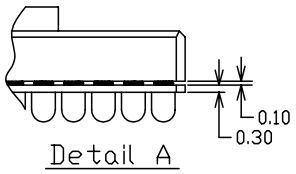
CG560 Pin Function Diagram



Package Drawing CG560 Ceramic Column Grid



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.80	2.00	2.20	
A_1	1.55	1.62	1.70	
D/E	42.10	42.50	42.90	
D_1/E_1	40.64 REF.			
e	1.27 BSC			
Øb	0.79	0.89	0.99	
ccc	—	—	0.15	
ddd	—	—	0.30	
M	33			2



NOTES:

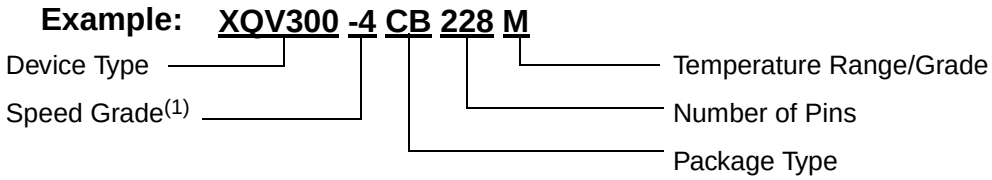
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. LEAD FINISH: HIGH TEMP. SOLDER Pb(90%)/Sn(10%)

CG560 Ceramic Column Grid Package

Device/Package Combinations and Maximum I/O

Package	Maximum User I/O (Excluding dedicated clock pins.)			
	XQV100	XQV300	XQV600	XQV1000
PQ240	166	166	-	-
HQ240	-	-	166	-
BG256	180	-	-	-
BG352	-	-	-	-
BG432	-	316	316	-
BG560	-	-	-	404
CB228	162	162	162	-
CG560	-	-	-	404

Ordering Information



Device Ordering Options

Device Type
XQV100
XQV300
XQV600
XQV1000

Package	
PQ240	240-pin Plastic Quad Flat Package
HQ240	240-pin High Heat Dissipation QFP Package
BG256	256-ball Plastic BGA Package
BG352	352-ball Plastic BGA Package
BG432	432-ball Plastic BGA Package
BG560	560-ball Plastic BGA Package
CB228	228-pin Ceramic Quad Flat Package
CG560	560-column Ceramic Column Grid Package

Grade		Temperature
M	Military Ceramic	T_C = –55°C to +125°C
N	Military Plastic	T_J = –55°C to +125°C
Q	MIL-PRF-38535(2)	T_C = –55°C to +125°C

Notes:
1. -4 only supported speed grade.
2. Class Q must be ordered with SMD number.

Valid Ordering Combinations

M Grade
XQV100-4CB228M
XQV300-4CB228M
XQV600-4CB228M
XQV1000-4CG560M

N Grade	
XQV100-4PQ240N	XQV300-4BG432N
XQV100-4BG256N	XQV600-4HQ240N
XQV300-4PQ240N	XQV600-4BG432N
XQV300-4BG352N	XQV1000-4BG560N