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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-LQFP
Supplier Device Package	36-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87fbh08au-eb-nh

■Minimum Instruction Cycle Time
- 250ns (12MHz at V_{DD}=2.7V to 5.5V, Ta=–40°C to +85°C)
- 300ns (10MHz at V_{DD}=2.2V to 5.5V, Ta=–40°C to +85°C)
- 750ns (4MHz at V_{DD}=1.8V to 5.5V, Ta=–40°C to +85°C)

■Ports
- Normal withstand voltage I/O ports
  Ports I/O direction can be designated in 1-bit units — 17 (P1n, P20, P21, P30, P31, P70 to P73 CF2/XT2)
  Ports I/O direction can be designated in 4-bit units — 8 (P0n)
- Dedicated oscillator ports/input ports — 1 (CF1/XT1)
- Reset pin — 1 ($\overline{RES}$)
- Power pins — 3 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$)

■Timers
- Timer 0: 16-bit timer/counter with a capture register.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■High-speed Clock Counter
- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- Can generate output real time.

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle =4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)

- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART1
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD converter: 12 bits/8 bits × 11 channels
- Successive approximation
- 12 bits/8 bits AD converter resolution selectable
- Port input: 10 channels, Reference voltage input: 1 channel

■PWM: Multifrequency 12-bit PWM × 2 channels

■Reference voltage generator circuit (VREF17)
- Capable of monitoring the power supply voltage by AD conversion of frequency variable RC oscillator circuit's reference voltage.

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Clock Output Function
- Capable generating clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Capable of generating the source clock for the subclock.

■Watchdog Timer
- Capable of generating an internal reset on an overflow of a timer running on the low-speed RC oscillator clock or subclock.
- Operating mode at standby is selectable from 3 modes (continue counting/stop operation/stop counting with a count value held).

■Interrupts
- 20 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/ PWM4, PWM5
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- Internal oscillation circuits

  Low-speed RC oscillation circuit (SRC): For system clock / For Watchdog timer (100kHz)
  Medium-speed RC oscillation circuit (RC): For system clock (1MHz)
  Frequency variable RC oscillation circuit (MRC): For system clock (8MHz ± 1.5%, Ta=–10°C to +85°C)
- External oscillation circuits

  Hi-speed CF oscillation circuit (CF): For system clock, with internal Rf
  Low speed crystal oscillation circuit (X'tal): For low-speed system clock / For Watchdog timer, with internal Rf

  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) Both the CF and crystal oscillator circuits stop operation on a system reset. After reset is released, oscillation is stopped so start the oscillation operation by program.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■Internal Reset Function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use or disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V) can be selected by optional configuration.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are four ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by low-voltage detection
     (3) System resetting by watchdog timer
     (4) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, low-/medium-/ Frequency variable RC, and crystal oscillators automatically stop operation.
     Note: The oscillation of the low-speed RC oscillator is also controlled directly by the watchdog timer and its standby-mode-time oscillation is also controlled.
  2) There are five ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by low-voltage detection
     (3) System resetting by watchdog timer
     (4) Having an interrupt source established at either INT0, INT1, INT2, INT4, INT5
        * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (5) Having an interrupt source established at port 0.

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- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF, low-/medium-/ Frequency variable RC oscillators automatically stop operation.
     Note: The oscillation of the low-speed RC oscillator is also controlled directly by the watchdog timer and its standby-mode-time oscillation is also controlled.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) System resetting by watchdog timer or low-voltage detection.
     (4) Having an interrupt source established at either INT0, INT1, INT2, INT4, INT5
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (5) Having an interrupt source established at port 0.
     (6) Having an interrupt source established in the base timer circuit.
         Note: Available only when X'tal oscillation is selected.

■Onchip Debugger (flash versions only)

- Supports software debugging with the microcontroller mounted on the target board.
- Software break setting
- Stepwise execution of instructions
- Real time RAM data monitoring function
  All the RAM data map contents can be monitored and rewritten on the screen when the program is running.
  (Part of the SFR data cannot be rewritten.)
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
  DBGP0 (P0), DBGP1 (P1)

■Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Package Form

- QFP36(7mm×7mm) : Pb-Free and Halogen Free type
- VQLP32(4mm×4mm) : Pb-Free and Halogen Free type (Build-to-order)

■Development Tools

- On-chip-debugger : (1) TCB87 TypeB + LC87FBH08A
  (2) TCB87 TypeC (3 wire version) + LC87FBH08A

■Flash ROM Programming Boards

Package	Programming boards
QFP36 (7mm×7mm)	W87F24Q
VQLP32 (4mm×4mm)	(build-to-order)

■Flash ROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 03.28 or later	87F008SU
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Flash Support Group, Inc. (FSG) + ON Semiconductor (Note 1)	In-circuit Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	-
		SIB87(Inter Face Driver) (ON Semiconductor model)		
ON Semiconductor	Single/Gang Programmer	SKK / SKK Type B / SKK Type C (SanyoFWS)	Application Version 1.07 or later Chip Data Version 2.38 or later	LC87FBH08
	In-circuit/Gang Programmer	SKK-DBG Type B / SKK-DBG Type C (SanyoFWS)		

For information about AF-Series:

Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

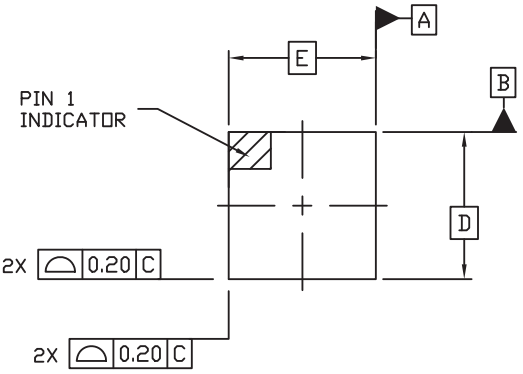
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

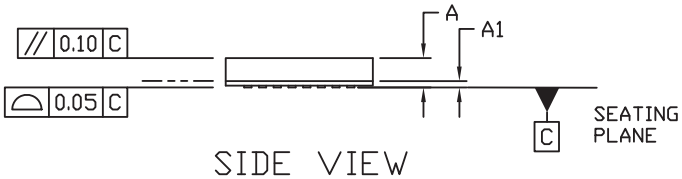
Package Dimensions

unit : mm
[Build to order]

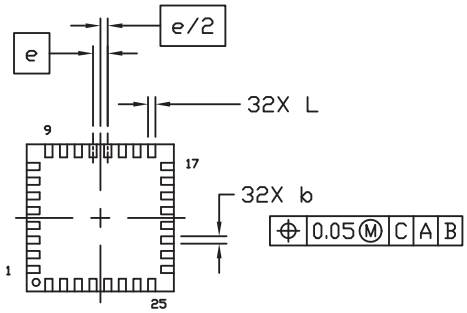
VQLP32 4x4
CASE 602AE
ISSUE A



TOP VIEW



SIDE VIEW

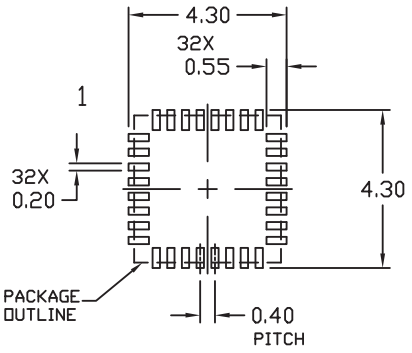


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS

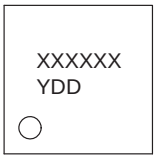
DIM	MILLIMETERS	
	MIN.	MAX.
A	---	0.85
A1	---	0.05
b	0.15	0.25
D	4.00 BSC	
E	4.00 BSC	
e	0.40 BSC	
L	0.30	0.40



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*

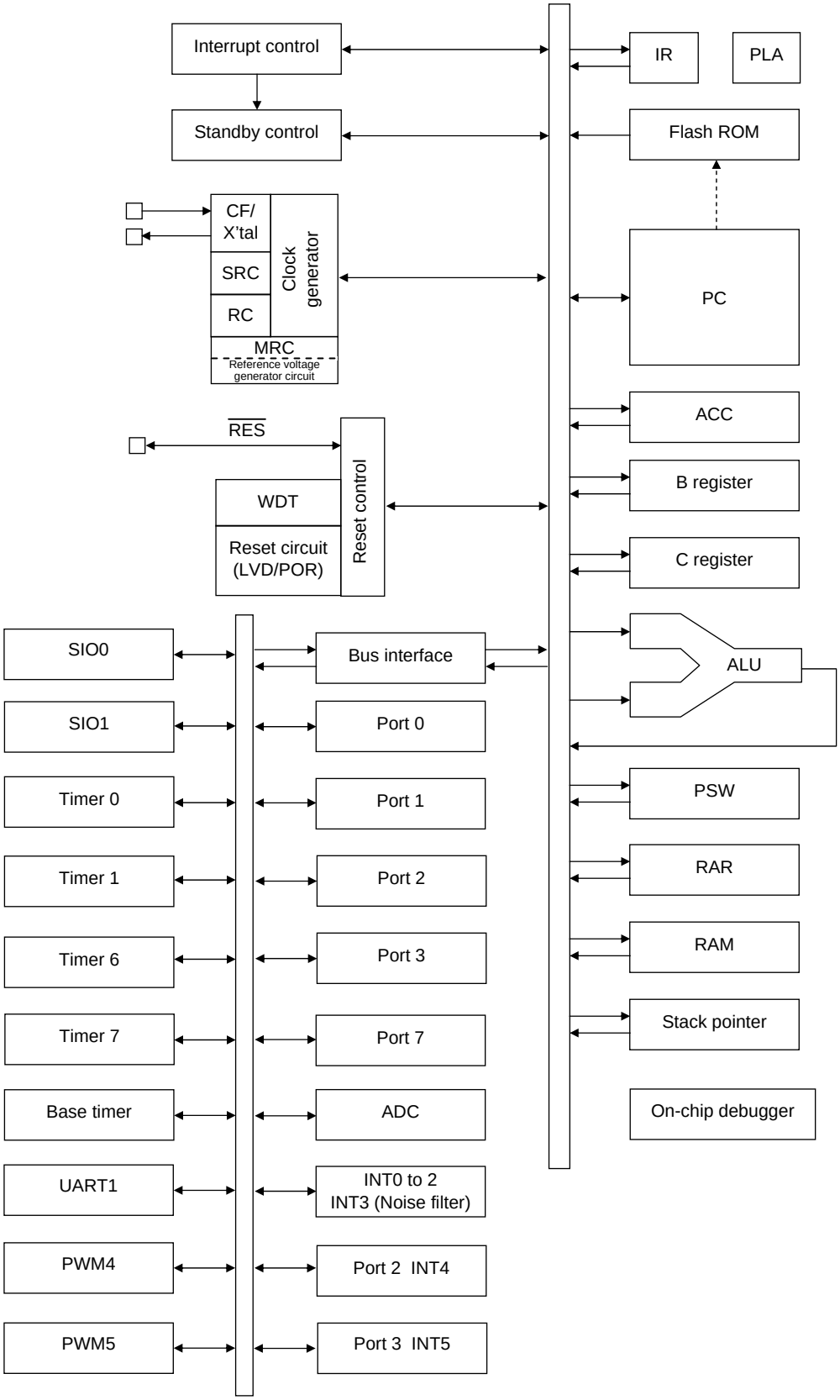
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

System Block Diagram



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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P70: INT0 input / HOLD reset input / timer 0L capture input
P71: INT1 input / HOLD reset input / timer 0H capture input
P72: INT2 input / HOLD reset input / timer 0 event input / timer 0L capture input
P73: INT3 input (with noise filter) / timer 0 event input / timer 0H capture input
P70(AN8) to P72(AN10): AD converter input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input / internal reset output</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic resonator or 32.768kHz crystal oscillator input pin
• Pin function
General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic resonator or 32.768kHz crystal oscillator output pin
• Pin function
General-purpose I/O port</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
CF2/XT2	-	No	Ceramic resonator/32.768kHz crystal resonator output Nch-open drain (N-channel open drain when set to general-purpose output port)	No

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$			−0.3		+6.5	V
Input voltage		V_I	CF1			−0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}	Ports 0, 1, 2, 3, Port 7, CF2, $\overline{RES}$			−0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		−10			mA
		IOPH(2)	P71 to P73	Per 1 applicable pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		−7.5			
		IOMH(2)	P71 to P73	Per 1 applicable pin		−3			
	Total output current	ΣIOAH(1)	Ports 0, 1, 2, 3, P71 to P73	Total of all applicable pins		−25			
Low level output current	Peak output current	IOPL(1)	P02 to P07, Ports 1, 2, 3	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Port 7, CF2	Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Port 7, CF2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 1, Ports 2, 3, CF2	Total of all applicable pins				70	
		ΣIOAL(2)	Port 7	Total of all applicable pins				15	
Power dissipation		Pd max(1)	QFP36(7×7)	Ta=−40 to +85°C Package only				120	mW
		Pd max(2)		Ta=−40 to +85°C Package with thermal resistance board (Note 1-2)				275	
Operating ambient temperature		Topr				−40		+85	°C
Storage ambient temperature		Tstg				−55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Conditions at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1$	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	V
	$V_{DD}(2)$		0.294μs ≤ tCYC ≤ 200μs		2.2		5.5	
	$V_{DD}(3)$		0.735μs ≤ tCYC ≤ 200μs		1.8		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3, 7		1.8 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Ports 0		1.8 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(3)$	CF1, CF2, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3, 7		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	CF1, CF2, $\overline{RES}$		1.8 to 5.5	V_{SS}		$0.25V_{DD}$	
High level output current	$I_{OH}(1)$	Ports 0, 1, 2, P71 to P73	Per 1 applicable pin	4.5 to 5.5	–1.0			mA
	$I_{OH}(2)$			2.7 to 4.5	–0.35			
	$I_{OH}(3)$			1.8 to 2.7	–0.15			
	$I_{OH}(4)$	Ports 3, P05 (System clock output function used)	Per 1 applicable pin	4.5 to 5.5	–6.0			
	$I_{OH}(5)$			2.7 to 4.5	–1.4			
	$I_{OH}(6)$			1.8 to 2.7	–0.8			
	$\Sigma I_{OH}(1)$	Ports 0, 1, 2, 3, 7	Total of all applicable pins	4.5 to 5.5	–25			
	$\Sigma I_{OH}(2)$			2.7 to 4.5	–11.2			
	$\Sigma I_{OH}(3)$			1.8 to 2.7	–5.4			
Low level output current	$I_{OL}(1)$	Ports 0, 1, 2, 3	Per 1 applicable pin	4.5 to 5.5			10	
	$I_{OL}(2)$			2.7 to 4.5			1.4	
	$I_{OL}(3)$			1.8 to 2.7			0.8	
	$I_{OL}(4)$	Port 7, CF2	Per 1 applicable pin	2.7 to 5.5			1.4	
	$I_{OL}(5)$			1.8 to 2.7			0.8	
	$I_{OL}(6)$	P00, P01	Per 1 applicable pin	4.5 to 5.5			25	
	$I_{OL}(7)$			2.7 to 4.5			4	
	$I_{OL}(8)$			1.8 to 2.7			2	
	$\Sigma I_{OL}(1)$	Ports 0, 1, 2, 3, CF2	Total of all applicable pins	4.5 to 5.5			70	
	$\Sigma I_{OL}(2)$			2.7 to 4.5			34.6	
	$\Sigma I_{OL}(3)$			1.8 to 2.7			19.2	
	$\Sigma I_{OL}(4)$	Ports 7	Total of all applicable pins	2.7 to 5.5			5.6	
	$\Sigma I_{OL}(5)$			1.8 to 2.7			3.2	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 5.5	0.245		200	μs
				2.2 to 5.5	0.294		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.7 to 5.5	0.1		12	MHz
				1.8 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio=1/2 • External system clock duty=50±5%	3.0 to 5.5	0.2		24.4	
				2.0 to 5.5	0.2		8	

Note 2-1: V_{DD} must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.
Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Continued on next page.

Electrical Characteristics at Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2, 3, Ports 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5			1	μA
	I_{IH}(2)	CF1, CF2	Input port selected $V_{IN}=V_{DD}$	1.8 to 5.5			1	
	IIH(3)	CF1	Reset state $V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	I_{IL}(1)	Ports 0, 1, 2, 3, Ports 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	−1			
	I_{IL}(2)	CF1, CF2	Input port selected $V_{IN}=V_{SS}$	1.8 to 5.5	−1			
High level output voltage	V_{OH}(1)	Ports 0, 1, 2 P71 to P73	I_{OH}=-1mA	4.5 to 5.5	V_{DD}−1			V
	V_{OH}(2)		I_{OH}=-0.35mA	2.7 to 5.5	V_{DD}−0.4			
	V_{OH}(3)		I_{OH}=-0.15mA	1.8 to 5.5	V_{DD}−0.4			
	V_{OH}(4)	Ports 3 P05 (System clock output function used)	I_{OH}=-6mA	4.5 to 5.5	V_{DD}−1			
	V_{OH}(5)		I_{OH}=-1.4mA	2.7 to 5.5	V_{DD}−0.4			
	V_{OH}(6)		I_{OH}=-0.8mA	1.8 to 5.5	V_{DD}−0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 2, 3	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}=1.4mA	2.7 to 5.5			0.4	
	V_{OL}(3)		I_{OL}=0.8mA	1.8 to 5.5			0.4	
	V_{OL}(4)	Port 7, CF2	I_{OL}=1.4mA	2.7 to 5.5			0.4	
	V_{OL}(5)		I_{OL}=0.8mA	1.8 to 5.5			0.4	
	V_{OL}(6)	P00, P01	I_{OL}=25mA	4.5 to 5.5			1.5	
	V_{OL}(7)		I_{OL}=4mA	2.7 to 5.5			0.4	
	V_{OL}(8)		I_{OL}=2mA	1.8 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3, Ports 7	$V_{OH}=0.9V_{DD}$ When Port 0 selected low-impedance pull-up.	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			1.8 to 4.5	18	50	230	
	Rpu(3)	Port 0	$V_{OH}=0.9V_{DD}$ When Port 0 selected high-impedance pull-up.	1.8 to 5.5	100	200	400	
Hysteresis voltage	VHYS(1)	Ports 1, 2, 3, Ports 7, $\overline{RES}$		2.7 to 5.5		$0.1V_{DD}$		V
	VHYS(2)			1.8 to 2.7		$0.07V_{DD}$		
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	1.8 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SIO0 Serial I/O Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$ (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 5. (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 5.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-3)	1.8 to 5.5			(1/3)tCYC +0.08	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-3)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

Consumption Current Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 10-1) (Note 10-2)	IDDOP(1)	$V_{DD}1$	• FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		5.1	9.3	mA
				2.7 to 3.6		3.1	5.6	
	IDDOP(2)		• CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		5.2	10	
				3.0 to 3.6		3.3	6.2	
	IDDOP(3)		• FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		4.4	8.4	
				2.2 to 3.6		2.8	5.5	
	IDDOP(4)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		2.3	5.3	
				1.8 to 3.6		1.6	3.0	
	IDDOP(5)		• CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.2 to 5.5		0.97	2.4	
				2.2 to 3.6		0.55	1.2	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.44	1.5	
				1.8 to 3.6		0.28	0.80	
	IDDOP(7)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio	1.8 to 5.5		3.4	5.5	
				1.8 to 3.6		2.4	4.6	
	IDDOP(8)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		51	163	μA
				1.8 to 3.6		38	103	
	IDDOP(9)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C	5.0		51	136	
				3.3		38	99	
				2.5		36	94	

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 10-1) (Note 10-2)	IDDOP(10)	V_{DD}1	• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		34	97	μA
				1.8 to 3.6		14	44	
	IDDOP(11)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		34	88	
				3.3		14	36	
				2.5		9.1	22	
HALT mode consumption current (Note 10-1) (Note 10-2)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		2.6	4.8	mA
				2.7 to 3.6		1.4	2.4	
	IDDHALT(2)		• HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		2.7	5.3	
				3.0 to 3.6		1.6	2.9	
	IDDHALT(3)		• HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		2.2	4.3	
				2.2 to 3.6		1.2	2.2	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		1.3	3.3	
				1.8 to 3.6		0.56	1.2	
	IDDHALT(5)		• HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.2 to 5.5		0.74	1.8	
				2.2 to 3.6		0.34	0.68	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.32	0.90	
				1.8 to 3.6		0.21	0.44	

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
HALT mode consumption current (Note 10-1) (Note 10-2)	IDDHALT(7)	V_{DD}1	• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio	1.8 to 5.5		1.3	2.3	mA
				1.8 to 3.6		0.91	1.5	
	IDDHALT(8)		• HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		18	68	μA
				1.8 to 3.6		11	35	
	IDDHALT(9)		• HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C	5.0		18	46	
				3.3		11	27	
				2.5		7.4	19	
	IDDHALT(10)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		24	98	
				1.8 to 3.6		8.0	35	
	IDDHALT(11)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		24	63	
				3.3		8.0	23	
				2.5		3.5	11	
HOLD mode consumption current (Note 10-1) (Note 10-2)	IDDHOLD(1)		HOLD mode • CF1=V_{DD} or open (External clock mode)	1.8 to 5.5		0.019	23	
				1.8 to 3.6		0.011	11	
	IDDHOLD(2)		HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C	5.0		0.019	1.2	
				3.3		0.011	0.59	
				2.5		0.010	0.30	
	IDDHOLD(3)		HOLD mode • CF1=V_{DD} or open (External clock mode) • LVD option selected	1.8 to 5.5		2.6	26	
				1.8 to 3.6		2.0	13	
	IDDHOLD(4)		HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C • LVD option selected	5.0		2.6	3.8	
				3.3		2.0	2.8	
				2.5		1.7	2.5	
Timer HOLD mode consumption current (Note 10-1) (Note 10-2)	IDDHOLD(5)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	1.8 to 5.5		22	84	
				1.8 to 3.6		6.5	30	
	IDDHOLD(6)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode • Ta=-10 to +50°C	5.0		22	53	
				3.3		6.5	16	
				2.5		2.7	7.2	

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2: The consumption current values do not include operational current of LVD function if not specified.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

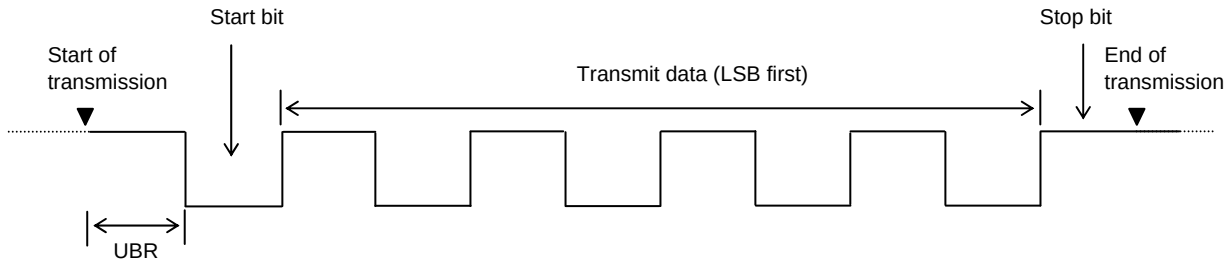
Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Only current of the Flash block.	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	μs

UART (Full Duplex) Operating Conditions at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

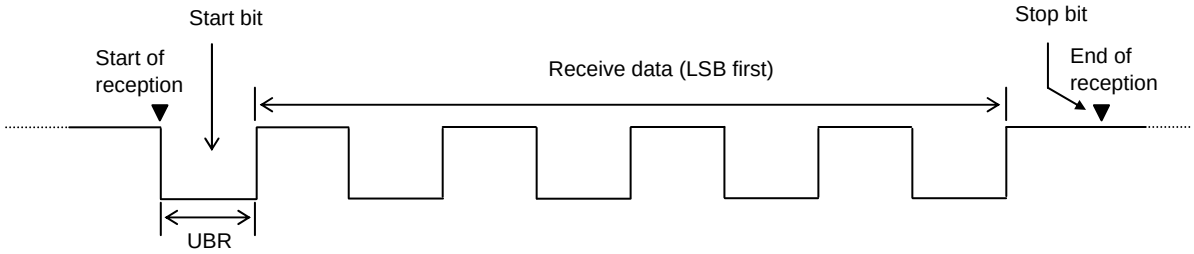
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	P20, P21		1.8 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

- CF oscillation normal amplifier size selected (CFLAMP=0)

■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	680	2.6 to 5.5	0.02	0.3	Internal C1, C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.1 to 5.5	0.02	0.3	
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	680	2.4 to 5.5	0.02	0.3	
		CSTLS10M0G53095-B0	(15)	(15)	Open	680	2.0 to 5.5	0.01	0.15	
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1k	2.1 to 5.5	0.02	0.3	
	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.2 to 5.5	0.02	0.3	
		CSTLS8M00G53095-B0	(15)	(15)	Open	1k	1.9 to 5.5	0.01	0.15	
6MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	1.5k	2.0 to 5.5	0.02	0.3	
		CSTCR6M00G53093-R0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.01	0.15	
	LEAD	CSTLS6M00G53-B0	(15)	(15)	Open	1.5k	2.0 to 5.5	0.02	0.3	
		CSTLS6M00G53095-B0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.01	0.15	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.03	0.45	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.02	0.3	

- CF oscillation low amplifier size selected (CFLAMP=1)

■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	470	3.9 to 5.5	0.03	0.45	Internal C1, C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	470	2.9 to 5.5	0.03	0.45	
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	470	3.6 to 5.5	0.03	0.45	
		CSTLS10M0G53095-B0	(15)	(15)	Open	470	2.7 to 5.5	0.02	0.3	
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	680	2.7 to 5.5	0.03	0.45	
	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	680	3.0 to 5.5	0.03	0.45	
		CSTLS8M00G53095-B0	(15)	(15)	Open	680	2.5 to 5.5	0.01	0.15	
6MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	1k	2.6 to 5.5	0.03	0.45	
		CSTCR6M00G53095-R0	(15)	(15)	Open	1k	2.2 to 5.5	0.02	0.3	
	LEAD	CSTLS6M00G53-B0	(15)	(15)	Open	1k	2.7 to 5.5	0.03	0.45	
		CSTLS6M00G53095-B0	(15)	(15)	Open	1k	2.2 to 5.5	0.01	0.15	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1k	2.1 to 5.5	0.04	0.6	
		CSTCR4M00G53095-R0	(15)	(15)	Open	1k	1.8 to 5.5	0.02	0.3	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1k	2.1 to 5.5	0.02	0.3	
		CSTLS4M00G53095-B0	(15)	(15)	Open	1k	1.8 to 5.5	0.01	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in follwing cases (see Figure 3).

- The time interval that is required for the oscillation to get stabilized after the instruction for starting the mainclock oscillation circuit is executed.
- The time interval that is required for the oscillation to get stabilized after the HOLD mode is reset and oscillation is started.
- The time interval that is required for the oscillation to get stabilized after the X'tal Hold mode, under the state which the main clock oscillation is enabled, is reset and oscillation is started.

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	MC-306	9	9	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value = 7.0pF

■SEIKO INSTRUMENTS

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	SSP-T7-F	18	22	Open	330k	1.8 to 5.5	0.75	2.0	Applicable CL value = 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 3).

- The time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed.
- The time interval that is required for the oscillation to get stabilized after the Hold mode, under the state which the subclock oscillation is enabled, is reset and oscillation is started.

(Notes on the implementation of the oscillator circuit)

- Oscillation is influenced by the circuit pattern layout of printed circuit board. Place the oscillation-related components as close to the CPU chip and to each other as possible with the shortest possible pattern length.
- Keep the signal lines whose state changes suddenly or in which large current flows as far away from the oscillator circuit as possible and make sure that they do not cross one another.
- Be sure to insert a current limiting resistor (Rd) so that the oscillation amplitude never exceeds the input voltage level that is specified as the absolute maximum rating.
- The oscillator circuit constants shown above are sample characteristic values that are measured using the Our designated oscillation evaluation board. Since the accuracy of the oscillation frequency and other characteristics vary according to the board on which the IC is installed, it is recommended that the user consult the resonator vendor for oscillation evaluation of the IC on a user's production board when using the IC for applications that require high oscillation accuracy. For further information, contact your resonator vendor or Our company sales representative serving your locality.
- It must be noted, when replacing the flash ROM version of a microcontroller with a mask ROM version, that their operating voltage ranges may differ even when the oscillation constant of the external oscillator is the same.

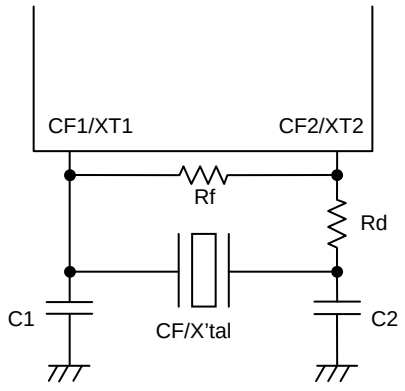


Figure 1 CF and XT Oscillator Circuit

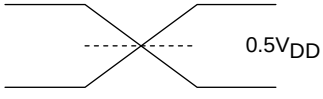
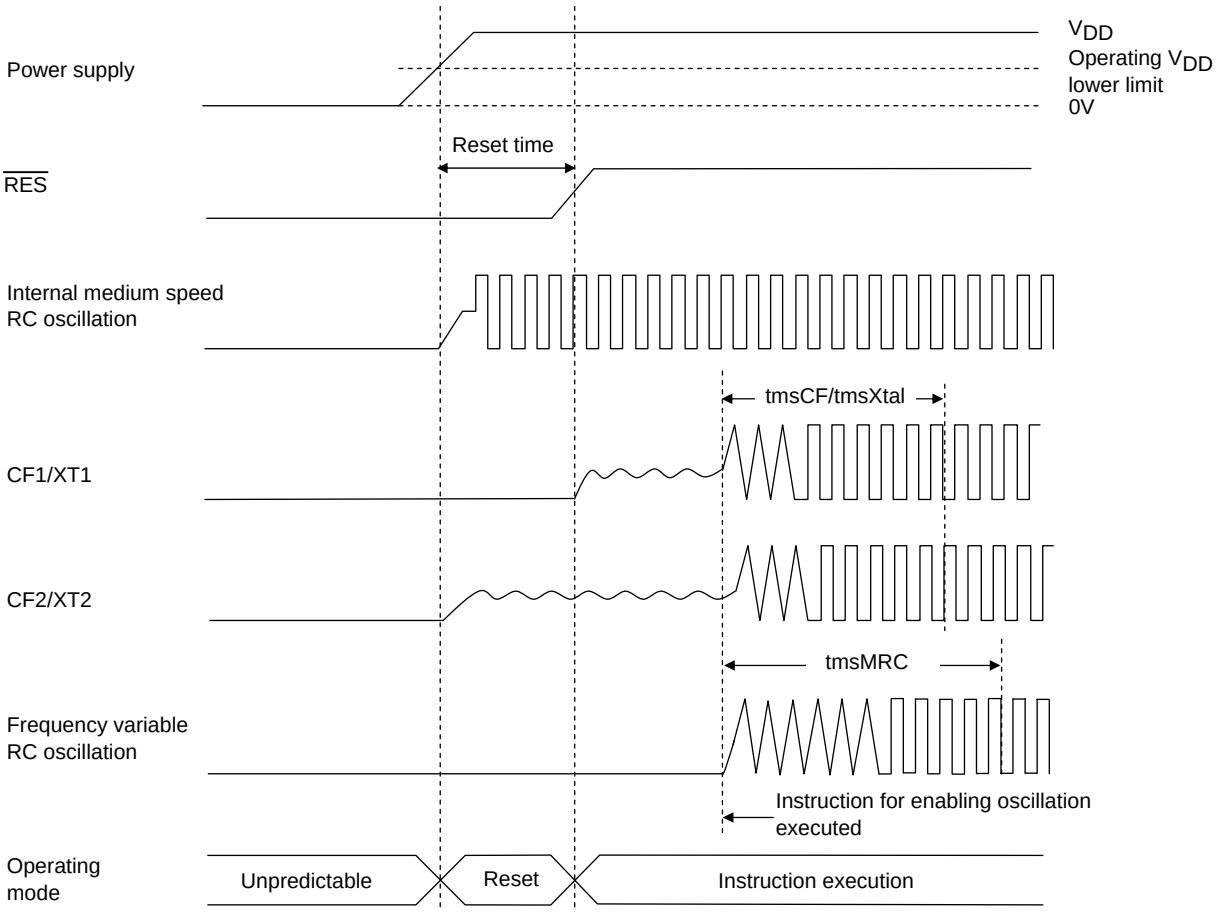
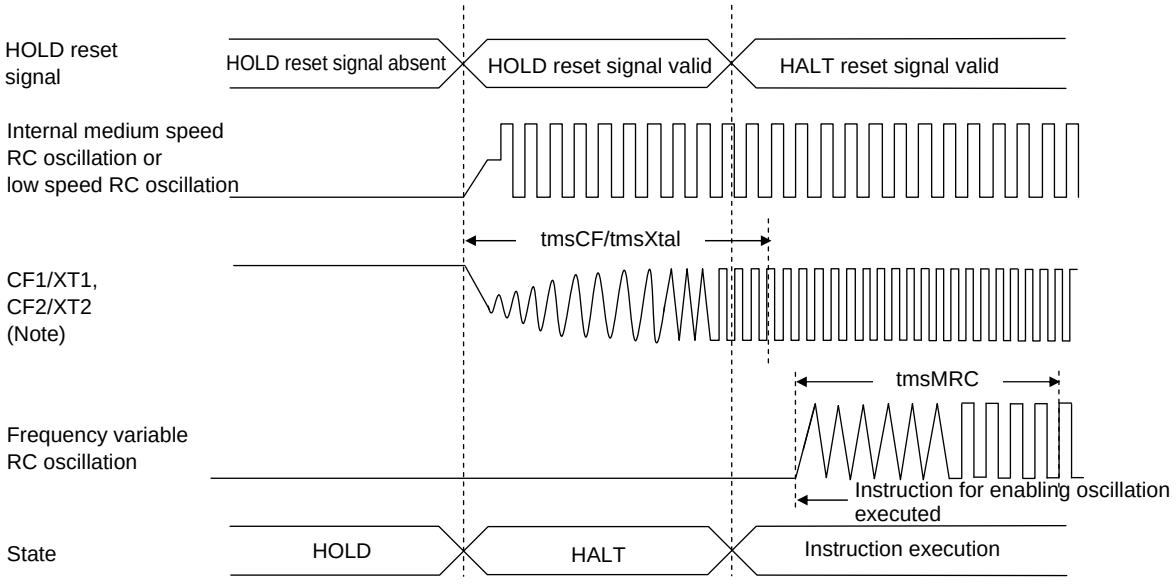


Figure 2 AC Timing Measurement Point



Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times

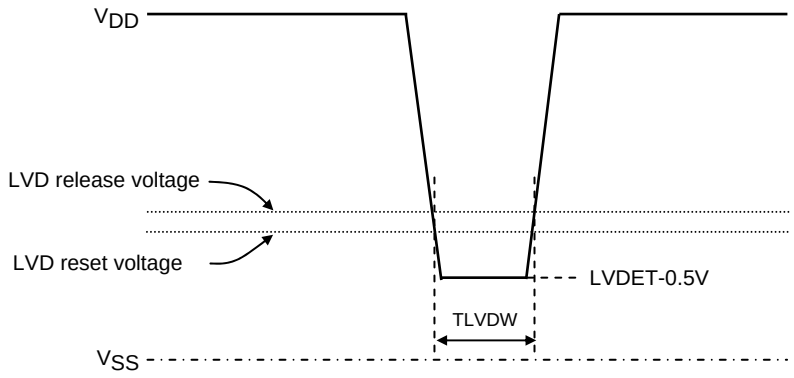


Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87FBH08AU-EB-3H	LQFP36 7x7 / QFP36 (Pb-Free / Halogen Free)	500 / Tray Foam
LC87FBH08AU-EB-NH	LQFP36 7x7 / QFP36 (Pb-Free / Halogen Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF