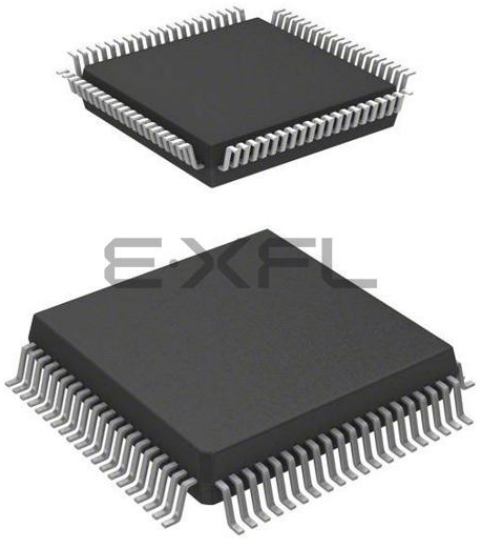

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	42
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7046f50v

Instruction		Instruction Code	Operation	Execution States	T Bit
MOV.L	Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B	@(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W	@(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L	@(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B	R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W	R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L	R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B	@(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W	@(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L	@(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA	@(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT	Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B	Rm,Rn	0110nnnnmmmm1000	Rm → Swap bottom two bytes → Rn	1	—
SWAP.W	Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT	Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

Electromagnetic waves are radiated from an LSI in operation. This LSI has an electromagnetic peak in the harmonics band whose primary frequency is determined by the lower frequency between the system clock (ϕ) and peripheral clock ($P\phi$). For example, when ϕ = 50 MHz and $P\phi$ = 40 MHz, the primary frequency is 40 MHz. If this LSI is used adjacent to a device sensitive to electromagnetic interference, e.g. FM/VHF band receiver, a printed circuit board of more than four layers with planes exclusively for system ground is recommended.

6.8.3 Handling Interrupt Request Signals as Source for CPU Interrupt but Not DTC Activating

1. For DTC, clear the corresponding DTE bits to 0.
2. When interrupts occur, interrupt requests are sent to the CPU.
3. The CPU clears the interrupt source and performs the necessary processing in the interrupt processing routine.

9.4 Register Descriptions

9.4.1 Bus Control Register 1 (BCR1)

BCR1 is a 16-bit readable/writable register that enables access to the MMT and MTU control registers.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0 and should always be written with 0.
14	MMTRWE	1	R/W	MMT Read/Write Enable This bit enables MMT control register access. For details, refer to MMT section. 0: MMT control register access is disabled 1: MMT control register access is enabled
13	MTURWE	1	R/W	MTU Read/Write Enable This bit enables MTU control register access. For details, refer to MTU section. 0: MTU control register access is disabled 1: MTU control register access is enabled
12 to 8	—	All 0	R	Reserved These bits are always read as 0 and should always be written with 0.
7 to 4	—	All 0	R	Reserved These bits are always read as 0 and should always be written with 0.
3 to 0	—	All 1	R	Reserved These bits are always read as 1 and should always be written with 1.

9.4.2 RAM Emulation Register (RAMER)

The RAM emulation register (RAMER) is a 16-bit readable/writable register that selects the RAM area to be used when emulating realtime programming of flash memory. For details, refer to section 18.5.5, RAM Emulation Register.

9.5 Bus Arbitration

This LSI has a bus arbitration function that, when a bus release request is received from a bus masters, releases the bus to that module. There are two internal bus masters, the CPU and DTC. The priority for arbitrate the bus mastership between these bus masters is:

DTC > CPU

9.6 On-chip Peripheral I/O Register Access

On-chip peripheral I/O registers are accessed from the bus state controller, as shown in Table 9.2.

Table 9.2 On-chip Peripheral I/O Register Access

On-chip Peripheral Module	SCI	MTU, POE	INTC	PFC, PORT	CMT	A/D	UBC	WDT	DTC	MMT
Connected bus width	8bit	16bit	16bit	16bit	16bit	16bit	16bit	16bit	16bit	16bit
Access cycle	2cyc*1	2cyc*1	2cyc*2	2cyc*1	2cyc*1	2cyc*1	3cyc*2	3cyc*2	3cyc*2	2cyc*1

Notes: 1. Converted to the peripheral clock.
2. Converted to the system clock.

10.3.1 Timer Control Register (TCR)

The TCR registers are 8-bit readable/writable registers that control the TCNT operation for each channel. The MTU has a total of five TCR registers, one for each channel (channel 0 to 4). TCR register settings should be conducted only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 0 to 2
6	CCLR1	0	R/W	These bits select the TCNT counter clearing source. See tables 10.3 and 10.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 0 and 1
3	CKEG0	0	R/W	These bits select the input clock edge. When the input clock is counted using both edges, the input clock period is halved (e.g. Pϕ/4 both edges = Pϕ/2 rising edge). If phase counting mode is used on channels 1 and 2, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is Pϕ/4 or slower. When Pϕ/1, or the overflow/underflow of another channel is selected for the input clock, although values can be written, counter operation compiles with the initial value. 00: Count at rising edge 01: Count at falling edge 1X: Count at both edges Legend: X: Don't care
2	TPSC2	0	R/W	Time Prescaler 0 to 2
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 10.5 to 10.8 for details.
0	TPSC0	0	R/W	

Table 10.9 MD0 to MD3

Bit 3 MD3	Bit 2 MD2	Bit 1 MD1	Bit 0 MD0	Description
0	0	0	0	Normal operation
			1	Reserved (do not set)
		1	0	PWM mode 1
			1	PWM mode 2*1
	1	0	0	Phase counting mode 1*2
			1	Phase counting mode 2*2
		1	0	Phase counting mode 3*2
			1	Phase counting mode 4*2
1	0	0	0	Reset synchronous PWM mode*3
			1	Reserved (do not set)
		1	X	Reserved (do not set)
	1	0	0	Reserved (do not set)
			1	Complementary PWM mode 1 (transmit at peak)*3
		1	0	Complementary PWM mode 2 (transmit at bottom)*3
			1	Complementary PWM mode 2 (transmit at peak and bottom)*3

Legend:

X: Don't care

Notes: 1. PWM mode 2 can not be set for channels 3, 4.

2. Phase counting mode can not be set for channels 0, 3, 4.

3. Reset synchronous PWM mode, complementary PWM mode can only be set for channel 3. When channel 3 is set to reset synchronous PWM mode or complementary PWM mode, the channel 4 settings become ineffective and automatically conform to the channel 3 settings. However, do not set channel 4 to reset synchronous PWM mode or complementary PWM mode. Reset synchronous PWM mode and complementary PWM mode can not be set for channels 0, 1, 2.

Table 10.14 TIOR_1 (channel 1)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_1 Function**	**TIOC1B Pin Function**
0	0	0	0	Output compare register	Output hold*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output hold
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges
	1	X	X		Input capture at generation of TGRC_0 compare match/input capture

Legend:

X: Don't care

Note: * The low level output is retained until TIOR contents is specified after a power-on reset.

Table 10.23 TIORH_4 (channel 4)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function**	**TIOC4A Pin Function**
0	0	0	0	Output compare register	Output hold*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output hold
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

Legend:

X: Don't care

Note: * The low level output is retained until TIOR contents is specified after a power-on reset.

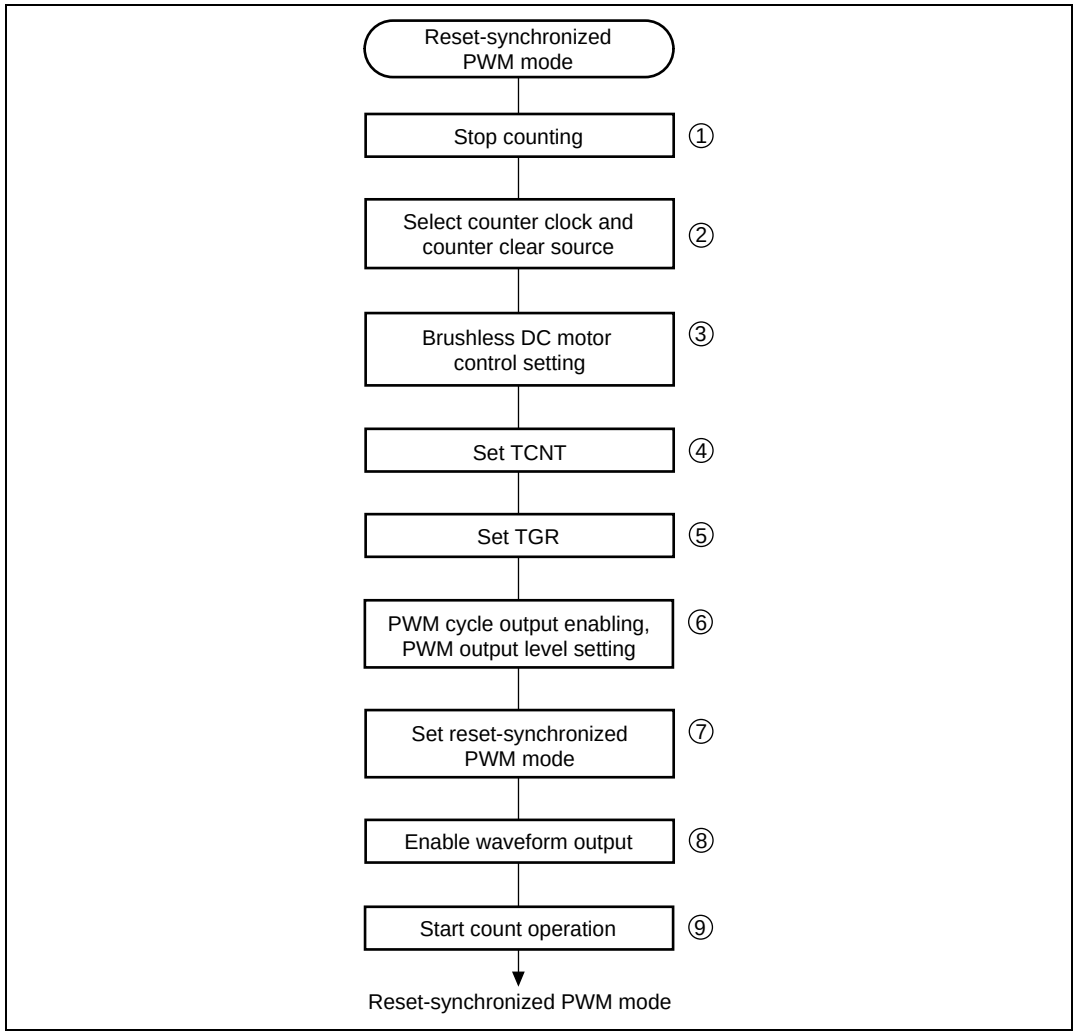

Figure 10.30 Procedure for Selecting the Reset-Synchronized PWM Mode

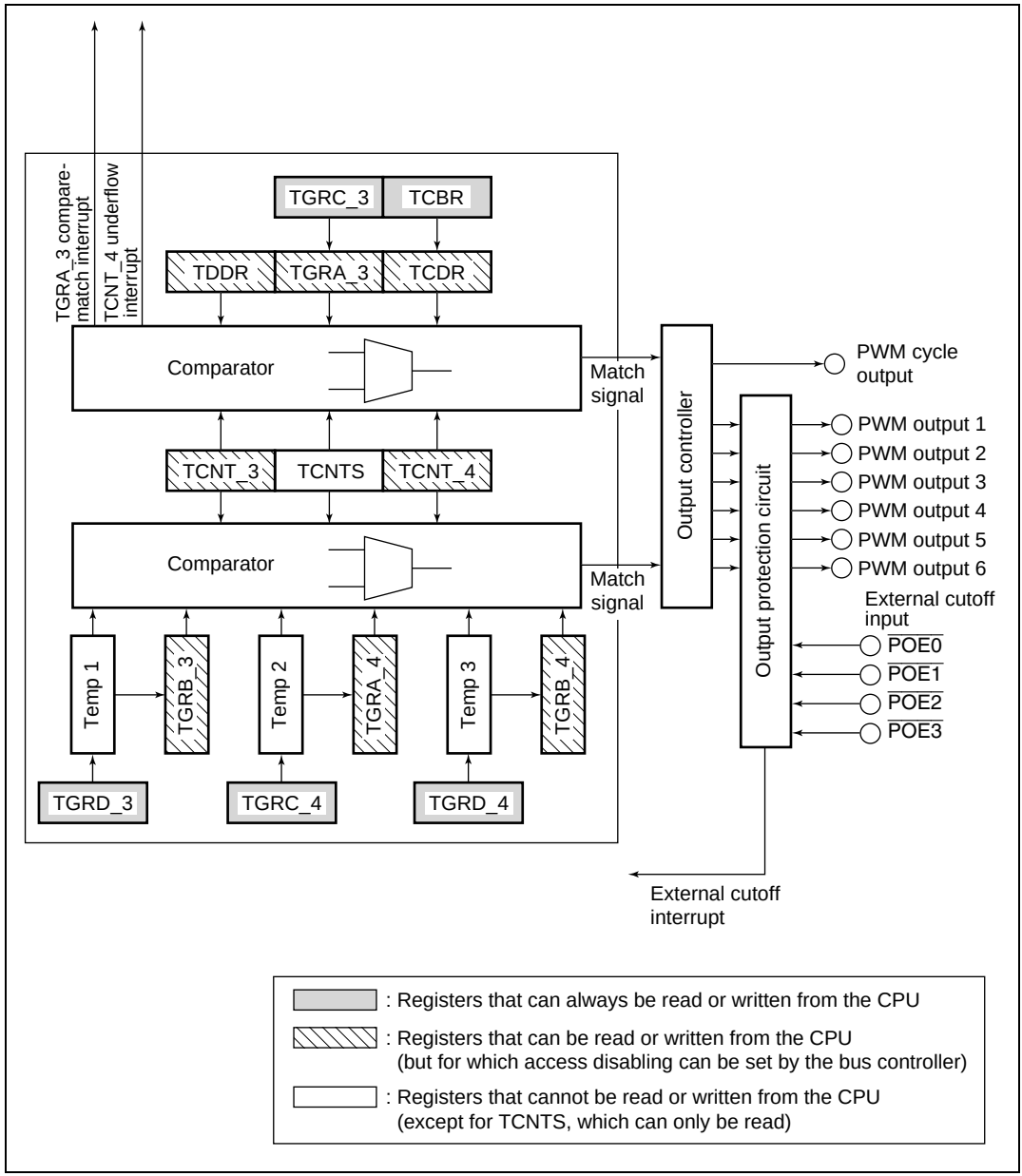

Figure 10.32 Block Diagram of Channels 3 and 4 in Complementary PWM Mode

Register Data Updating: In complementary PWM mode, the buffer register is used to update the data in a compare register. The update data can be written to the buffer register at any time. There are five PWM duty and carrier cycle registers that have buffer registers and can be updated during operation.

There is a temporary register between each of these registers and its buffer register. When subcounter TCNTS is not counting, if buffer register data is updated, the temporary register value is also rewritten. Transfer is not performed from buffer registers to temporary registers when TCNTS is counting; in this case, the value written to a buffer register is transferred after TCNTS halts.

The temporary register value is transferred to the compare register at the data update timing set with bits MD3–MD0 in the timer mode register (TMDR). Figure 10.37 shows an example of data updating in complementary PWM mode. This example shows the mode in which data updating is performed at both the counter crest and trough.

When rewriting buffer register data, a write to TGRD_4 must be performed at the end of the update. Data transfer from the buffer registers to the temporary registers is performed simultaneously for all five registers after the write to TGRD_4.

A write to TGRD_4 must be performed after writing data to the registers to be updated, even when not updating all five registers, or when updating the TGRD_4 data. In this case, the data written to TGRD_4 should be the same as the data prior to the write operation.

Section 12 Serial Communication Interface (SCI)

This LSI has two independent serial communication interface (SCI) channels. The SCI can handle both asynchronous and clocked synchronous serial communication. In asynchronous serial communication mode, serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function).

12.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected

  External clock can be selected as a transfer clock source.
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

  Four interrupt sources — transmit-end, transmit-data-empty, receive-data-full, and receive error — that can issue requests.

  The transmit-data-empty interrupt and receive data full interrupts can activate the data transfer controller (DTC).
- Module standby mode can be set

Asynchronous mode

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Multiprocessor bit: 1 or 0
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RxD pin level directly in case of a framing error

Table 13.3 A/D Conversion Time (Single Mode)

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A/D conversion start delay time	t_D	31	—	62	15	—	30	7	—	14	3	—	6
Input sampling time	t_{SPL}	—	256	—	—	128	—	—	64	—	—	32	—
A/D conversion time	t_{CONV}	1024	—	1055	515	—	530	259	—	266	131	—	134

Note: All values represent the number of states for Pϕ.

Table 13.4 A/D Conversion Time (Scan Mode)

CKS1	CKS0	Conversion Time (State)
0	0	1024 (Fixed)
	1	512 (Fixed)
1	0	256 (Fixed)
	1	128 (Fixed)

13.4.5 A/D Converter Activation by MTU or MMT

The A/D converter can be independently activated by an A/D conversion request from the interval timer of the MTU or MMT.

To activate the A/D converter by the MTU or MMT, set the A/D trigger select register (ADTSR). After this register setting has been made, the ADST bit in ADCR is automatically set to 1 when an A/D conversion request from the interval timer of the MTU or MMT occurs. The timing from setting of the ADST bit until the start of A/D conversion is the same as when 1 is written to the ADST bit by software.

13.4.6 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS0 and TRGS1 bits are set to 00 or 01 in ADTSR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge of the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCR, starting A/D conversion. Other operations, in both single and scan modes, are the same as when the ADST bit has been set to 1 by software. Figure 13.3 shows the timing.

15.7 Usage Notes

15.7.1 Module Standby Mode Setting

MMT operation can be disabled or enabled using the module standby control register. The initial setting is for MMT operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 21, Power-Down Modes.

15.7.2 Notes for MMT Operation

Note that the kinds of operation and contention described below occur during MMT operation.

Contention between Buffer Register Write and Compare Match: If a compare match occurs in the T2 state of a buffer register (TBRU to TBRW, or TPBR) write cycle, data is transferred from the buffer register to the compare register (TGR or TPDR) by a buffer operation. The data transferred is the buffer register write data.

Figure 15.15 shows the timing in this case.

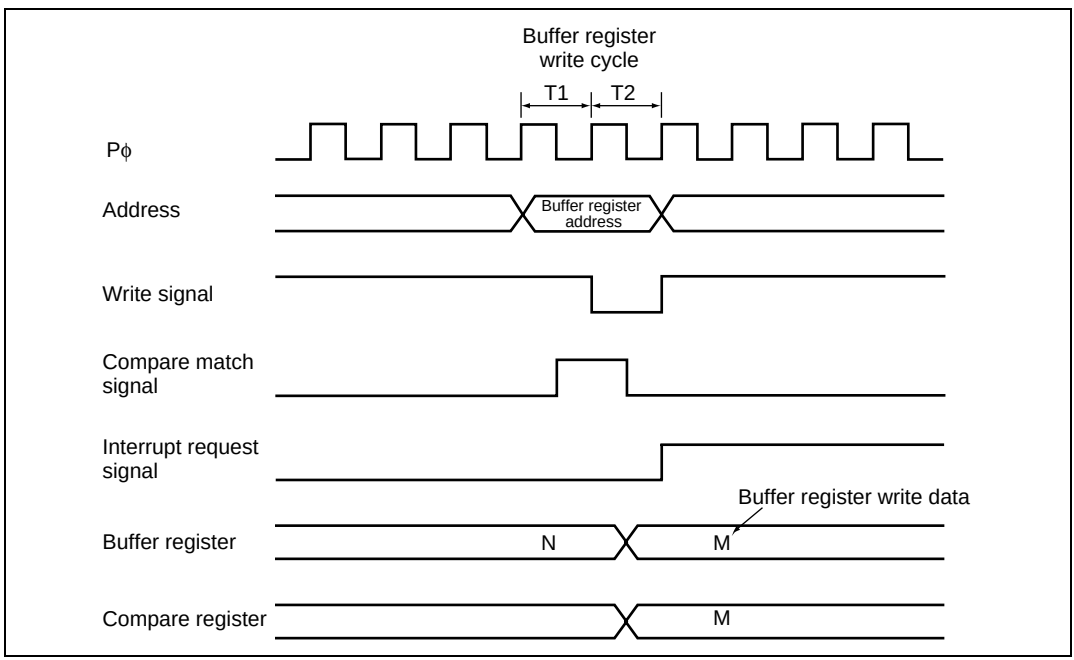

Figure 15.15 Contention between Buffer Register Write and Compare Match

15.8 Port Output Enable (POE)

The port output enable (POE) circuit enables the MMT's output pins (POUA, POUB, POVA, POVB, POWA, and POWB) to be placed in the high-impedance state by varying the input to pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$. An interrupt can also be requested at the same time.

In addition, the MMT's output pins will also enter the high-impedance state in standby mode or when the oscillator halts.

15.8.1 Features

The POE circuit has the following features:

- Falling edge, Pϕ/8 × 16 times, Pϕ/16 × 16 times, or Pϕ/128 × 16 times low-level sampling can be set for each of input pins POE4 to POE6.
- The MMT's output pins can be placed in the high-impedance state at the falling edge or low-level sampling of pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$.
- An interrupt can be generated by input level sampling.

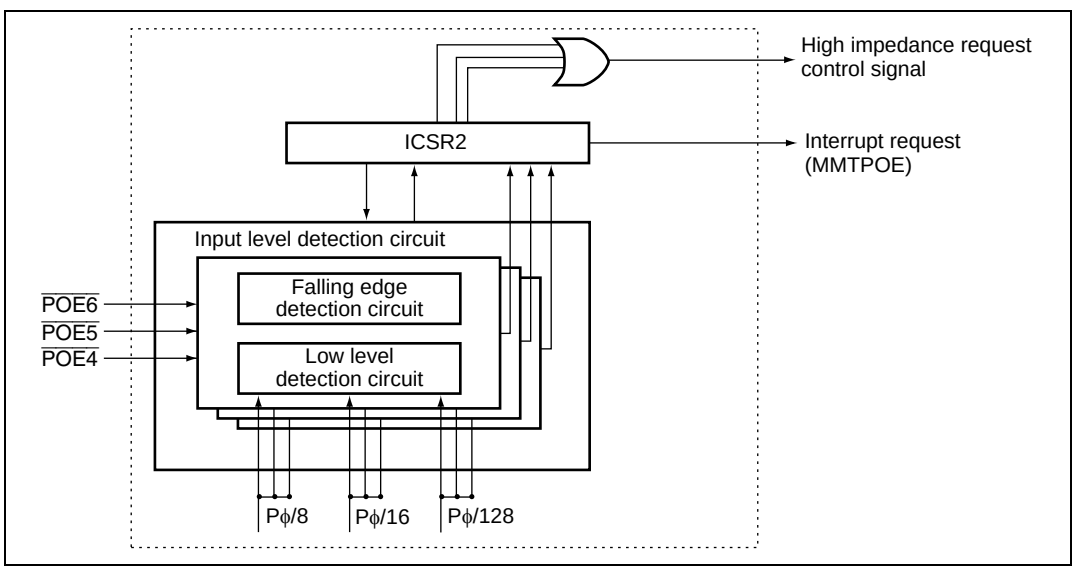

Figure 15.18 Block Diagram of POE

Bit	Bit Name	Initial Value	R/W	Description
7	FWE	1/0	R	Flash Write Enable Reflects the input level at the FWP pin. It is set to 1 when a low level is input to the FWP pin, and cleared to 0 when a high level is input.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1 while the FWE bit is 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, other FLMCR1 bits and all EBR1 and EBR2 bits cannot be set.
5	ESU	0	R/W	Erase Setup When this bit is set to 1 while the FWE and SWE bits are 1, the flash memory changes to the erase setup state. When it is cleared to 0, the erase setup state is cancelled.
4	PSU	0	R/W	Program Setup When this bit is set to 1 while the FWE and SWE bits are 1, the flash memory changes to the program setup state. When it is cleared to 0, the program setup state is cancelled.
3	EV	0	R/W	Erase-Verify When this bit is set to 1 while the FWE and SWE bits are 1, the flash memory changes to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled.
2	PV	0	R/W	Program-Verify When this bit is set to 1 while the FWE and SWE bits are 1, the flash memory changes to program-verify mode. When it is cleared to 0, program-verify mode is cancelled.
1	E	0	R/W	Erase When this bit is set to 1 while the FWE, SWE and ESU bits are 1, the flash memory changes to erase mode. When it is cleared to 0, erase mode is cancelled.
0	P	0	R/W	Program When this bit is set to 1 while the FWE, SWE and PSU bits are 1, the flash memory changes to program mode. When it is cleared to 0, program mode is cancelled.

Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep	Module
TGRA_3	Initialized	Held	Initialized	Initialized	Held	MTU (channels 3 and 4)
TGRB_3	Initialized	Held	Initialized	Initialized	Held	
TGRA_4	Initialized	Held	Initialized	Initialized	Held	
TGRB_4	Initialized	Held	Initialized	Initialized	Held	
TCNTS	Initialized	Held	Initialized	Initialized	Held	
TCBR	Initialized	Held	Initialized	Initialized	Held	
TGRC_3	Initialized	Held	Initialized	Initialized	Held	
TGRD_3	Initialized	Held	Initialized	Initialized	Held	
TGRC_4	Initialized	Held	Initialized	Initialized	Held	
TGRD_4	Initialized	Held	Initialized	Initialized	Held	
TSR_3	Initialized	Held	Initialized	Initialized	Held	
TSR_4	Initialized	Held	Initialized	Initialized	Held	
TSTR	Initialized	Held	Initialized	Initialized	Held	
TSYR	Initialized	Held	Initialized	Initialized	Held	
TCR_0	Initialized	Held	Initialized	Initialized	Held	MTU (channel 0)
TMDR_0	Initialized	Held	Initialized	Initialized	Held	
TIORH_0	Initialized	Held	Initialized	Initialized	Held	
TIORL_0	Initialized	Held	Initialized	Initialized	Held	
TIER_0	Initialized	Held	Initialized	Initialized	Held	
TSR_0	Initialized	Held	Initialized	Initialized	Held	
TCNT_0	Initialized	Held	Initialized	Initialized	Held	
TGRA_0	Initialized	Held	Initialized	Initialized	Held	
TGRB_0	Initialized	Held	Initialized	Initialized	Held	
TGRC_0	Initialized	Held	Initialized	Initialized	Held	
TGRD_0	Initialized	Held	Initialized	Initialized	Held	
TCR_1	Initialized	Held	Initialized	Initialized	Held	
TMDR_1	Initialized	Held	Initialized	Initialized	Held	
TIOR_1	Initialized	Held	Initialized	Initialized	Held	
TIER_1	Initialized	Held	Initialized	Initialized	Held	
TSR_1	Initialized	Held	Initialized	Initialized	Held	
TCNT_1	Initialized	Held	Initialized	Initialized	Held	