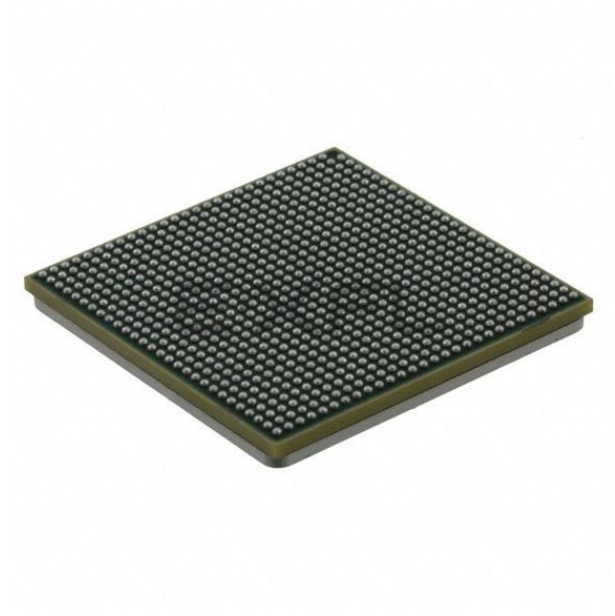

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8154sag1000b

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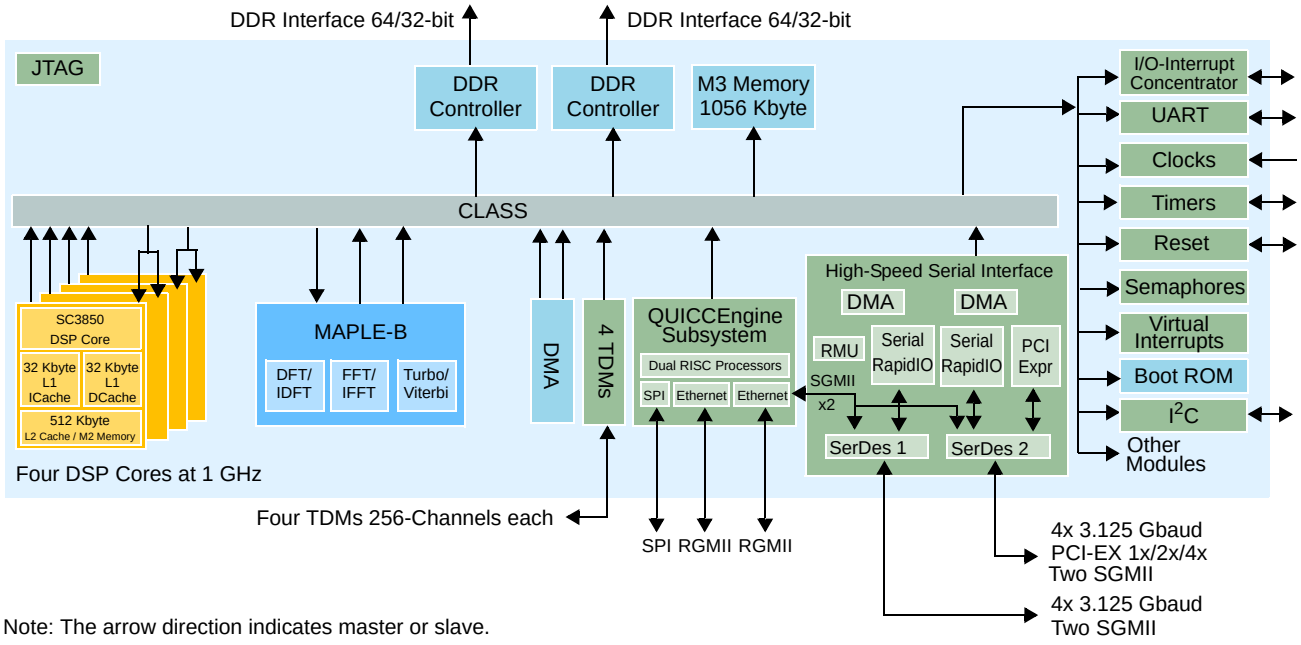


Figure 1. MSC8154 Block Diagram

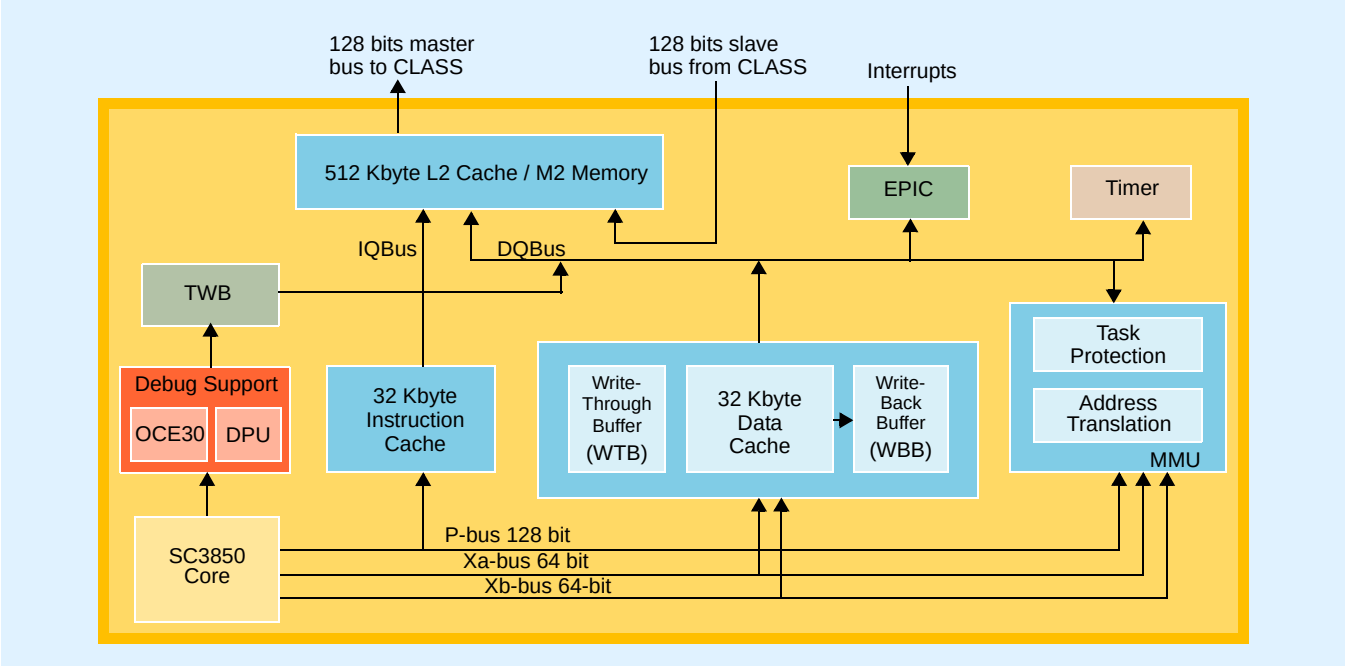


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
G7	M2CKE0	O	GVDD2
G8	M2A11	O	GVDD2
G9	M2A7	O	GVDD2
G10	$\overline{\text{M2CK2}}$	O	GVDD2
G11	M2APAR_OUT	O	GVDD2
G12	M2ODT1	O	GVDD2
G13	$\overline{\text{M2APAR\_IN}}$	I	GVDD2
G14	M2DQ43	I/O	GVDD2
G15	M2DM5	O	GVDD2
G16	M2DQ44	I/O	GVDD2
G17	M2DQ40	I/O	GVDD2
G18	M2DQ59	I/O	GVDD2
G19	M2DM7	O	GVDD2
G20	M2DQ60	I/O	GVDD2
G21	Reserved	NC	—
G22	Reserved	NC	—
G23	SXPVSS1	Ground	N/A
G24	SXPVDD1	Power	N/A
G25	SR1_IMP_CAL_TX	I	SXCVDD1
G26	SXCVSS1	Ground	N/A
G27	Reserved	NC	—
G28	Reserved	NC	—
H1	GVDD2	Power	N/A
H2	VSS	Ground	N/A
H3	M2DQ18	I/O	GVDD2
H4	GVDD2	Power	N/A
H5	VSS	Ground	N/A
H6	M2DQ20	I/O	GVDD2
H7	GVDD2	Power	N/A
H8	VSS	Ground	N/A
H9	M2A15	O	GVDD2
H10	M2CK2	O	GVDD2
H11	M2MDIC0	I/O	GVDD2
H12	M2VREF	I	GVDD2
H13	M2MDIC1	I/O	GVDD2
H14	M2DQ46	I/O	GVDD2
H15	M2DQ47	I/O	GVDD2
H16	M2DQ45	I/O	GVDD2
H17	M2DQ41	I/O	GVDD2
H18	M2DQ62	I/O	GVDD2
H19	M2DQ63	I/O	GVDD2
H20	M2DQ61	I/O	GVDD2
H21	Reserved	NC	—
H22	Reserved	NC	—
H23	SR1_TXD3/SG2_TX[4]	O	SXPVDD1
H24	$\overline{\text{SR1\_TXD3}}$/$\overline{\text{SG2\_TX}}$[4]	O	SXPVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
M5	M2DQ1	I/O	GVDD2
M6	VSS	Ground	N/.A
M7	GVDD2	Power	N/A
M8	M2DQ7	I/O	GVDD2
M9	M2DQ6	I/O	GVDD2
M10	VSS	Ground	N/A
M11	VDD	Power	N/A
M12	VSS	Ground	N/A
M13	VDD	Power	N/A
M14	VSS	Ground	N/A
M15	VSS	Ground	N/A
M16	VSS	Ground	N/A
M17	VSS	Ground	N/A
M18	VSS	Ground	N/A
M19	VDD	Power	N/A
M20	Reserved	NC	—
M21	Reserved	NC	—
M22	Reserved	NC	—
M23	SXPVSS2	Ground	N/A
M24	SXPVDD2	Power	N/A
M25	SR2_IMP_CAL_TX	I	SXCVDD2
M26	SXCVSS2	Ground	N/A
M27	Reserved	NC	—
M28	Reserved	NC	—
N1	VSS	Ground	N/A
N2	$\overline{\text{TRST}}$[7]	I	QVDD
N3	$\overline{\text{PORESET}}$[7]	I	QVDD
N4	VSS	Ground	N/A
N5	TMS[7]	I	QVDD
N6	CLKOUT	O	QVDD
N7	VSS	Ground	N/A
N8	VSS	Ground	N/A
N9	VSS	Ground	N/A
N10	VDD	Power	N/A
N11	VSS	Ground	N/A
N12	M3VDD	Power	N/A
N13	VSS	Ground	N/A
N14	VSS	Ground	N/A
N15	VSS	Ground	N/A
N16	VDD	Power	N/A
N17	VSS	Ground	N/A
N18	VDD	Power	N/A
N19	VSS	Ground	N/A
N20	Reserved	NC	—
N21	SXPVDD2	Power	N/A
N22	SXPVSS2	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS}}$5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- I^2C
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$)
- Clock and resets (CLKIN, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

Table 17. 2.5 V I/O DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input high current ($V_{IN} = V_{DDIO}$)	I_{IN}	—	30	μA	2
Output high voltage (V_{DDIO} = min, I_{OH} = –1.0 mA)	V_{OH}	2.0	VDDIO + 0.3	V	1
Output low voltage (V_{DDIO} = min, I_{OL}= 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	1

Notes: **1.** The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values listed in Table 3.
2. The symbol V_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8154.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.20	V
AC input high voltage	V_{IH}	MV_{REF} + 0.20	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 19 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 19. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.				

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}				1, 2
• 800 MHz data rate		–200	200	ps	
• 667 MHz data rate		–240	240	ps	
Tolerated Skew for MDQS—MDQ/MECC/MDM	t_{DISKEW}				2, 3
• 800 MHz data rate		–425	425	ps	
• 667 MHz data rate		–510	510	ps	

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

2.6.2.2 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8154 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 25 and the receiver specifications are defined in Table 26. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 25. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit interval	UI	399.88	400.00	400.12	ps	1
Minimum Tx eye width	T_{TX-EYE}	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	3, 4
AC coupling capacitor	C_{TX}	75	—	200	nF	5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 – T_{TX-EYE} = 0.3$ UI.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 8 and measured over any 250 consecutive Tx UIs. A $T_{TX-EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.30$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data.
4. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.
5. All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself. The SerDes transmitter does not have built-in Tx capacitance. An external AC coupling capacitor is required.

Table 26. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	3, 4, 5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 – T_{RX-EYE} = 0.6$ UI.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 8 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Figure 21 shows the TDM transmit signal timing.

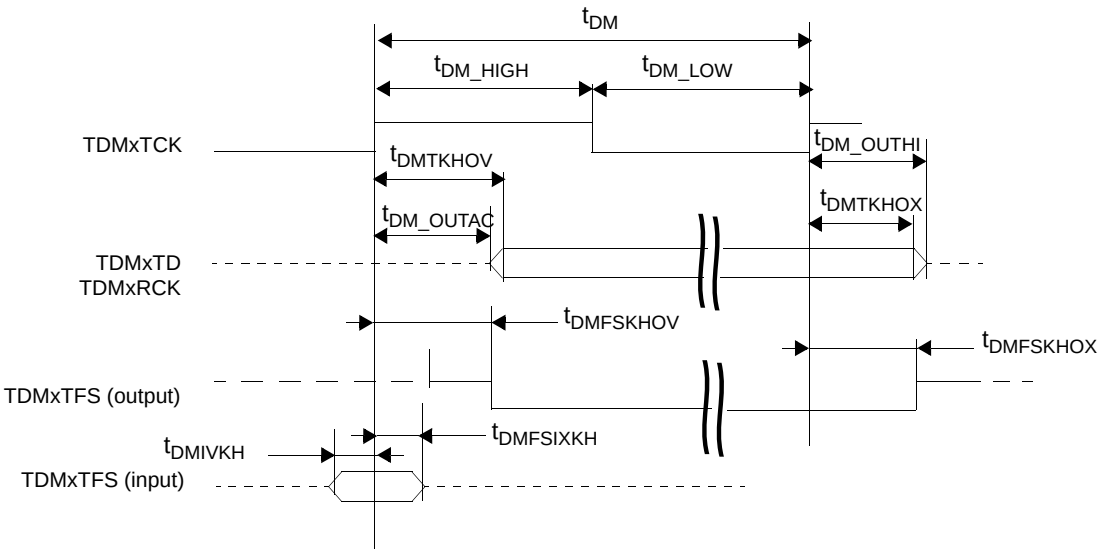


Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

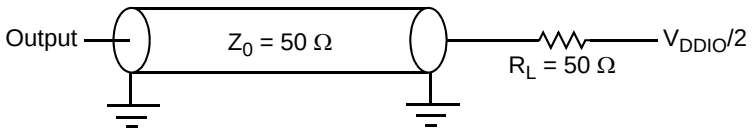


Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

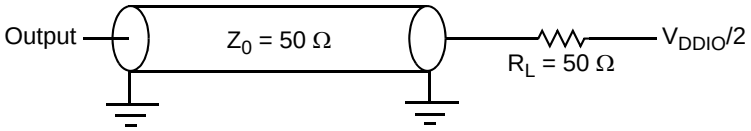


Figure 23. Timer AC Test Load

2.6.5 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8154 Reference Manual*.

2.6.5.1 Management Interface Timing

Table 33 lists the timer input Ethernet controller management interface timing specifications shown in Figure 24.

Table 33. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay[2]	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the GE_MDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8154 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

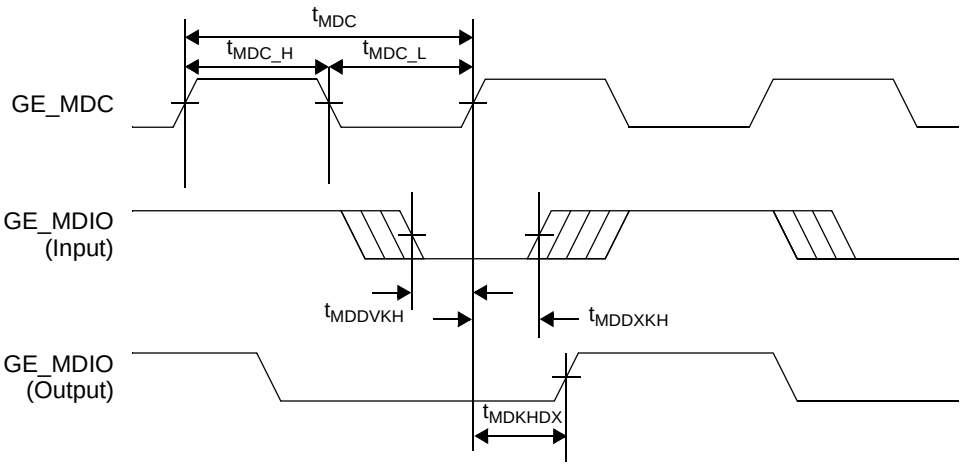


Figure 24. MII Management Interface Timing

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps[2] with On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–-0.5	—	0.5	ns
Data to clock input skew (at receiver) [4]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. Program GCR4 as 0x00000000.
4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps[2] with No On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–2.6	—	–1.0	ns
Data to clock input skew (at receiver)[4]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. GCR4 should be programmed as 0x000CC330.
4. This implies that PC board design requires clocks to be routed with no additional trace delay

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

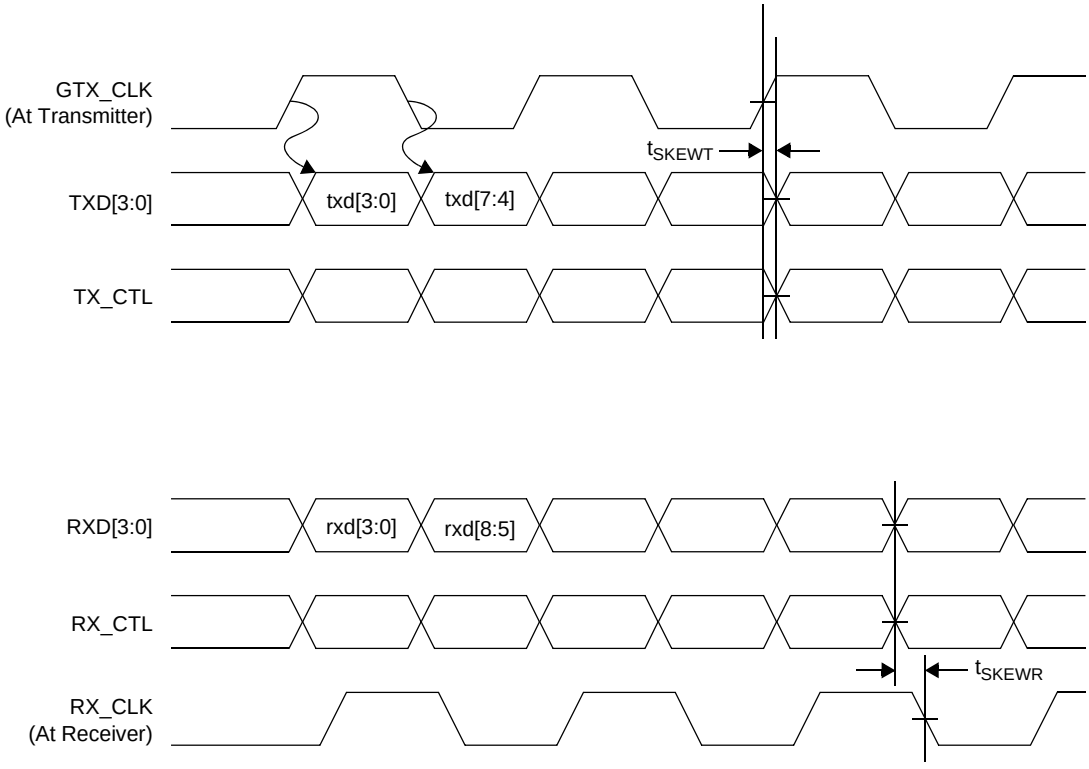


Figure 25. RGMII AC Timing and Multiplexing

Figure 30 shows the boundary scan (JTAG) timing diagram.

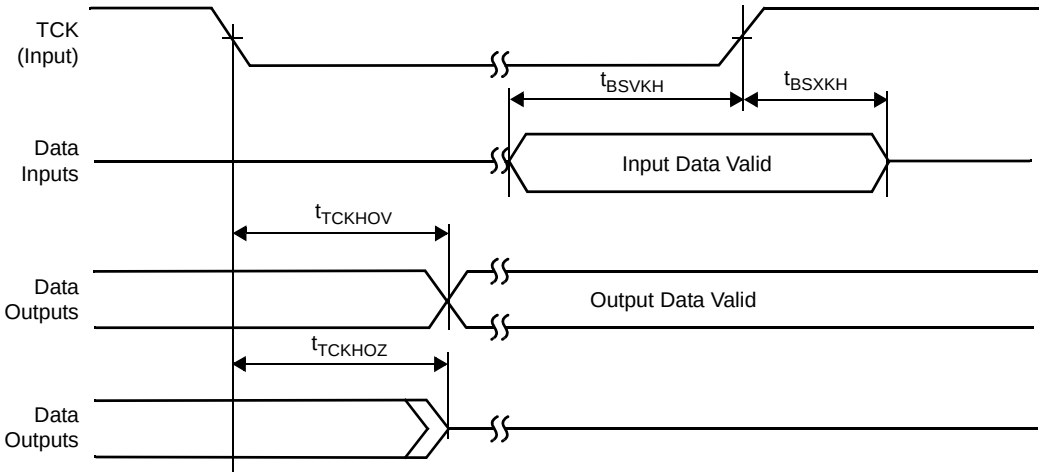


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

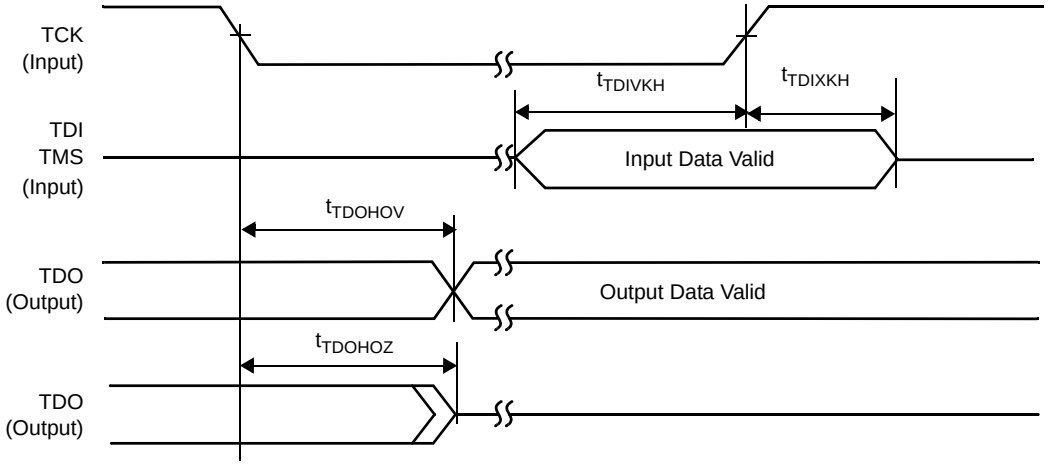


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 32. $\overline{\text{TRST}}$ Timing

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

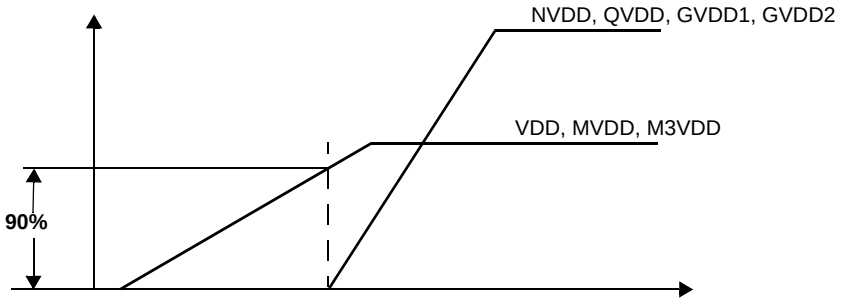


Figure 34. Supply Ramp-Up Sequence

Notes:
1. If the M3 memory is not used, M3VDD can be tied to GND.
2. If the MAPLE-B is not used, MVDD can be tied to GND.
3. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
4. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
5. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
6. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

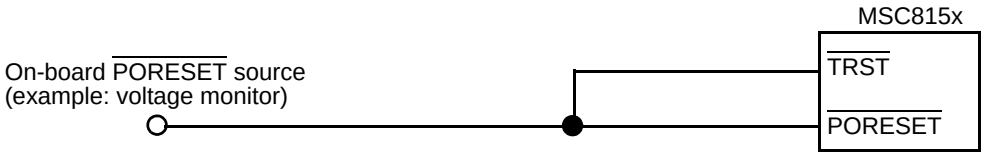


Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in Figure 36.

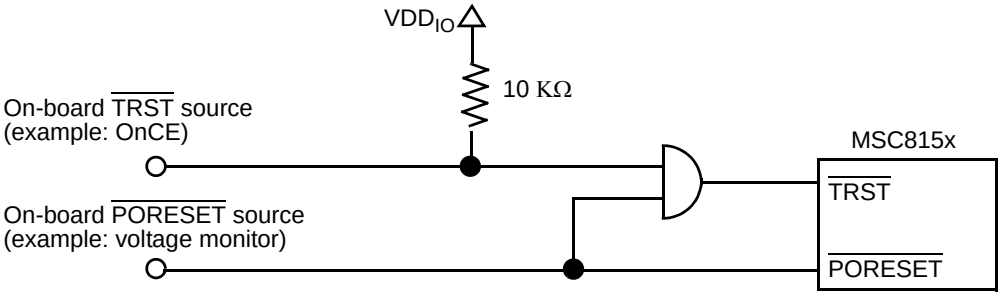


Figure 36. Reset Connection in Debugger Application

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.

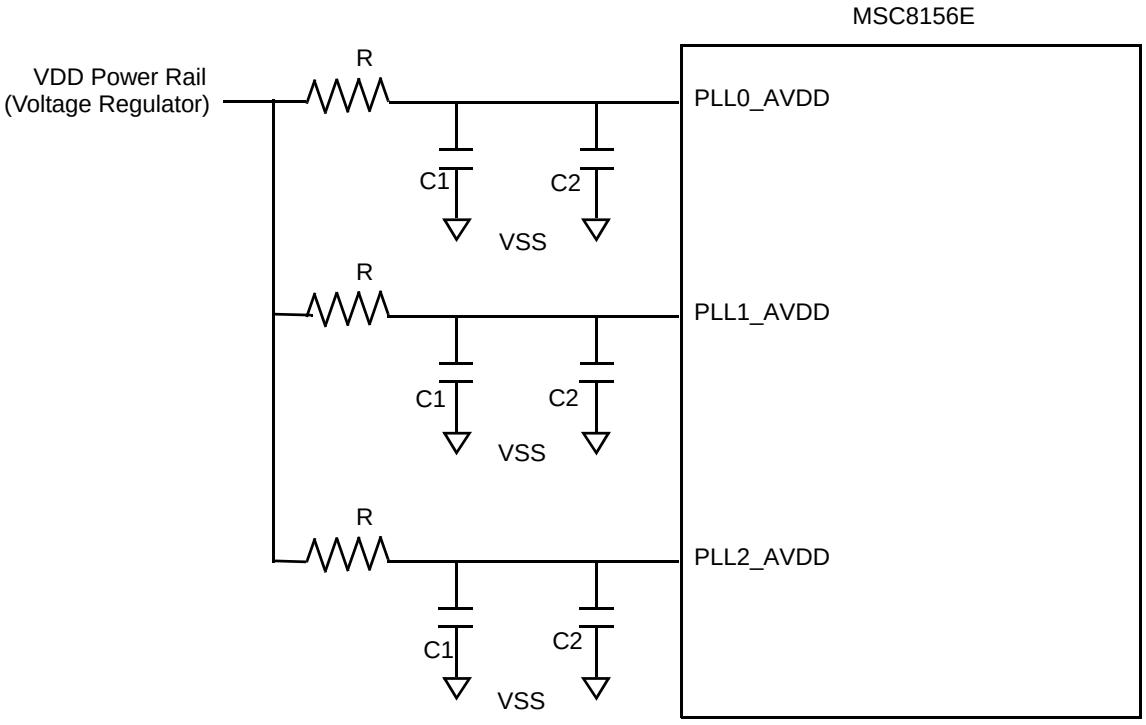


Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

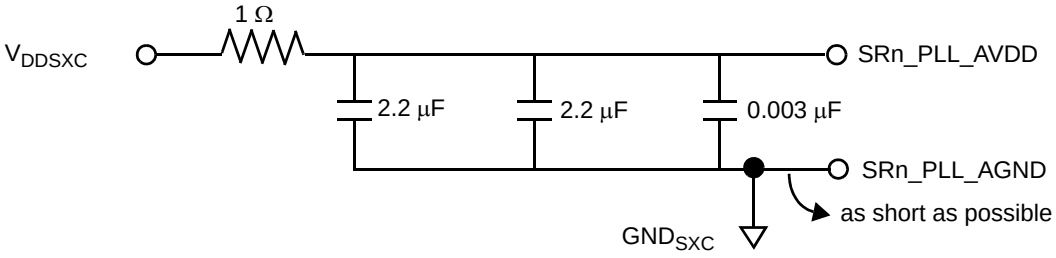


Figure 38. SerDes PLL Supplies

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used (continued)

Signal Name	Pin Connection
SR[1–2]_RXD***n***	SXCVSS
$\overline{\text{SR[1–2]\_RXD}\textit{n}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD}\textit{n}}$	NC
SR[1–2]_TXD***n***	NC
SR[1–2]_PLL_AVDD	in use
SR[1–2]_PLL_AGND	in use
SXPVSS	in use
SXCVSS	in use
SXPVDD	in use
SXCVDD	in use
Note: The ***n*** indicates the lane number {0,1,2,3} for all unused lanes.	

3.5.3 RGMII Ethernet Related Pins

Note: Table 46 and Table 47 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

Table 46. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used

Signal Name	Pin Connection
GE1_RX_CTL	GND
GE2_TX_CTL	NC
Note: Assuming GE1 and GE2 are disabled in the reset configuration word.	

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used, Table 47 lists the recommended management pin connections.

Table 47. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

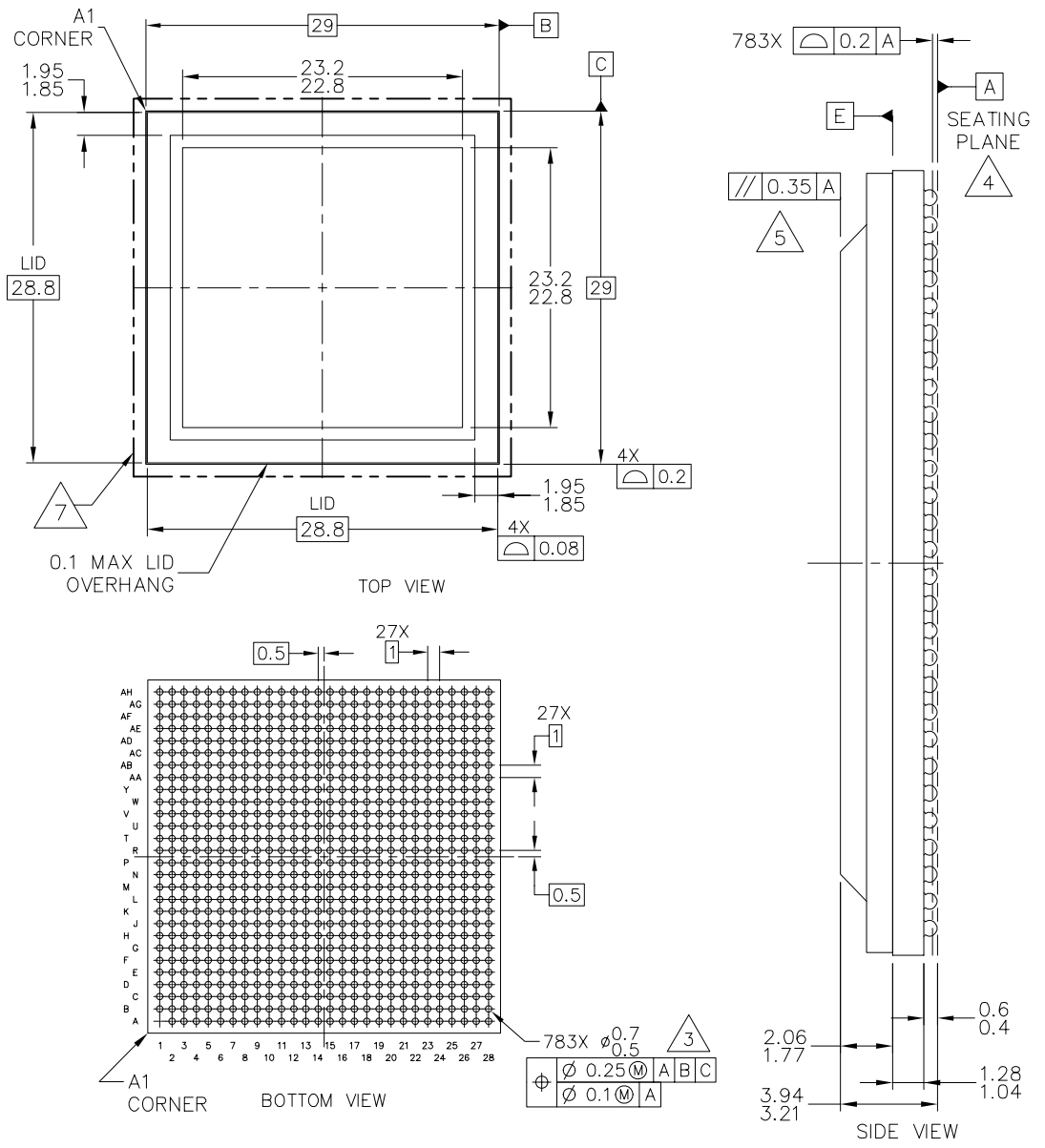
3.5.4 TDM Interface Related Pins

Table 48 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 48 for those signals that are not selected. Table 48 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***RCLK	GND
TDM***n***RDAT	GND
TDM***n***RSYN	GND

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 40. MSC8154 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8154 Technical Data Sheet* (MSC8154). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8154 device.
- *MSC8154 Reference Manual* (MSC8154RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8154 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 50 provides a revision history for this data sheet.

Table 50. Document Revision History

Rev.	Date	Description
0	Apr. 2010	• Initial public release.
1	May 2010	• Changed connection for pins K17, L14, L16, M15, M17, and N14 from VDD to VSS in Table 1. • Updated **Section 3.1.2**, *Power-On Ramp Time*.
2	Dec 2010	• Updated Table 16. • Updated **Section 3.1.2**, *Power-On Ramp Time*.
3	Mar 2011	• Updated Table 8. • Updated Table 15. • Updated Table 17. • Updated Table 33. • Updated Table 35. • Updated Table 39.
4	May 2011	• Updated Table 1. Changed the pin types for the following: – F25 from ground to power. – F26 from power to ground. – T6 from power to O.
5	Oct 2011	• Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz.
6	Dec 2011	• Added note 4 to Table 39.
7	Aug 2013	• Updated Section 4, “Ordering Information”.

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