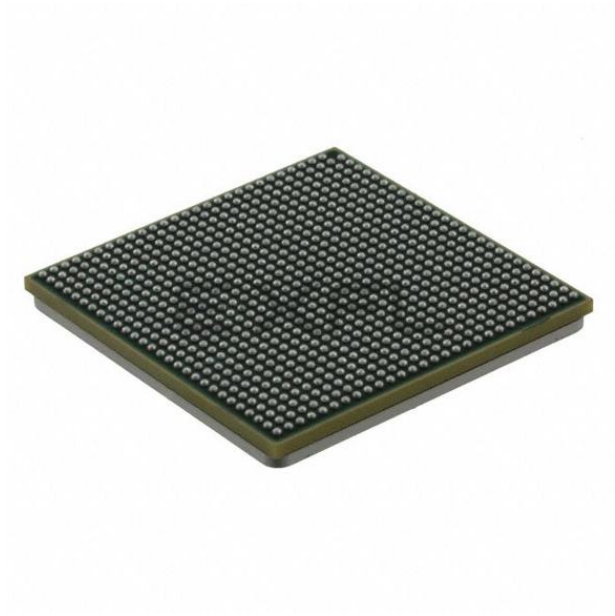

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8154svt1000b

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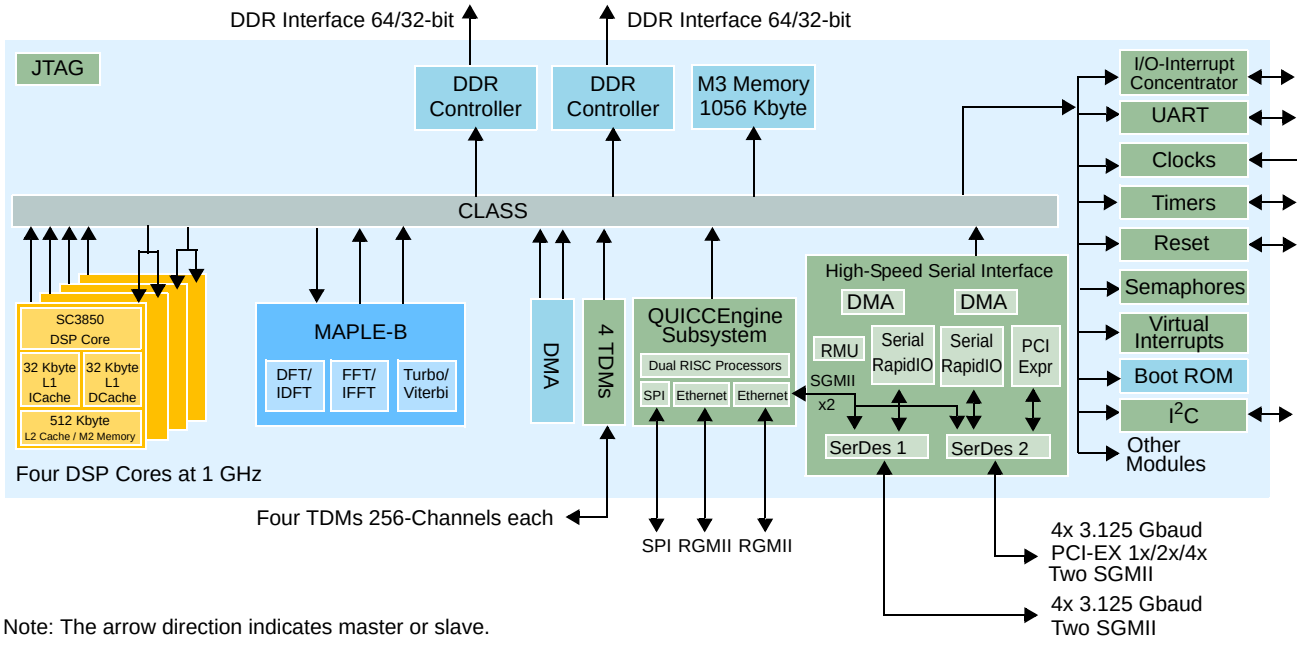

Figure 1. MSC8154 Block Diagram

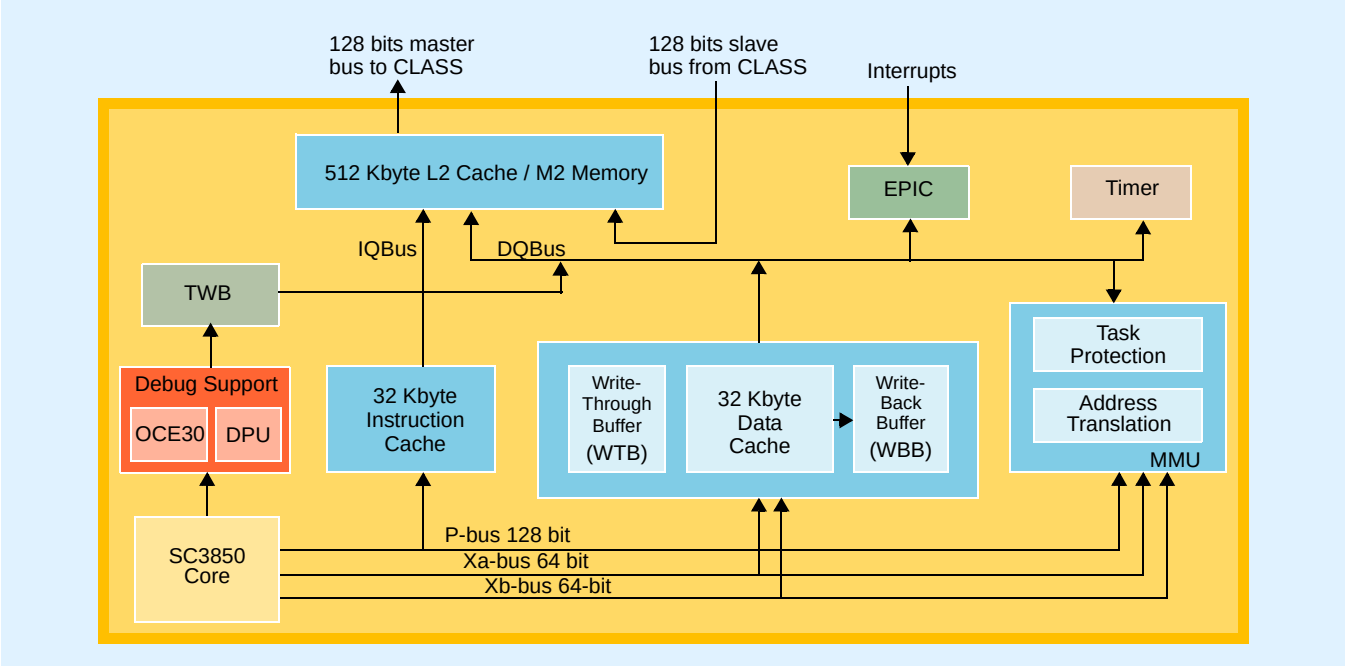

Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
H25	SXCVSS1	Ground	N/A
H26	SXCVDD1	Power	N/A
H27	$\overline{\text{SR1\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD1
H28	SR1_RXD3/SG2_RX[4]	I	SXCVDD1
J1	M2DQS1	I/O	GVDD2
J2	$\overline{\text{M2DQS1}}$	I/O	GVDD2
J3	M2DQ10	I/O	GVDD2
J4	M2DQ11	I/O	GVDD2
J5	M2DQ14	I/O	GVDD2
J6	M2DQ23	I/O	GVDD2
J7	M2ODT0	O	GVDD2
J8	M2A12	O	GVDD2
J9	M2A14	O	GVDD2
J10	VSS	Ground	N/A
J11	GVDD2	Power	N/A
J12	VSS	Ground	N/A
J13	GVDD2	Power	N/A
J14	VSS	Ground	N/A
J15	GVDD2	Power	N/A
J16	VSS	Ground	N/A
J17	GVDD2	Power	N/A
J18	VSS	Ground	N/A
J19	GVDD2	Power	N/A
J20	Reserved	NC	—
J21	Reserved	NC	—
J22	Reserved	NC	—
J23	SXPVDD1	Power	N/A
J24	SXPVSS1	Ground	N/A
J25	SXCVDD1	Power	N/A
J26	SXCVSS1	Ground	N/A
J27	SXCVDD1	Power	N/A
J28	SXCVSS1	Ground	N/A
K1	VSS	Ground	N/A
K2	GVDD2	Power	N/A
K3	M2DM1	O	GVDD2
K4	VSS	Ground	N/A
K5	GVDD2	Power	N/A
K6	M2DQ0	I/O	GVDD2
K7	VSS	Ground	N/A
K8	GVDD2	Power	N/A
K9	M2DQ5	I/O	GVDD2
K10	VSS	Ground	N/A
K11	VDD	Power	N/A
K12	VSS	Ground	N/A
K13	VDD	Power	N/A
K14	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
R13	VSS	Ground	N/A
R14	VDD	Power	N/A
R15	VSS	Ground	N/A
R16	MVDD	Power	N/A
R17	VSS	Ground	N/A
R18	VDD	Power	N/A
R19	VSS	Ground	N/A
R20	VSS	Non-user	N/A
R21	SXPVSS2	Ground	N/A
R22	SXPVDD2	Power	N/A
R23	SR2_TXD1/PE_TXD1[4]	O	SXPVDD2
R24	$\overline{\text{SR2\_TXD1}}/\overline{\text{PE\_TXD1}}$[4]	O	SXPVDD2
R25	SXCVSS2	Ground	N/A
R26	SXCVDD2	Power	N/A
R27	$\overline{\text{SR2\_RXD1}}/\overline{\text{PE\_RXD1}}$[4]	I	SXCVDD2
R28	SR2_RXD1/PE_RXD1[4]	I	SXCVDD2
T1	VSS	Ground	N/A
T2	TCK	I	QVDD
T3	$\overline{\text{SRESET}}$[6,7]	I/O	QVDD
T4	TDI	I	QVDD
T5	VSS	Ground	N/A
T6	TDO	O	QVDD
T7	VSS	Ground	N/A
T8	VSS	Ground	N/A
T9	QVDD	Power	N/A
T10	VSS	Ground	N/A
T11	VDD	Power	N/A
T12	VSS	Ground	N/A
T13	M3VDD	Power	N/A
T14	VSS	Ground	N/A
T15	VDD	Power	N/A
T16	VSS	Ground	N/A
T17	MVDD	Power	N/A
T18	VSS	Ground	N/A
T19	VDD	Power	N/A
T20	VSS	Ground	N/A
T21	VSS	Non-user	N/A
T22	SR2_IMP_CAL_RX	I	SXCVDD2
T23	SXPVSS2	Ground	N/A
T24	SXPVDD2	Power	N/A
T25	SR2_REF_CLK	I	SXCVDD2
T26	$\overline{\text{SR2\_REF\_CLK}}$	I	SXCVDD2
T27	Reserved	NC	—
T28	Reserved	NC	—
U1	M1DQ8	I/O	GVDD1
U2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
U3	GVDD1	Power	N/A
U4	M1DQ15	I/O	GVDD1
U5	M1DQ1	I/O	GVDD1
U6	VSS	Ground	N/A
U7	GVDD1	Power	N/A
U8	M1DQ7	I/O	GVDD1
U9	M1DQ6	I/O	GVDD1
U10	VDD	Power	N/A
U11	VSS	Ground	N/A
U12	M3VDD	Power	N/A
U13	VSS	Ground	N/A
U14	VDD	Power	N/A
U15	VSS	Ground	N/A
U16	VDD	Power	N/A
U17	VSS	Ground	N/A
U18	VDD	Power	N/A
U19	VSS	Ground	N/A
U20	VSS	Ground	N/A
U21	VSS	Ground	N/A
U22	VSS	Non-user	N/A
U23	SR2_TXD0/PE_TXD0[4]	O	SXPVDD2
U24	$\overline{\text{SR2\_TXD0}}/\overline{\text{PE\_TXD0}}$[4]	O	SXPVDD2
U25	SXCVDD2	Power	N/A
U26	SXCVSS2	Ground	N/A
U27	$\overline{\text{SR2\_RXD0}}/\overline{\text{PE\_RXD0}}$[4]	I	SXCVDD2
U28	SR2_RXD0/PE_RXD0[4]	I	SXCVDD2
V1	M1DQ9	I/O	GVDD1
V2	M1DQ12	I/O	GVDD1
V3	M1DQ13	I/O	GVDD1
V4	$\overline{\text{M1DQS0}}$	I/O	GVDD1
V5	M1DQS0	I/O	GVDD1
V6	M1DM0	O	GVDD1
V7	M1DQ3	I/O	GVDD1
V8	M1DQ2	I/O	GVDD1
V9	M1DQ4	I/O	GVDD1
V10	VSS	Ground	N/A
V11	VDD	Power	N/A
V12	VSS	Ground	N/A
V13	VDD	Power	N/A
V14	VSS	Ground	N/A
V15	VDD	Power	N/A
V16	VSS	Ground	N/A
V17	VDD	Power	N/A
V18	VSS	Ground	N/A
V19	VDD	Power	N/A
V20	NVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
Y11	GVDD1	Power	N/A
Y12	VSS	Ground	N/A
Y13	GVDD1	Power	N/A
Y14	VSS	Ground	N/A
Y15	GVDD1	Power	N/A
Y16	VSS	Ground	N/A
Y17	GVDD1	Power	N/A
Y18	VSS	Ground	N/A
Y19	GVDD1	Power	N/A
Y20	VSS	Ground	N/A
Y21	NVDD	Power	N/A
Y22	GPIO20/$\overline{\text{SPI\_SL}}$[5,8]	I/O	NVDD
Y23	GPIO17/SPI_SCK[5,8]	I/O	NVDD
Y24	GPIO14/DRQ0/$\overline{\text{IRQ14}}$/RC14[5,8]	I/O	NVDD
Y25	GPIO12/$\overline{\text{IRQ12}}$/RC12[5,8]	I/O	NVDD
Y26	GPIO8/$\overline{\text{IRQ8}}$/RC8[5,8]	I/O	NVDD
Y27	NVDD	Power	N/A
Y28	VSS	Ground	N/A
AA1	GVDD1	Power	N/A
AA2	VSS	Ground	N/A
AA3	M1DQ18	I/O	GVDD1
AA4	GVDD1	Power	N/A
AA5	VSS	Ground	N/A
AA6	M1DQ20	I/O	GVDD1
AA7	GVDD1	Power	N/A
AA8	VSS	Ground	N/A
AA9	M1A15	O	GVDD1
AA10	M1CK2	O	GVDD1
AA11	M1MDIC0	I/O	GVDD1
AA12	M1VREF	I	GVDD1
AA13	M1MDIC1	I/O	GVDD1
AA14	M1DQ46	I/O	GVDD1
AA15	M1DQ47	I/O	GVDD1
AA16	M1DQ45	I/O	GVDD1
AA17	M1DQ41	I/O	GVDD1
AA18	M1DQ62	I/O	GVDD1
AA19	M1DQ63	I/O	GVDD1
AA20	M1DQ61	I/O	GVDD1
AA21	VSS	Ground	N/A
AA22	GPIO21[5,8]	I/O	NVDD
AA23	GPIO18/SPI_MOSI[5,8]	I/O	NVDD
AA24	GPIO16/RC16[5,8]	I/O	NVDD
AA25	GPIO4/DDN1/$\overline{\text{IRQ4}}$/RC4[5,8]	I/O	NVDD
AA26	GPIO9/$\overline{\text{IRQ9}}$/RC9[5,8]	I/O	NVDD
AA27	GPIO6/$\overline{\text{IRQ6}}$/RC6[5,8]	I/O	NVDD
AA28	GPIO1/$\overline{\text{IRQ1}}$/RC1[5,8]	I/O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AE9	M1A8	O	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	O	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD[5,8]	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK[3]	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL[3]	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK[3]	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK[3]	I/O	NVDD
AE27	TDM2RSN/GE1_TD2[3]	I/O	NVDD
AE28	TDM2RDT/GE1_TD1[3]	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	O	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	O	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	O	GVDD1
AF8	M1CK0	O	GVDD1
AF9	$\overline{\text{M1CK0}}$	O	GVDD1
AF10	M1BA1	O	GVDD1
AF11	M1A1	O	GVDD1
AF12	$\overline{\text{M1WE}}$	O	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	O	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	O	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD[5,8]	I/O	NVDD
AF22	TDM0RSN/GE2_TD2[3]	I/O	NVDD
AF23	TDM0TDT/GE2_TD3[3]	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL[3]	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8154 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8154.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
MAPLE-B supply voltage	MVDD	V_{DDM}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8154 (see Figure 37 and Figure 38)

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8154.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8154.

Note: DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V and DDR3 SDRAM uses V_{DDDDR}(typ) = 1.5 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V.

Table 6. DDR2 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	0.49 × V_{DDDDR}	0.51 × V_{DDDDR}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.125	V_{DDDDR} + 0.3	V	5
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} (VOH) = 1.37 V)	I_{OH}	–13.4	—	mA	7
Output low current (V_{OUT} (VOL) = 0.33 V)	I_{OL}	13.4	—	mA	7

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to 0.5 × V_{DDDDR} and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 300 μA.
5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, 0 V ≤ V_{OUT} ≤ V_{DDDDR}.
7. Refer to the IBIS model for the complete output IV curve characteristics.

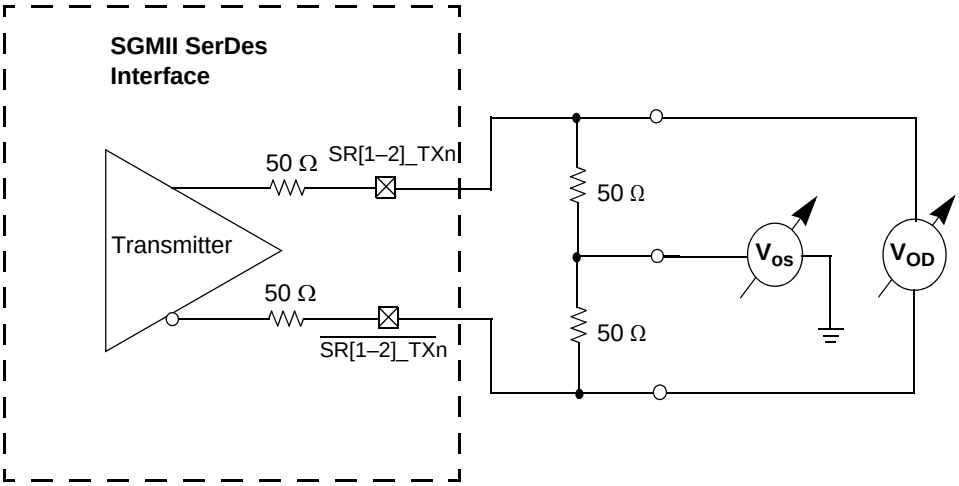

Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16. SGMII DC Receiver Electrical Characteristics[5]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—		N/A		—	1
Input differential voltage	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		175	—			
Loss of signal threshold	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	VLOS	30	—	100	mV	3, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	W	—

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.
4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.
5. The supply voltage is 1.0 V.

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8154.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.20	V
AC input high voltage	V_{IH}	MV_{REF} + 0.20	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 19 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 19. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.				

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}				1, 2
• 800 MHz data rate		–200	200	ps	
• 667 MHz data rate		–240	240	ps	
Tolerated Skew for MDQS—MDQ/MECC/MDM	t_{DISKEW}				2, 3
• 800 MHz data rate		–425	425	ps	
• 667 MHz data rate		–510	510	ps	

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SR[1–2]_REF_CLK) to falling edge rate (SR[1–2]_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6

Figure 21 shows the TDM transmit signal timing.

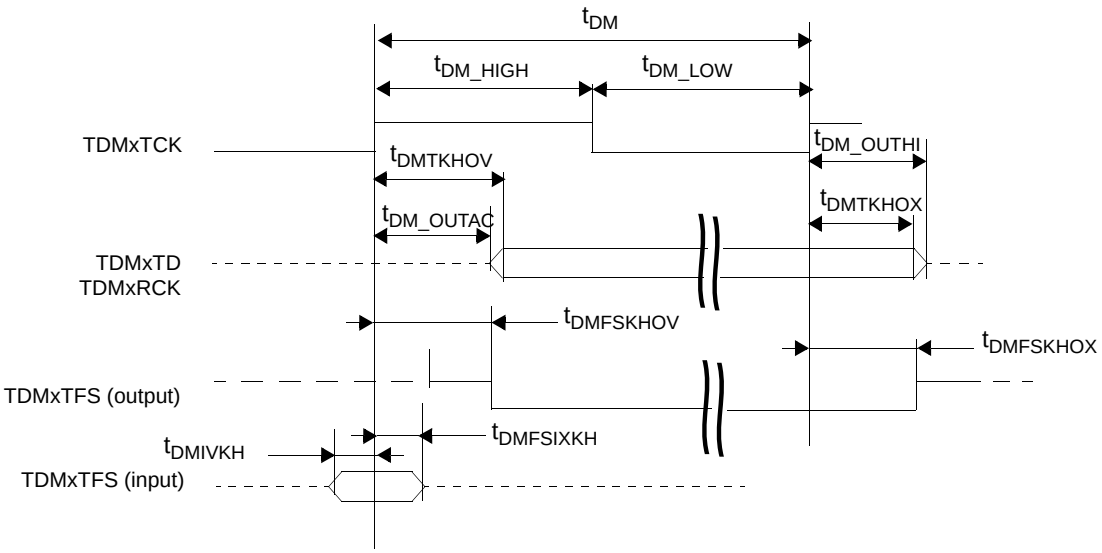

Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

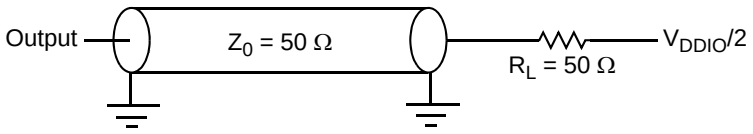

Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

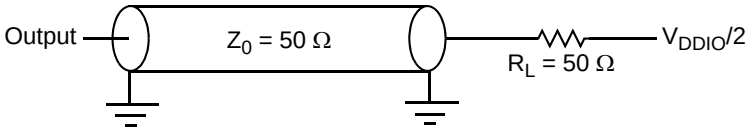

Figure 23. Timer AC Test Load

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

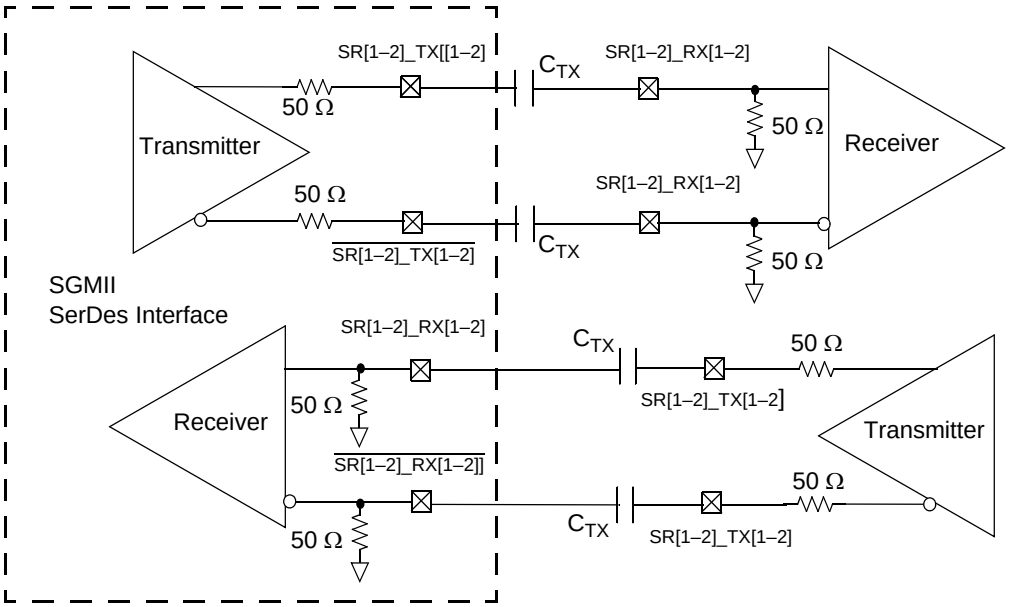

Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor is clearly indicated as “pull-up/pull-down.” For buses, each pin on the bus should have its own resistor.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection
MDQ[31–0]	in use
MDQ[63–32]	NC
MDQS[3–0]	in use
MDQS[7–4]	NC
$\overline{\text{MDQS}}$[3–0]	in use
$\overline{\text{MDQS}}$[7–4]	NC
MA[15–0]	in use
MCK[2–0]	in use
$\overline{\text{MCK}}$[2–0]	in use
$\overline{\text{MCS}}$[1–0]	in use
MDM[3–0]	in use
MDM[7–4]	NC
MBA[2–0]	in use
$\overline{\text{MCAS}}$	in use
MCKE[1–0]	in use
MODT[1–0]	in use
MMDIC[1–0]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MVREF	in use
GVDD1/GVDD2	in use

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8154 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8154, connecting these pins to GND increases device power consumption.

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

Table 42. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8154 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8154, connecting these pins to GND increases device power consumption.

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***TCLK	GND
TDMT***n***DAT	GND
TDM***n***TSYN	GND
V_{DDIO}	2.5 V

Notes: 1. ***n*** = {0, 1, 2,3}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See *TDM* chapter in the ***MSC8154 Reference Manual*** for details.

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[15–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 3.1** for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
V_{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8154 Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* W10, T19
- *VSS:* J18, Y10
- *M3VDD:* None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Qual Status	Cores	Encryption	Temeprature Range	Package Type	Core Frequency	Die Revision
PC = Prototype MSC = Production	8154 = 4 Core	[blank] = Non-encrypted	S = 0° to 105°C T = –40°C to 105°C	VT = FC-PBGA Lead Free AG = FC-PBGA C4/C5 Lead Free	1000 = 1Ghz	B = Rev 2.1